A Multirate Digital Controller for an Electric Vehicle Battery Charger

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Abstract

This paper describes a power electronic system that, among other possibilities, can be used to charge electric vehicle batteries. A large-signal linear, multirate digital controller for the charging current permits the charger to track and deliver a desired current trajectory for a wide range of loads. This controller simultaneously ensures that the charger draws power from the electric utility with unity power factor. The analytical development of the controller and experimental results from a prototype charger are presented.

I. Introduction

In a *regulation* application, a power supply is typically tasked with maintaining a fixed voltage or current in the face of possible disturbances. Control schemes based on small-signal linearized models are often completely adequate for such power supplies, for at least two reasons. First, the power supply does in fact generally operate around a nominal operating point, and the assumptions made in developing a small-signal model for control are therefore reasonable. Second, precise quantitative characterization of the recovery characteristics from extreme transients may not be necessary or may be empirically or approximately determined. Large energy storage elements (capacitors and inductors, or even batteries) can, for a price, substantially moderate the effect of disturbances. As long as a designer includes sufficient filtering or energy storage to ensure adequate operation within accepted tolerances for a range of typical conditions and disturbances, only qualitative stability information may be necessary regarding extreme transients. This large-signal stability is often "guaranteed" with relatively *ad hoc* arguments.

In a *tracking* application, on the other hand, a controller works to cause an output voltage or current to follow (within some tolerance) a desired reference waveform as a function of time or some other variable. There may be no single nominal operating point for the converter, and its controller must provide stable, well-characterized performance in the presence of large signal variations. Also, for reliable tracking, a relatively high-bandwidth control scheme may be essential.

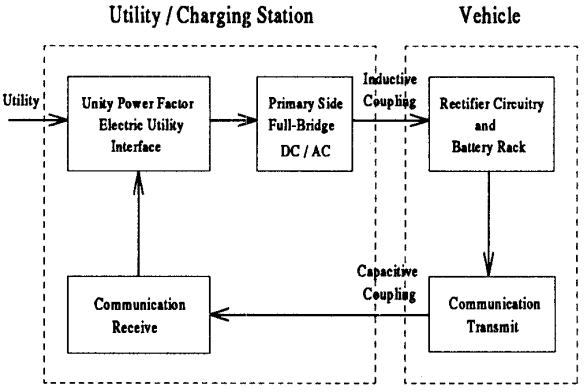

Figure 1: Charging system overview.

Consider, for example, a power electronic charger for electric vehicle batteries. Depending on the battery, especially with advanced or proposed battery technologies, the controller may be required to follow large, rapid changes in a charging-current reference. This is a tracking application.

We are engaged in exploring the use of a boost-type UPF rectifier in a charging system illustrated in the block diagram in Fig. 1. This system is similar to topologies considered in [1]. Power is transferred to the vehicle through an inductive coupling, which is considered by some to maximize operator safety and connector life [2–7]. A bridge inverter operating from a DC link created by the UPF rectifier impresses a high frequency AC signal on the primary of a relatively lightweight inductive coupling. Unity power factor operation is essential to ensure maximum power delivery for the fastest possible charging and to minimize the generation of harmonic currents. The voltage on the secondary side of the coupling is applied to the battery charging circuitry inside the vehicle. The inverter operates with a fixed frequency and duty cycle to maximize efficiency. To alter the charging current, the charging current controller modifies the DC-link voltage created at the output of the UPF rectifier. In our pro-

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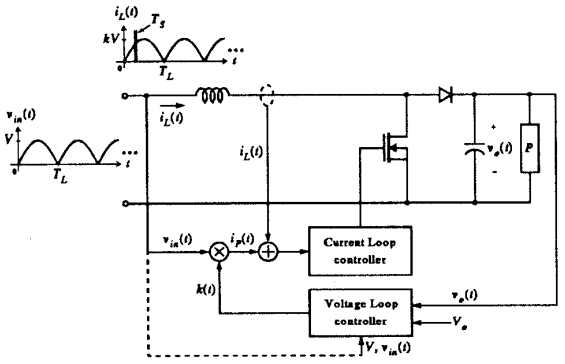

Figure 2: High power factor preregulator.

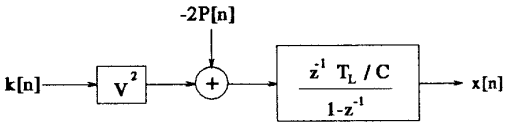

Figure 3: Boost converter sampled data model.

totype, a capacitively coupled transmitter relays information about the charging current to the charging station while maintaining safety isolation. (Note that this architecture is general in the sense that, even if an inductively coupled connector interface is not desired, safety isolation and ground fault protection are nearly always desired. That is, some high-frequency transformer with an inverter is likely to be part of the charger. The system shown in Fig. 1 could as easily be used with an ohmic connector by moving the entire charger into the vehicle.)

In contrast to UPF controllers for typical regulation applications, the charging system requires a controller whose stability is verifiably guaranteed over a wide range of operating conditions. Also, for adequate tracking performance, the controller may need to respond relatively swiftly to command changes or load disturbances over this range. This paper describes a multirate digital controller for battery charging that meets these demands.

II. Background

A boost converter as shown in Fig. 2 serves as the UPF rectifier in the battery charger. The input voltage is the rectified AC utility voltage. All voltage and current variables in Fig. 2 refer to quantities averaged over at least one switch period, i.e., switching ripple will be ignored in the following discussion. An inner current loop controls the input or inductor current $i_L(t)$ to follow a desired reference waveform $i_p(t)$ by providing an appropriate pulse width modulated switching sequence to the controllable switch. To ensure UPF operation, the reference waveform $i_p(t)$ is a scaled copy of the rectified input voltage waveform. An outer, voltage loop controller can adjust v_o to a desired value by varying the scale factor k used to compute $i_p(t)$. Changing k is tantamount to changing input power.

In [8] and [9], a large-signal linear, "power balance" model of the boost UPF rectifier was derived using Tellegen's theorem [10]. Assuming that the inner current loop works well, the inductor current waveform is presumed to be a scaled copy of the input voltage waveform, i.e., $i_L(t) = kv_{in}(t)$. Also, to ensure unity power factor operation, it is presumed that k and the load power, P, will vary no more frequently than once per rectified line cycle. With these assumptions, the following sampled data model of the boost rectifier may be developed:

$$x[n+1] = x[n] + \frac{T_L V^2}{C} k[n] - \frac{2T_L}{C} P[n], \qquad (1)$$

where the state variable $x[n]$ denotes the value of the *squared* output voltage at the beginning of the nth cycle. Similarly, $k[n]$ and $P[n]$ represent the value of the scale factor k and the load power, respectively, during the nth cycle. The variable T_L represents the period of one rectified input line cycle, i.e., $1/T_L = 120Hz$. The index n in the sampled data model, (1), increments once every T_L seconds. The sampled data, power balance model of the boost rectifier is illustrated schematically with the use of the z-transform [11] in Fig. 3.

Because this model is *not* a small-signal approximation, it is especially suitable for use in developing a controller for tracking applications like the battery charger. Because it is a sampled data model, it is a convenient starting point for developing a digital controller. We begin by developing a discrete time (DT) controller for the squared output voltage, since this is the state variable described by the power balance model. Charging current is controlled by a DT outer loop that computes the reference for the inner voltage loop. The total charging system consists of a multirate cascade of three nested control loops, listed from highest to lowest closed loop tracking bandwidth: an innermost current loop to control and shape the input current to the boost converter; a voltage loop to control the output bus voltage; and an outermost current control loop to track the desired output charging current profile. In our prototype, the inner current loop is implemented with analog hardware. The outer voltage and current loops are implemented on a digital microcontroller.

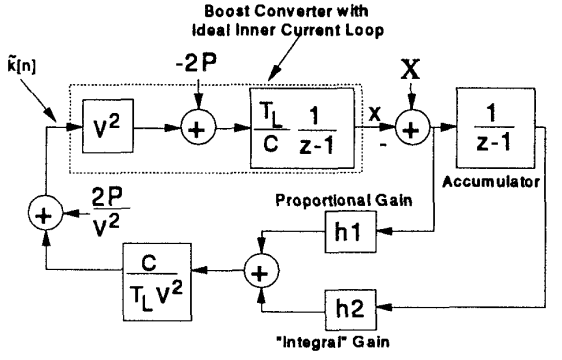

Figure 4: Voltage loop.

III. Voltage Control

In [9] and [10], the voltage loop is stabilized with the discrete time version of a *proportional-integral* (PI) compensator. A DT accumulator serves to "integrate" the squared output voltage error. A future accumulator state, $\sigma_v[n+1]$, is computed as the sum of the current accumulator state, $\sigma_v[n]$, and the output error,

$$\sigma_v[n+1] = \sigma_v[n] + (X[n] - x[n]), \qquad (2)$$

where $X[n]$ is the squared voltage reference and $(X[n] - x[n])$ is the error in the squared voltage at time n. In [9], the control command or scale factor k is computed as the sum of a term proportional to the output error and another term proportional to the accumulator state:

$$k[n] = \frac{C}{T_L V^2}(h_1(X[n] - x[n]) + h_2\sigma_v[n]) \qquad (3)$$

This choice of compensation results in a closed loop system whose dynamics are, unfortunately, dependent on the load power $P[n]$. We will see in the next section that the inability to guarantee the voltage loop dynamics independently of the load would significantly complicate the development of the outer charging current control loop. To make the voltage loop dynamics independent of load power, the control command in the charger prototype is computed as in (3), but with the addition of a feedfoward of the load power:

$$\tilde{k}[n] = \frac{C}{T_L V^2}(h_1(X[n] - x[n]) + h_2\sigma_v[n]) + \frac{2}{V^2}P[n] \quad (4)$$

In a charging circuit, both load terminal voltage and terminal current will be available, and computing load power requires little additional expense or computational effort. Substituting (4) into (1) yields a new second-order, large-signal linear model for the actively controlled boost converter:

$$\begin{bmatrix} \sigma_v[n+1] \\ x[n+1] \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ h_2 & (1-h_1) \end{bmatrix} \begin{bmatrix} \sigma_v[n] \\ x[n] \end{bmatrix} + \begin{bmatrix} 1 \\ h_1 \end{bmatrix} X[n] \qquad (5)$$

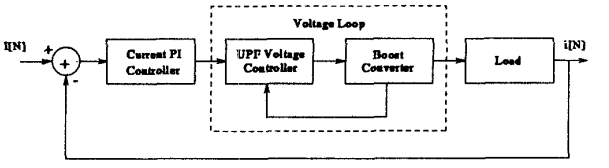

Figure 5: Closed loop current control.

The system poles are

$$z_1, z_2 = \frac{(2-h_1) \pm \sqrt{h_1^2 - 4h_2}}{2}. \qquad (6)$$

The complete system with the voltage loop closed is shown schematically in Fig. 4. Selecting gains h_1 and h_2 so that these poles have magnitude less than one results in a stable system. Once gains have been calculated to yield stable closed loop pole locations, the system will remain stable *for practically any load* because (5) is independent of load power. The stable voltage loop will converge to any reference given sufficient time. This guaranteed convergence substantially simplifies the construction of the charging current control loop.

IV. Charging Current Control

The outermost control loop in the battery charger ensures that the output charging current tracks a current reference. This loop creates a desired charging current by computing an appropriate voltage command reference for the voltage loop to follow. The complete system is illustrated schematically in Fig. 5. The dashed *voltage loop* box in Fig. 5 represents the boost converter and voltage loop control circuitry shown in Fig. 4.

The load dynamics are easily represented by a driving point admittance for a wide range of loads (e.g., battery types) in the charging current loop. Given the availability of a function relating applied terminal voltage to load current, a natural and convenient formulation for the current loop is to assume that load or charging current will be sensed, and a desired terminal voltage will be created by the action of the current loop computation and the voltage amplifier (boost converter and voltage loop). However, *squared* output voltage is the state variable controlled by the voltage loop. This complicates the formulation of a complete state space description for the full three-loop system.

The guaranteed convergence of the voltage loop, independent of load dynamics, facilitates simplifying assumptions. Recall that the DT voltage loop operates with sample step index n. The current loop will be designed to operate with sample index $N = Qn$ where Q is a positive integer. That is, every step of the DT current loop

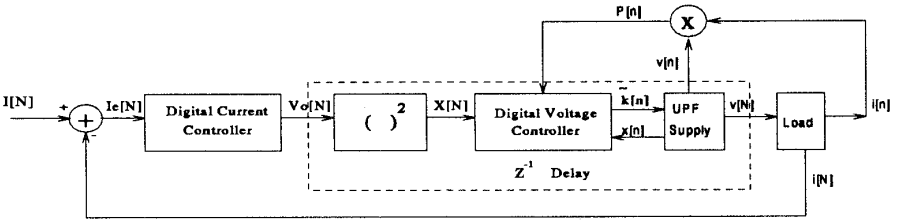

Figure 6: Current control system.

corresponds to Q steps of the voltage loop. This *multirate* arrangement makes it possible to model the voltage loop dynamics, from the standpoint of the outer current loop, in any of several simplified ways. Two approaches will be considered here: a delay model of the voltage loop appropriate for resistive loads, and a zero-order hold model appropriate for loads representable as combinations of linear, time invariant (LTI) circuit elements and independent sources.

Delay Model

One possibility, employed in our prototype with a resistive load, is to select Q and the closed loop pole locations of the voltage loop so that the output bus voltage will converge to a new reference X in a single step of the current loop index N. That is, the current loop computes a voltage reference at time N. This reference is squared and supplied as the command reference to the inner voltage loop. With the proper choice of Q and the voltage loop poles, the output bus voltage will have converged to the reference command supplied by the current loop by time $N+1$. Under these assumptions, the voltage loop may be modeled as a unit delay on the slow, current loop time scale. This arrangement is illustrated in Fig. 6. Signals in the figure are indexed by "n" or "N," depending on whether they are part of the fast voltage loop or slow current loop, respectively.

With a resistive load, and modeling the voltage loop as a unit delay on the time scale of the current loop, the charging current loop may be satisfactorily stabilized with a PI-type DT compensator. The current loop accumulator state variable σ_i is governed by the state equation

$$\sigma_i[N+1] = \sigma_i[N] + (I[N] - i[N]). \quad (7)$$

where I is the current reference and i is the actual output current. The reference voltage V_o is

$$V_o[N] = h_3(I[N] - i[N]) + h_4\sigma_i[N] \quad (8)$$

where h_3 and h_4 are the proportional and "integral" gains, respectively.

Modeling the action of the voltage loop as a unit delay on the time scale of the current loop, the output voltage applied to the load is equivalent to the delayed command signal, i.e.,

$$v_o[N+1] = V_o[N] = h_3(I[N] - i[N]) + h_4\sigma_i[N]. \quad (9)$$

With a resistive load, a state equation for i can be written using (9) and Ohm's law:

$$i[N+1] = \frac{h_3}{R}(I[N] - i[N]) + \frac{h_4}{R}\sigma_i[N]. \quad (10)$$

Equations (7) and (10) together describe the state dynamics of the charging current loop:

$$\begin{bmatrix} \sigma_i[N+1] \\ i[N+1] \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ \frac{h_4}{R} & \frac{-h_3}{R} \end{bmatrix} \begin{bmatrix} \sigma_i[N] \\ i[N] \end{bmatrix} + \begin{bmatrix} 1 \\ \frac{h_3}{R} \end{bmatrix} I[N]. \quad (11)$$

In the z plane, the closed loop system poles for the charging current loop are

$$z_1, z_2 = \frac{(1 - \frac{h_3}{R}) \pm \sqrt{(\frac{h_3}{R})^2 + \frac{2h_3}{R} + 1 - \frac{4h_4}{R}}}{2}. \quad (12)$$

The stability and transient characteristics of the current loop may be adjusted by selecting appropriate proportional and "integral" gains h_3 and h_4.

Zero-Order Hold Model

For a resistive load, load terminal voltage is proportionally related to load terminal current. This made it easy to step from (9) to (10) while developing the full state equations (11) for the current loop in the previous section. For a more complicated LTI load model, the delay model of the voltage loop may not be as easy to apply. In this case, we can exploit the guaranteed, large-signal transient characteristics of the voltage loop to develop other useful control models and approaches.

Once again, the DT current loop steps with index $N = Qn$ where n is the index of the voltage loop and Q is a positive integer. We now add the additional constraint

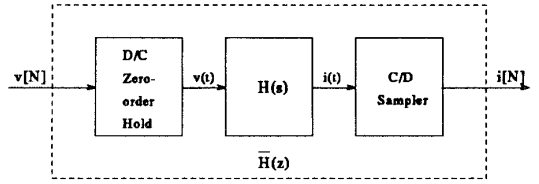

Figure 7: Driving point characteristic.

that the voltage loop, given a new reference, will drive the output voltage to this reference in *many fewer* than Q steps of the index n. This condition is ensured through judicious selection of Q and the closed-loop pole locations of the voltage loop. Given these conditions, the voltage loop may be modeled as a zero-order hold (ZOH) on the time scale of the outer current loop.

For an LTI load, the load terminal current can be related to the applied terminal voltage by an expression for the driving point admittance of the load, represented henceforth by the CT Laplace transform $H(s)$. [1] Assuming that Q steps of the index n are substantially longer than the time required for the voltage loop to settle to a new command reference, the CT voltage applied to the load will appear "pulse like" throughout one step of the index N, i.e., the operation of the voltage loop will closely approximate that of a zero-order hold. The current loop controller will provide a command reference to the voltage loop, and will also sample the load current, on each step of the current loop index N. Figure 7 schematically illustrates this arrangement. The zero-order hold block represents the boost converter with voltage loop.

The ZOH and sampling operations in Fig. 7 model the interface between the CT driving point characteristic of the load and the DT current loop [13]. The DT driving point admittance can be described as a z-transform $\overline{H}(z)$. The admittance $\overline{H}(z)$ is related to $H(s)$ by a *step-invariant transformation* [11].

Given $H(s)$, the DT transfer function $\overline{H}(z)$ may be computed as follows:

- Compute the step response of $H(s)$. That is, calculate the inverse Laplace transform of $\frac{H(s)}{s}$.
- Sample the resulting continuous-time step response $x(t)$ to obtain $x[N] = x(NT)$.
- Determine the z-transform of $x[N]$, denoted by $\overline{X}(z)$.

[1] Many loads of interest can be modeled as circuits consisting of LTI circuit elements, or as switched circuits that are piecewise LTI. Most batteries, on the other hand, tend to exhibit nonlinear driving point current/voltage characteristics. It is often possible, however, to develop LTI or piecewise LTI battery models; see [12] for example.

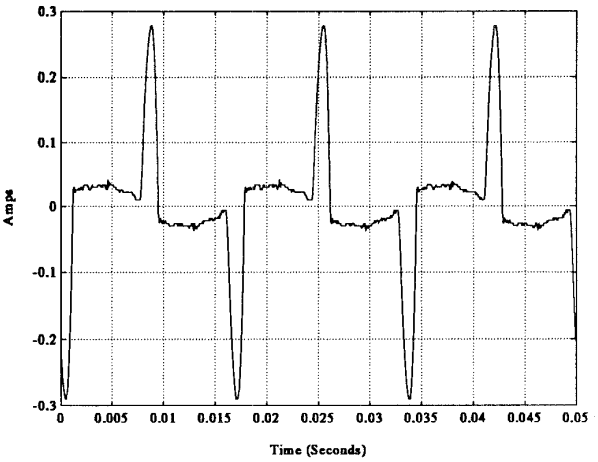

Figure 8: Uncorrected input current.

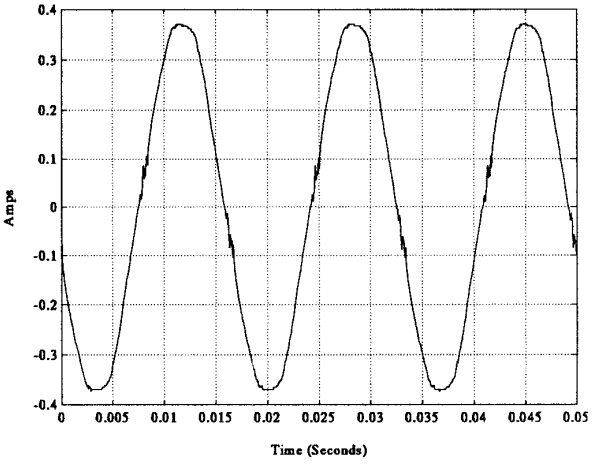

Figure 9: Corrected input current.

- The z-transform $\overline{X}(z)$ represents the step response of the DT transfer function $\overline{H}(z)$, i.e. $\frac{z\overline{H}(z)}{z-1}$. To find $\overline{H}(z)$, multiply $\overline{X}(z)$ by $\frac{z-1}{z}$.

Tables relating common functions $H(s)$ to their "pulse" transfer functions $\overline{H}(z)$ may be found in many texts (See [13], for example).

In general, complex load models will add state variables to the overall current loop state space description through the driving point admittance $\overline{H}(z)$. In such cases, the current loop state equations will generally be more complicated than those summarized in (11). Gains might have to be adapted and/or different compensation schemes might be needed for different loads. Fortunately, the digital implementation of the current loop controller accommodates these changes.

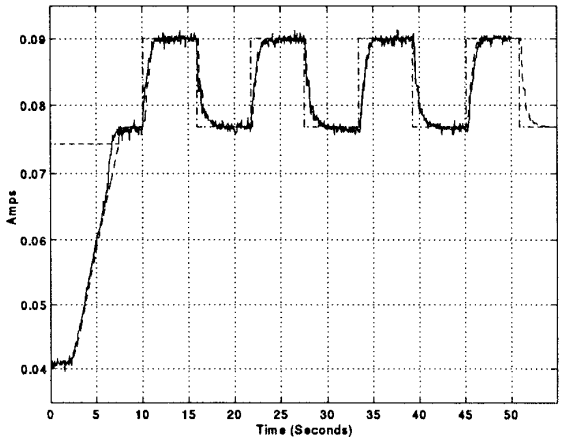

Figure 10: Step response: command, simulation and measured current.

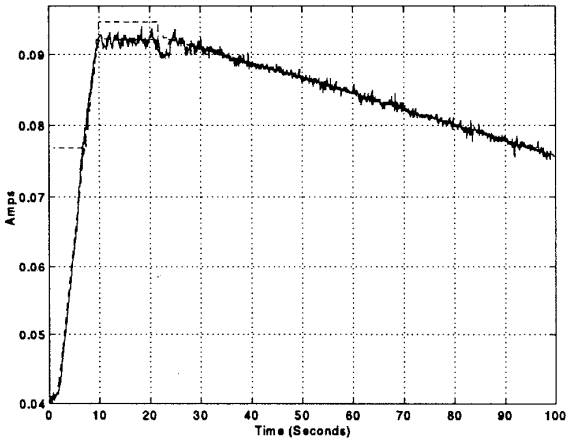

Figure 11: Ramp response: command, simulation and measured current.

The approach outlined in this section requires that the voltage loop converge to its reference in many fewer than Q steps of the index n. This limits the performance of the current loop. In principle, however, the voltage loop can be made *deadbeat* [10], i.e., the voltage loop can converge in two steps of the index n, or one electrical input line cycle. This, of course, is subject to the limitations imposed by the maximum current command that can be followed by the inner current loop, and by the discharge rate made possible by the loading conditions. Nevertheless, the achievable, practical performance appears to be more than adequate for high performance battery charging applications.

V. Experimental Results

The 250 W boost converter used in the prototype consisted of a $470\mu F$ capacitor, a $1mH$ inductor, a Motorola MUR 1560 diode, and an International Rectifier IRFP450 MOSFET. For these preliminary tests, the load was a $3.9K\Omega$ resistor. The inner current loop was implemented with part of a Unitrode UC3854 averaged current mode control chip [14]. Both the voltage and charging current controllers were implemented on a single Intel 80C196KC microcontroller (with plenty of spare processing power). Code for the microcontroller was developed in the C programming language using a cross-compiler from Intel [15].

The operation of the voltage loop controller was synchronized to the period of the rectified line, T_L, by a timer on the 80C196KC. For tests with the resistive load, the delay model of the voltage loop was used to develop the charging current controller. The charging current loop index N in the prototype increments once for every 50 steps of the voltage loop index n. Gain selection for the voltage and charging current loops is discussed in [16].

Figure 8 shows the steady-state *input* current to the full-wave rectifier that precedes the boost converter *before* any control action commences. Initially, all three control loops are inactive, and the controllable MOSFET in the boost converter is held in the off state. The input current exhibits the "spikey" shape that typically occurs when a sinusoidal voltage is recitified and used to charge a capacitor. When the output voltage stabilizes, the inner current loop is activated. The input current assumes the shape and phase of the input voltage waveform, indicating the proper functioning of the inner current loop. The 80C196KC performs a "soft start" by sending open loop scale factor commands to the inner current loop, causing the input current to rise gently until the output voltage/current is close to a desired initial operating point. At this time, the processor initializes the voltage and charging current loops in the microprocessor, and closed loop control of the output current begins. Figure 9 shows a steady-state input current level after the control loops have been activated.

Figures 10 and 11 show the output current during two different tests with the converter. Each figure shows a charging current command reference (dotted/dashed line), a simulation prediction of the converter performance (dashed line), and the experimental curve (solid line) from the actual hardware prototype. The simulations were conducted in MATLAB. They attempt to predict exactly the empirical responses by simulating the converter dynamics described by the power balance model, (1), under the control of the current and voltage loop controller software transcribed into MATLAB.

In Fig. 10, the current command reference is a pulsatile waveform. Following the open loop soft start during the first 7 seconds of operation, the output current agrees closely with the command reference, and precisely with the simulation prediction. In Fig. 11, the command ref-

erence is a brief plateau, followed by a decreasing ramp. The soft start dominates the first 7 seconds of the output current profile. When the current and voltage loop controllers engage after the soft start, the current closely follows both the command reference and the simulated prediction. From the 10 to 22 second mark, we have "lifted" the simulated prediction from the other traces to aid in seeing it. Otherwise, the prediction would be indistinguishable from the actual trace.

VI. Conclusions

The sample experiments reviewed in the previous section are representative of many similar laboratory tests. They indicate that the voltage loop controller with load power feedfoward as described in (4) operates as anticipated. The voltage loop dynamics can therefore be guaranteed with minor restrictions on load behavior, permitting us to approximate the voltage loop behavior in a number of different ways from the standpoint of the outer charging current loop. The experiments presented here directly demonstrate the performance of the charging current loop and its close agreement with predicted results.

The pole placements for the charging current and voltage loops in the prototype were not aggressive, i.e., the transient response could be improved, if necessary. We are working to test the performance of the controller with different, more challenging loads and load models. Also, we are engaged in studying the robustness of the multirate cascade controller in the face of load model errors or uncertainties, which may be of special concern in a field version of a battery charger, where significant deviations or drift in battery parameters may occur. The digital implementation of the charging current and voltage loops makes it easy to consider adaptive or scheduled control compensation for different loads in the field.

Acknowledgements

This research was funded by Amp, Incorporated. Additional funding was provided by MIT's Carl Richard Soderberg Career Development Chair. The authors gratefully acknowledge the valuable advice, support, and encouragement of Dr. Howard Peiffer, Joseph Sweeney, and Professor James L. Kirtley, Jr. Essential hardware for this project was made available through generous donations from the Intel Corporation and Tektronix.

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