A Power Factor Corrector with Bidirectional Power Transfer Capability

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Abstract—

This paper describes a high-power-factor electric utility interface that is capable of bidirectional power transfer, i.e., to or from the electric utility. Bidirectional power transfer capability is essential in many servomechanical and power electronic drive applications. The circuit presented here is capable of serving as a recitifer, an inverter, or as a stand-alone power supply (when operated with a battery as a load). It performs these functions with significantly enhanced efficiency and construction simplicity in comparison to conventional boost-type high power factor rectifiers.

I. Background

THIS paper describes the hardware design and operation of a 600-W bidirectional, high-power-factor utility interface. This system demonstrates capabilities and features not provided by conventional high-power factor interfaces. Experimental data from the prototype system will be presented and compared with predicted results.

The prototype interface is capable of bidirectional power flow to or from the input AC source, typically the electric utility. Bidirectional power flow expands the possible applications for the utility interface to a wide range of servomechanical and drive applications. With this interface, it becomes much easier to consider practical drives for complex loads, electromechanical devices, and battery chargers, all of which might operate most effectively with a drive that can source as well as sink power.

An electric-vehicle battery charger is one example application we are considering for the bidirectional interface [1]. Traditionally, power is transferred into a battery, raising its state of charge. Reversing this power flow makes it possible to discharge the battery, returning the power back to the utility or perhaps to an external load. It has been shown that, for certain battery technologies, the lifetime of a battery can be extended by properly discharging or "conditioning" before recharging [2], [3]. This conditioning may prove even more vital as new high-density battery chemistries are developed. A bidirectional charger could provide a safe and reliable "total charging solution."

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II. Converter Topology

The utility interface can be operated in three distinct modes. Forward power flow is possible in a boost mode, and reverse power flow is possible in a buck mode or an AC-inverter mode. A simplified schematic of the converter topology is shown in Fig. 1. The basic circuit, a modification of the unidirectional topology presented in [4], uses two half-bridge legs to form an H-bridge, which connects to the AC utility through an inductor L_1. The topology has several advantages over alternative designs, including: bidirectional power flow; elimination of the input full-bridge diode rectifier, reducing conduction losses (only two semiconductor drops in any conduction path as opposed to three in a conventional unity-power-factor (UPF) boost converter circuit); one high-frequency switching leg and one line-frequency switching leg; and an N-cell interleaved topology, shown in Fig. 2, that uses only $2N + 2$ active switches.

In order to accomplish bidirectional power flow, the conventional boost topology must be extended. A traditional approach is to replace the diode in the boost converter with a high-frequency switch. This switch is operated complementary to the controllable switch. An H-bridge of line-frequency switches replaces the full-bridge rectifier, thus enabling the unfolding of the waveform during reverse operation. In total, the number of **active** switches for a single-cell converter would increase from one to six.

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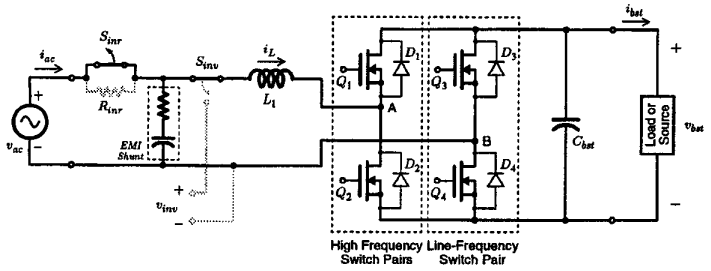

Fig. 1. Simplified schematic of the utility interface.

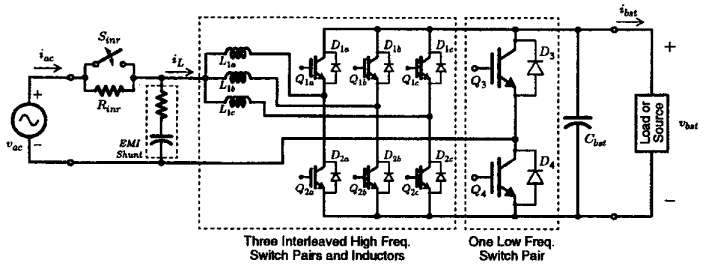

Fig. 2. Interleaved topology.

With only four active switches, the topology shown in Fig. 1 offers the same performance and better efficiency. The rectifier bridge at the input of a conventional topology has been removed entirely. The inductor L_1 instead connects directly to the AC source, and the unfolding operation is performed by two line-frequency switches Q_3 and Q_4. The resulting circuit has lower switching and conduction losses than its traditional counterpart. Since two of the four switches are operated at the line-frequency, their switching losses are negligible. Also, the current path from input to output has only two semiconductor drops. A conventional boost topology, unidirectional or bidirectional, has three. Conduction losses can be therefore reduced.

In addition, the topology in Fig. 1 can easily be extended to include multiple interleaved switching cells, as shown in Fig. 2. The interleaved topology requires that the waveshaping switches (Q_1 and Q_2) and the inductor L_1 are duplicated for each cell. The line-frequency "unfolding" switches Q_3 and Q_4 do not need to be duplicated. Therefore, the number of active switches for an N-cell interleaved converter is $2N + 2$, and the current through the $2N$ high-frequency switches is derated by a factor N.

A 600 watt single-cell prototype converter was built as shown in Fig. 1 and used to demonstrate the boost, buck, and AC-inverter conversion modes. The prototype operates at a switching frequency of 25 kHz with an inductor $L_1 = 2mH$. Complete circuit and control details are presented in [1]. The boost and buck switching modes are used to accomplish power transfer with near-unity power factor out of and in to, respectively, the AC utility. Because the voltages at the input and output of the converter are nearly identical for both the boost and buck modes of operation, the switching patterns are closely related. For example, the same inner-loop current controller is used to perform power-factor correction in both directions. The following sections illustrate the three operating modes of the prototype.

III. Boost Mode

In boost mode, the converter takes as input the AC voltage v_{ac} and converts it to a DC output voltage, v_{bst}. Ideally, the current i_{ac} is modulated to track the shape and phase of v_{ac} in order to achieve a unity power factor. Figure 3 illustrates typical boost-mode drive waveforms (with a very slow switch frequency, strictly for illustrative purposes). During the positive half-cycle of v_{ac}, MOSFET Q_4 is held on and Q_3 is held off. Consequently, node B is pulled low, effectively connecting the negative terminals of v_{bst} and v_{ac}. With Q_1 held off, Q_2 is switched at a constant frequency and a duty ratio $d(t)$. When Q_2 is on, the current i_L ramps up at a rate v_{ac}/L_1. When Q_2 is off, the current commutates to diode D_1 and ramps down at a rate $(v_{bst} - v_{ac})/L_1$. During the negative half-cycle of v_{ac}, the pattern is altered slightly to allow i_L to go negative. MOSFETs Q_3 and Q_4 are toggled, bringing node B up to v_{bst}. By reversing the roles of Q_1 and Q_2, the current i_L is identically controlled in the negative direction. This switch pattern ensures that L_1 always serves as a switch-frequency filtering impedance between the switches and the utility.

Figure 4 shows the experimental results measured from the system during forward, boost-mode operation with a switch frequency of 25 kHz. The waveforms demonstrate an experimental power factor of 0.997. The measured THD of the current waveform is 4.44 percent. The waveforms in the figure show the converter operating from 120 VAC supplied by an HP 6834B AC source/analyzer. The expanded region in Fig. 4(b) shows the current ripple measured before

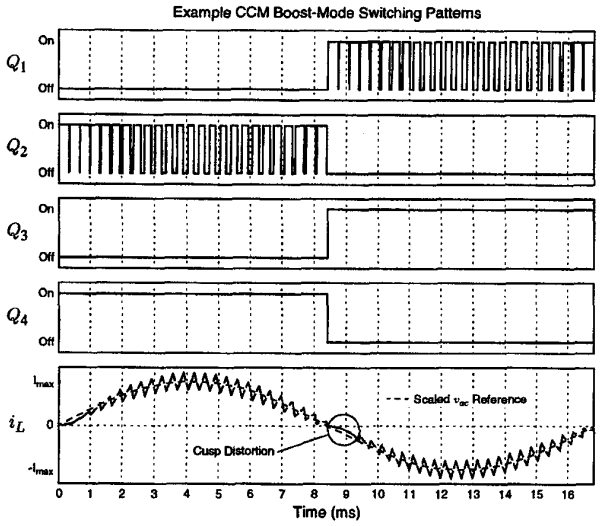

Fig. 3. Switch patterns for boost operation (power removed from the utility).

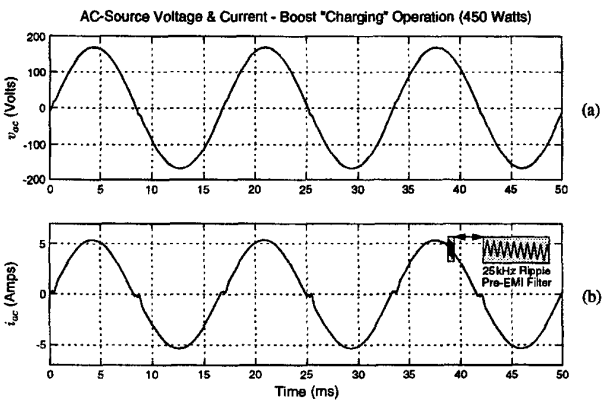

Fig. 4. Experimental input voltage and current, boost mode.

the EMI shunt filter. The filter effectively bypasses the 25-kHz ripple current so that it does not pass through to the utility. Figure 5 shows the magnitude of the input current harmonics with respect to IEC 555-2A limits.

IV. Buck Mode

The buck mode of the converter operates in a similar fashion, but the power flow is reversed to extract power from the load and return it to the utility. The waveforms in Fig. 6 illustrate the buck mode. During the positive half-cycle of v_{ac}, current is fed into the AC source. As with the boost mode, node B

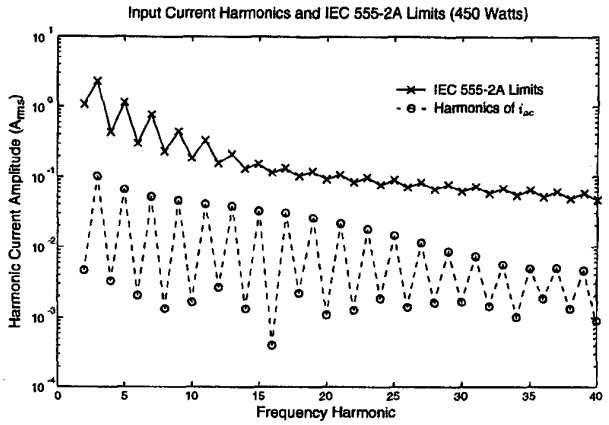

Fig. 5. Magnitude of the input current harmonics in comparison to IEC 555-2A limits.

is held low by MOSFET Q_4, but now switch Q_1 is modulated by a duty ratio $d(t)$. When Q_1 is on, the current i_L ramps in a negative direction with a slope $(v_{bst} - v_{ac})/L_1$. When Q_1 is off, the free-wheeling current is carried by diode D_2, and i_L ramps positive at a rate v_{ac}/L_1. During the negative half-cycle of v_{ac}, the pattern is reversed. MOSFETs Q_3 and Q_4 are toggled, and the roles of Q_1 and Q_2 are reversed.

Figure 7 shows the experimental results measured from the system during reverse, buck-mode operation. Notice that the current waveform is 180 degrees out of phase with the voltage waveform. This indicates negative power, meaning the converter is actually returning power from the load (batteries, in this case) to the AC utility. Approximately 210 W return to the utility with an experimental power factor of -0.996. The measured THD of the current waveform is 5.43 percent. Figure 8 shows the magnitude of the input current harmonics. As in boost mode, the converter operates in compliance with IEC 555-2A limits.

V. AC-Inverter Mode

The third mode of operation for the converter is the AC-inverter mode. The inverter mode could be used, for example, to power household AC equipment or supplement utility power during a short-term outage. In this configuration, illustrated in Fig. 9, power is extracted from the load, e.g., batteries, and used to create a synthesized 60-Hz AC waveform. The relay S_{inv} disconnects the existing AC utility and

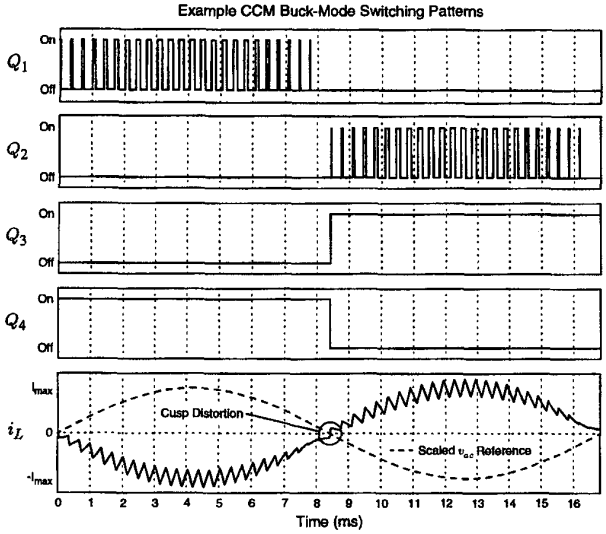

Fig. 6. Switch patterns for buck operation (power returned to the utility).

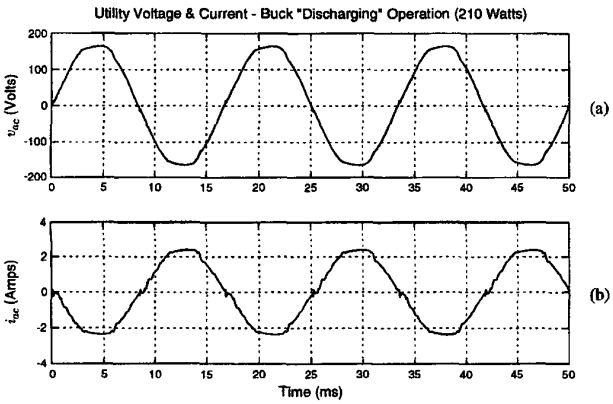

Fig. 7. Experimental utility voltage and current, buck mode.

routes the two half-bridge midpoints (nodes A and B) to the external AC load. The converter transfers power from the DC voltage at v_{bst} to the external load or loads connected across the v_{inv} terminals. The boost/buck inductor L_1 provides filtering, which helps to smooth the output waveforms. The MOSFET switches Q_1 through Q_4 are modulated to produce a tri-level voltage waveform measured between nodes A and B of the full-bridge. It is generally possible to synthesize the 60-Hz voltage waveform using an open-loop switching technique.

Several methods have been proposed to minimize the low-frequency harmonic content of PWM circuits

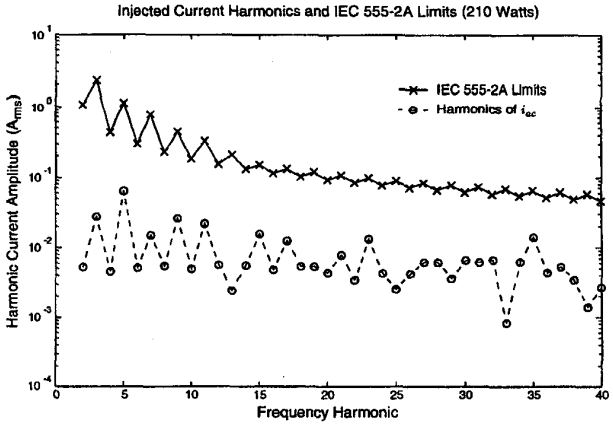

Fig. 8. Magnitude of the output current harmonics in comparison to IEC 555-2A limits.

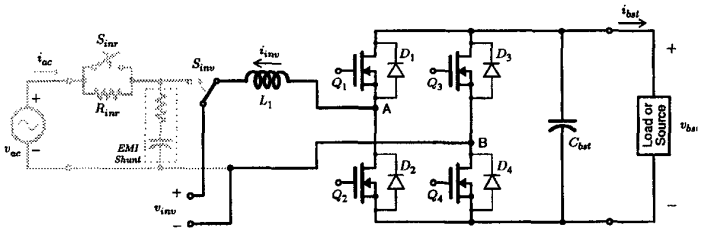

Fig. 9. Simplified schematic of the inverter topology.

[5]. More generally, switching sequences can be created with switch transitions that do not occur at a fixed frequency [6] – [8]. For example, a fixed-length sequence can be used to construct a discrete approximation to a reference sinewave. The number and position of the "ones" and "zeros" can be selected to minimize distortion without regard to the fixed-frequency constraints. It is possible to create low distortion sinewave approximations that use fewer switch transitions per cycle than a comparable PWM pattern. It is also possible to tailor or place the harmonic content of a switching sequence for a particular application. The bit patterns of the binary sequence can be stored in a memory and clocked out at a fixed rate, or generated in real time using a simple state machine or microcontroller.

To illustrate the use of programmed switching sequences in the inverter mode of the prototype, a sample 30-bit switch pattern is shown in Fig. 10. If this example pattern is used with the circuit shown in Fig. 9 to synthesize a 60-Hz sinusoid, then the bits are clocked out at a rate of 1800 Hz. The gate

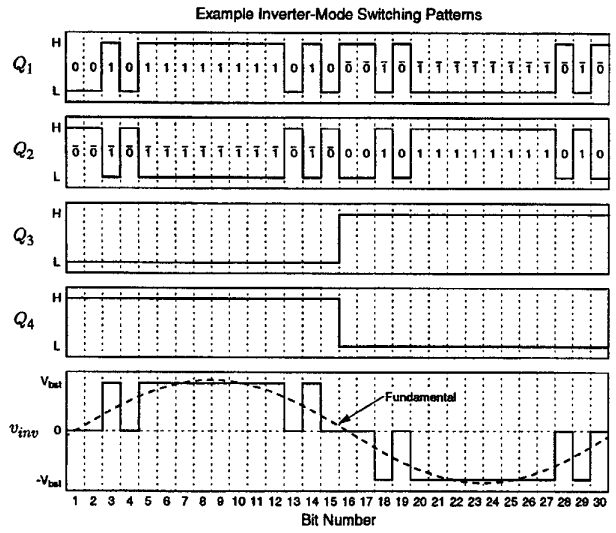

Fig. 10. Example 30-bit inverter switching sequence.

drives for MOSFETs Q_1 through Q_4 are related to the bit pattern as shown in the figure. Thus, very little additional logic is needed. The bottom trace in Fig. 10 shows the resulting tri-level waveform measured across nodes A and B. The voltage inversion during the second half-cycle is due to node B's transition from 0 to v_{bst} as Q_3 and Q_4 change state. The fundamental harmonic of this example waveform is a 60-Hz sinusoid with a peak amplitude approximately 6 % greater than v_{bst}. The fundamental is sketched with a dashed line in the figure.

The 30-bit waveform in Fig. 10 is special in that an amazing number of its higher-order harmonics are zero. Harmonic numbers 2, 3, 4, 5, 6, 8, 9, and 10 are all zero, and the seventh is only 12 % of the fundamental. In general, longer sequences will allow many more harmonics to be eliminated and thus lessen the filter requirements.

The simulated annealing algorithm described in [9] was used to produce a 1024-bit switching sequence for use with a circuit constructed for these experiments. The resulting switching sequence was coded into a PAL-based finite-state machine. This yielded a simple digital circuit that interfaced easily with the gate-drive signals for all four MOSFET switches in the inverter. Small, several hundred nano-second delays were built into the MOSFET gate-drive circuitry to prevent the possibility of shoot-through due to overlapping edges. The MOSFET switches Q1 through

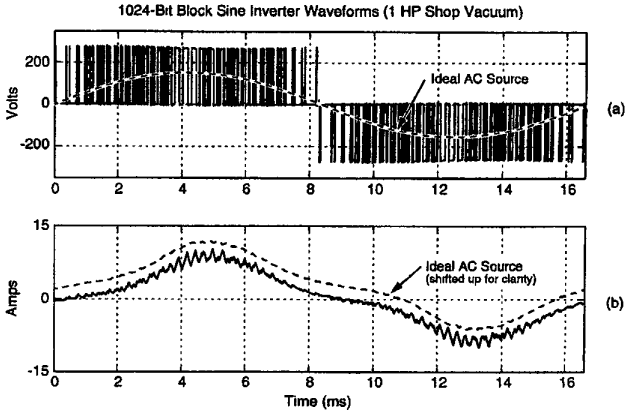

Fig. 11. Measured waveforms with the converter driving a 1 HP shop vacuum.

Q4 are modulated to produce a tri-level voltage waveform measured across the load.

The experimental output of the system is shown in Fig. 11. A 1-HP shop vacuum was used as a load for the experiment. The top axis in Fig. 11 shows the inverter output voltage measured across the load. The dashed line is the fundamental component of the voltage waveform. The lower axis shows the current drawn by the shop vacuum. The solid line is the current measured at the inverter output. The dashed line is the ideal current, which was generated using an HP 6834 AC source to provide a near perfect sinusoidal voltage.

A discrete-Fourier-transform (DFT) analysis of the experimental voltage waveform harmonics is provided in Fig. 12. The figure demonstrates the extremely low harmonic content of the 1024-bit switching pattern. The first 40 harmonics have an amplitude smaller than 1% of the fundamental, and the higher harmonics are well distributed. The THD of the unfiltered voltage waveform is approximately 113%. However, the small amount of filtering provided by the inverter inductor and the load inductance results in only about 10% distortion in the current from its ideal. A capacitor could be added to the filter circuit to provide second-order filtering. A second-order low-pass filter centered at 2 kHz would reduce the voltage THD to approximately 5%.

VI. Discussion

The bidirectional rectifier/inverter described in this paper provides unique advantages in a wide

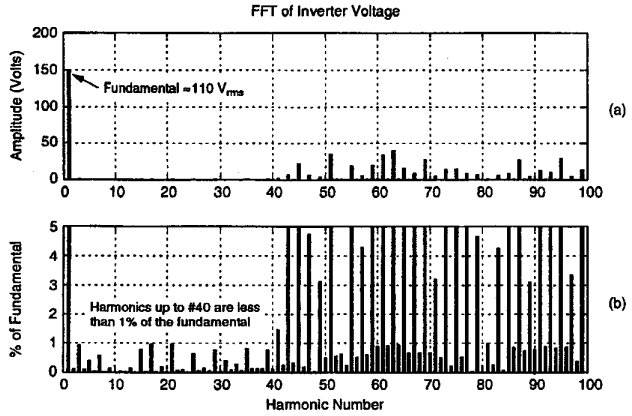

Fig. 12. Fourier transform of the inverter voltage. (a) FFT with amplitude in volts. (b) FFT showing harmonics as a percent of the fundamental. (Please note that the y-axis has been magnified.)

range of servomechanical and power electronic drive applications. We have employed this circuit, for example, for electric-vehicle battery charging. In this application, the load is a battery rack that can be charged from or discharged to the AC utility during recharging or conditioning operations.

The AC-inverter mode was discussed only in the context of generating open-loop voltage waveforms for AC loads. However, in servomechanical applications, all three operating modes of the circuit could be exploited with active control. For example, the circuit can be used to energize a motor from a battery load to provide motoring operation and regenerative braking. The battery in this system could also be charged or discharged from an AC utility or generator.

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