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Small-signal analysis of fully-differential closed-loop op-amp circuits with arbitrary external impedance elements

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Abstract: An analytical modelling approach for fully differential amplifiers is presented and validated through examples. Separation of the analysis into two steps coupled with linear superposition techniques leads to concise mathematical expressions. An added benefit of the two-step approach is that the usual symmetry assumptions are not needed. As a consequence, the results hold for arbitrary element values. The mathematical results are validated by comparison to SPICE simulations and experimental data.

1 Introduction

Fully differential (FD) amplifiers afford notable benefits in dynamic range and rejection of unwanted signals. The dynamic range benefit is significant when contending with low supply voltages in fully integrated and system-on-chip design [1–7], general purpose and audio frequency instrumentation [4, 8–10] and in discrete op-amp applications particularly for accommodating dynamic mode (DM) input analogue to digital converters [9–13]. Integrated switched capacitor amplifiers have exploited this benefit as well [14–17]. Power supply disturbances and common-mode (CM) pickup constitute typical unwanted signals that are better rejected by FD electronics when compared to their single-ended (SE) counterparts [8, 14, 18–21]. Both voltage-mode and current-mode (transimpedance) FD amplifiers are useful as front-end amplifiers for suppressing unwanted carrier content in balanced or 'bridge-like' systems [22–25]. Additionally, DM signal processing rejects the effects of even-order non-linearities [11, 20]. Both balanced and intentionally asymmetric FD amplifiers play important roles [10, 13].

These benefits come at the expense of added complexity in analysis. Powerful simplifications are possible upon assuming perfect or almost perfect symmetry, for example, equality between homologous elements, Z_{f1} and Z_{f2}, in Fig. 1. References [20, 26–28] exploit those simplifications to develop half-circuit decomposition methods. In [10] the author analyses FD amplifiers directly, but relies on perfect symmetry assumptions late in the analysis to arrive at expressions in terms of DM or CM input signals.

This work takes an alternative approach to the analysis of FD amplifiers. The analysis is separated into two steps corresponding to the inner transimpedance amplifier and the outer voltage-mode amplifier. Linear superposition of CM and DM signals assures that the results are written directly in terms of those quantities. Separation of the analysis and the use of linear superposition lead to concise or 'low-entropy' mathematical expressions [29]. An added benefit of the approach is that the usual symmetry assumptions are not needed and so the results hold for arbitrary element values.

The development of the FD transimpedance amplifier circuit model in Section 2 is perhaps the core contribution of this work. The versatility of that circuit model is demonstrated in three key contexts. First, the transimpedance amplifier model is used to derive the performance of a voltage amplifier with arbitrary impedance elements, Z_1 and Z_2 in Fig. 1. The results hold for arbitrary impedance values and agree well with the simulated behaviour of a commercial FD op-amp. Second, the extension of that analysis to include finite op-amp input impedance using the same transimpedance amplifier circuit model is described. Finally, the transimpedance amplifier model is used to predict the behaviour of a capacitive bridge sensor system. In the capacitive bridge sensor system, the external impedance elements Z_1 and Z_2 are further generalised to an arbitrary impedance network. Finite op-amp input impedance is captured by including shunt impedances at the transimpedance amplifier circuit model inputs. In the capacitive bridge sensor system, the front-end amplifier is loaded by the subsequent synchronous demodulation circuitry. Model validation comparing experimental data to data simulated using the transimpedance amplifier circuit model shows excellent agreement.

1.1 Current paths in FD amplifiers

The ensuing analysis will be better appreciated having an understanding of the CM and DM current paths through a FD amplifier. The current paths in the FD amplifier

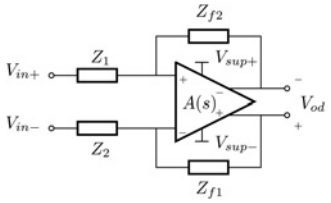

Fig. 1 *FD closed-loop op-amp circuit*

(Fig. 2*b*) are in some sense a generalisation of those in the SE amplifier (Fig. 2*a*); current return paths are supported by the output structure of the op-amp itself, but in the FD amplifier purely DM and purely CM currents take two distinct paths. The circuit models developed through the analysis in Sections 2 and 3 will mirror the current paths shown in Fig. 2*b*. Note that the incremental grounds in Fig. 2 are physically supported by the op-amp power supply connections. Incremental grounds are those potential surfaces exhibiting purely DC voltages with respect to the actual system ground.

1.2 Definitions

Definitions of CM and DM signal decompositions vary among the literature. We define them in this work as follows

$$v_{\mathrm{dm}} = v_+ - v_- \tag{1}$$

$$v_{\mathrm{cm}} = \frac{v_+ + v_-}{2} \tag{2}$$

$$i_{\mathrm{dm}} = \frac{i_+ - i_-}{2} \tag{3}$$

$$i_{\mathrm{cm}} = i_+ + i_- \tag{4}$$

1.3 Scope

The analysis in Sections 2 and 3 focuses on the DM output voltage while the CM output voltage is assumed to be held fixed by the CM feedback circuit included in all commercial FD op-amps. The scope of this paper is intended to address op-amp circuits that process signals having frequency content well below the op-amp cross-over frequency, for example, 1 kHz in the simulations of the LTC6404. These cases are ubiquitous as they are coincident with good design practices guaranteeing that the op-amp will exhibit large DM–DM gain, a_{d}, and relatively small CM–DM gain, a_{c}. Loading effects on the closed-loop op-amp circuit are negligible under these conditions because the feedback control significantly reduces the effect of finite-op-amp (open-loop) output impedance. The assumptions described above will be validated in both simulation and in a practical setting in Section 4.

1.4 Dynamics

The results in this paper are derived in terms of op-amp gain parameters, a_{d} and a_{c}, and generalised external impedance elements. The behaviour of an arbitrary system having dynamic effects may be described by inserting the frequency dependencies of those parameters into the mathematical results or circuit models.

1.5 Model validation

Comparison of the mathematical results with the simulated and experimental data validates the assumptions taken in the analysis, the practical relevance of this work and the correctness of the mathematical manipulations. Simulated model validation was carried out by comparing numerical results from the mathematical results to SPICE simulations of ideal circuit models and of a commercial FD op-amp, the LTC6404. The commercial LTC6404 FD op-amp part was chosen for the model validations because of the availability of a SPICE model for that part in the library provided with the simulation software used here, LTSPICE. The model validations plot the quantities of interest against percentage mismatch between homologous elements, e.g. ΔZ is the mismatch between Z_1 and Z_2 in Fig. 1. 0% mismatch corresponds to perfect symmetry. 200% mismatch means that one element is zero-valued while the other is twice the average value.

Experimental model validation was carried out by comparing simulated data to experimental data in a practical setting involving macroscopic capacitive occupancy sensing and a synchronous detection signal processing system. The commercial FD op-amp employed in that experimental setup was the Texas Instruments part, THS4140. While a SPICE model was not readily available for the THS4140 part, only the linearised circuit model developed in this paper was needed in the experimental model validation for

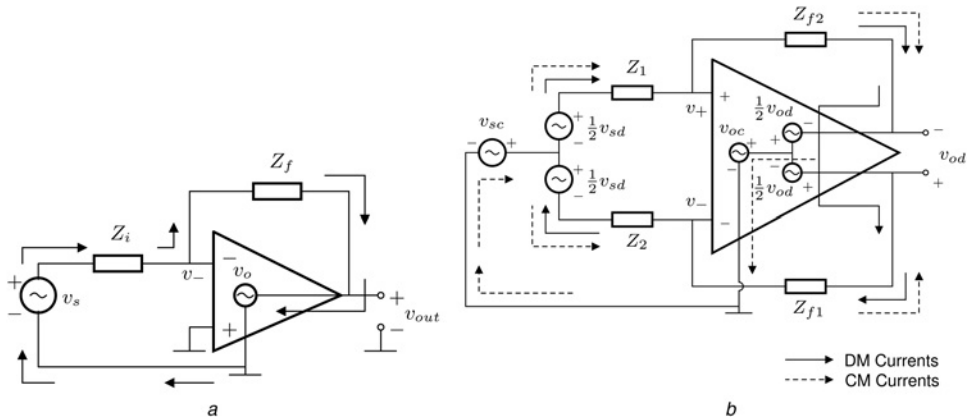

Fig. 2 *Small-signal current paths in closed-loop op-amp amplifiers*

a SE
b FD

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Section 4. The model parameters inserted into the linearised circuit model can be taken from the data sheet for that part, which was readily available.

2 Analysis step one: transimpedance amplifier

In this section we analyse a FD transimpedance amplifier using the small-signal model shown in Fig. 3. In the small-signal model, the input and output voltages are

$$v_{\mathrm{id}} = v_+ - v_- \tag{5}$$

$$v_{\mathrm{ic}} = \frac{1}{2}(v_+ + v_-) \tag{6}$$

$$v_{\mathrm{od}} = v_{o+} - v_{o-} \tag{7}$$

The DM and CM input currents are respectively

$$i_{\mathrm{id}} = i_{\mathrm{sd}} = \frac{1}{2}(i_+ - i_-) \tag{8}$$

$$i_{\mathrm{ic}} = i_{\mathrm{sc}} = i_+ + i_- \tag{9}$$

and the amplifier has the effects

$$v_{\mathrm{od}} = a_{\mathrm{d}} v_{\mathrm{id}} + a_{\mathrm{c}} v_{\mathrm{ic}} \tag{10}$$

$$v_{o+} = -v_{o-} \tag{11}$$

where a_{d}, the DM–DM op-amp gain, is large by design and a_{c}, the CM–DM op-amp gain, is relatively small, also by design. The small-signal CM output voltage is an incremental ground.

2.1 Transimpedance amplifier output behaviour

A CM–DM superposition approach for determining the transimpedance amplifier's DM output voltage is summarised by the equation

$$v_{\mathrm{od}} = i_{\mathrm{id}}\left(\frac{v_{\mathrm{od}}}{i_{\mathrm{id}}}\right)_{i_{\mathrm{ic}}=0} + i_{\mathrm{ic}}\left(\frac{v_{\mathrm{od}}}{i_{\mathrm{ic}}}\right)_{i_{\mathrm{id}}=0} \tag{12}$$

in which the terms in parentheses are the transimpedance and cross-transimpedance. To find $(v_{\mathrm{od}}/i_{\mathrm{id}})_{i_{\mathrm{ic}}=0}$, the CM input current sources are deactivated. Note that in this case

$$i_{\mathrm{id}} = i_{\mathrm{sd}} = i_+ = -i_- \tag{13}$$

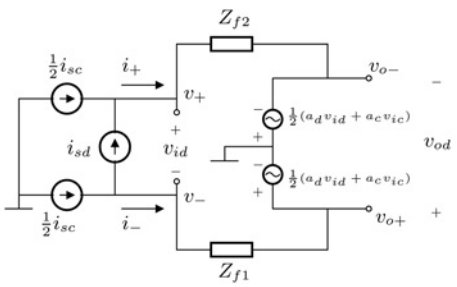

Fig. 3 *FD transimpedance amplifier small-signal model*

From Fig. 3, the resulting input terminal voltages are

$$v_+ = v_{o-} + i_{\mathrm{id}} Z_{f2} \tag{14}$$

$$v_- = v_{o+} - i_{\mathrm{id}} Z_{f1} \tag{15}$$

so that, from (5) and (6), the CM and DM input voltages become

$$v_{\mathrm{ic}} = \frac{1}{2}(v_+ + v_-) = \frac{i_{\mathrm{id}}}{2}(Z_{f2} - Z_{f1}) \tag{16}$$

$$v_{\mathrm{id}} = v_+ - v_- = -v_{\mathrm{od}} + i_{\mathrm{id}} Z_{f2} + i_{\mathrm{id}} Z_{f1} \tag{17}$$

Substituting the CM and DM input voltages into the output voltage from (10) yields

$$v_{\mathrm{od}} = a_{\mathrm{d}}(i_{\mathrm{id}}(Z_{f1} + Z_{f2}) - v_{\mathrm{od}}) + a_{\mathrm{c}}\frac{i_{\mathrm{id}}}{2}(Z_{f2} - Z_{f1}) \tag{18}$$

so that

$$\left(\frac{v_{\mathrm{od}}}{i_{\mathrm{id}}}\right)_{i_{\mathrm{ic}}=0} = 2\frac{a_{\mathrm{d}}}{1 + a_{\mathrm{d}}}\overline{Z_f} - \frac{a_{\mathrm{c}}}{2(1 + a_{\mathrm{d}})}\Delta Z_f \tag{19}$$

where we have made the following definitions

$$\overline{Z_f} \equiv \frac{(Z_{f1} + Z_{f2})}{2} \tag{20}$$

$$\Delta Z_f \equiv Z_{f1} - Z_{f2} \tag{21}$$

To calculate $(v_{\mathrm{od}}/i_{\mathrm{ic}})_{i_{\mathrm{id}}=0}$, the DM input current source is deactivated. A similar analysis yields

$$\left(\frac{v_{\mathrm{od}}}{i_{\mathrm{ic}}}\right)_{i_{\mathrm{id}}=0} = \frac{1}{2}\frac{(-a_{\mathrm{d}}\Delta Z_f + a_{\mathrm{c}}\overline{Z_f})}{(1 + a_{\mathrm{d}})} \tag{22}$$

Superposing the two responses in (19) and (22) yields the complete expression for the DM output voltage in response to generalised input currents

$$v_{\mathrm{od}} = i_{\mathrm{id}}\left(\frac{2a_{\mathrm{d}}\overline{Z_f} - (1/2)\,a_{\mathrm{c}}\Delta Z_f}{(1 + a_{\mathrm{d}})}\right) + i_{\mathrm{ic}}\left(\frac{a_{\mathrm{c}}\overline{Z_f} - a_{\mathrm{d}}\Delta Z_f}{2(1 + a_{\mathrm{d}})}\right) \tag{23}$$

2.2 Transimpedance amplifier input behaviour

Having derived the DM output voltage, a similar analysis leads to the DM and CM input voltages. These results will be grouped according to the superposition expressions below

$$v_{\mathrm{id}} = i_{\mathrm{id}}\left(\frac{v_{\mathrm{id}}}{i_{\mathrm{id}}}\right)_{i_{\mathrm{ic}}=0} + i_{\mathrm{ic}}\left(\frac{v_{\mathrm{id}}}{i_{\mathrm{ic}}}\right)_{i_{\mathrm{id}}=0} \tag{24}$$

$$v_{\mathrm{ic}} = i_{\mathrm{id}}\left(\frac{v_{\mathrm{ic}}}{i_{\mathrm{id}}}\right)_{i_{\mathrm{ic}}=0} + i_{\mathrm{ic}}\left(\frac{v_{\mathrm{ic}}}{i_{\mathrm{ic}}}\right)_{i_{\mathrm{id}}=0} \tag{25}$$

Analysing the small-signal model in Fig. 3 leads to

$$v_{\mathrm{ic}} = -i_{\mathrm{id}}\frac{\Delta Z_f}{2} + i_{\mathrm{ic}}\frac{\overline{Z_f}}{2} \tag{26}$$

and

$$v_{\mathrm{id}} = i_{\mathrm{id}}\left(\frac{2\overline{Z_f} + \frac{1}{2}a_{\mathrm{c}}\Delta Z_f}{(1+a_{\mathrm{d}})}\right) - i_{\mathrm{ic}}\left(\frac{\Delta Z_f + a_{\mathrm{c}}\overline{Z_f}}{2(1+a_{\mathrm{d}})}\right) \tag{27}$$

Comparing these results to (24) and (25) reveals the distinct terms resulting from the superposition of the CM and DM input sources. An interesting pattern arises in the results above. Terms with one of a_{c} or ΔZ_f influence cross-coupling from CM to DM signals. On the other hand, terms with a product of a_{c} and ΔZ_f appear as non-ideal terms in the relation between two DM signals. This pattern is intuitive and ubiquitous in this paper.

2.3 Circuit models of the transimpedance amplifier

For the second step of the analysis, it will be useful to form circuit models of the transimpedance amplifier. Figs. 4*b* and *c* show 'T' and 'Π' topologies that are helpful for representing the CM and DM input voltages in (26) and (27). Both models include a dependent voltage source at the output, which captures the function of the transimpedance and the cross-transimpedance from (23). The two models differ in their input structures. The T-network and the Π-network are each intended to approximate the behaviour of the CM and DM input voltages in (26) and (27).

To simplify the following discussion, it is convenient to rename the terms in (26) and (27) as follows

$$Z_{\mathrm{c}} \equiv \left(\frac{v_{\mathrm{ic}}}{i_{\mathrm{ic}}}\right)_{i_{\mathrm{id}}=0} = \left(\frac{\overline{Z_f}}{2}\right) \tag{28}$$

$$Z_{\mathrm{d}} \equiv \left(\frac{v_{\mathrm{id}}}{i_{\mathrm{id}}}\right)_{i_{\mathrm{ic}}=0} = \left(\frac{2\overline{Z_f} + (1/2)\Delta Z_f a_{\mathrm{c}}}{(1+a_{\mathrm{d}})}\right) \tag{29}$$

$$e_{\mathrm{c}}(i_{\mathrm{id}}) \equiv i_{\mathrm{id}}\left(\frac{v_{\mathrm{ic}}}{i_{\mathrm{id}}}\right)_{i_{\mathrm{ic}}=0} = -i_{\mathrm{id}}\left(\frac{\Delta Z_f}{2}\right) \tag{30}$$

$$e_{\mathrm{d}}(i_{\mathrm{ic}}) \equiv i_{\mathrm{ic}}\left(\frac{v_{\mathrm{id}}}{i_{\mathrm{ic}}}\right)_{i_{\mathrm{id}}=0} = -i_{\mathrm{ic}}\left(\frac{\Delta Z_f + a_{\mathrm{c}}\overline{Z_f}}{2(1+a_{\mathrm{d}})}\right) \tag{31}$$

The terms Z_{c} and Z_{d} are the diagonal-terms from (26) and (27) and they are the CM and DM input impedances of the transimpedance amplifier. The terms $e_{\mathrm{c}}(i_{\mathrm{id}})$ and $e_{\mathrm{d}}(i_{\mathrm{ic}})$ represent dependent voltage sources that capture the effects of the 'cross-terms' in (26) and (27).

Using the definitions in (28)–(31), the following model parameters achieve an exact match between the terminal behaviours of the circuits in Figs. 4*b* and *c* and the input voltages represented by (26) and (27)

T-Model:	Π-Model:	
$Z_\alpha = Z_{\mathrm{d}}$	$Z_\gamma = Z_{\mathrm{d}}\dfrac{Z_{\mathrm{d}}}{Z_{\mathrm{d}}\|\|4Z_{\mathrm{c}}}$	(32)
$Z_\beta = Z_{\mathrm{c}}$	$Z_\delta = Z_{\mathrm{c}}$	(33)
$e_\alpha = e_{\mathrm{d}}(i_{\mathrm{ic}})$	$e_\gamma = e_{\mathrm{d}}(i_{\mathrm{ic}})\dfrac{Z_{\mathrm{d}}}{Z_{\mathrm{d}}\|\|4Z_{\mathrm{c}}}$	(34)
$e_\beta = e_{\mathrm{c}}(i_{\mathrm{id}}) - \dfrac{i_{\mathrm{ic}}Z_{\mathrm{d}}}{4}$	$e_\delta = e_{\mathrm{c}}(i_{\mathrm{id}})$	(35)

The model parameters in (32)–(35) can be simplified under practical approximations to make the circuit models more intuitive. For sufficiently small Z_{d}, the additive term, ($i_{\mathrm{ic}}Z_{\mathrm{d}}$/

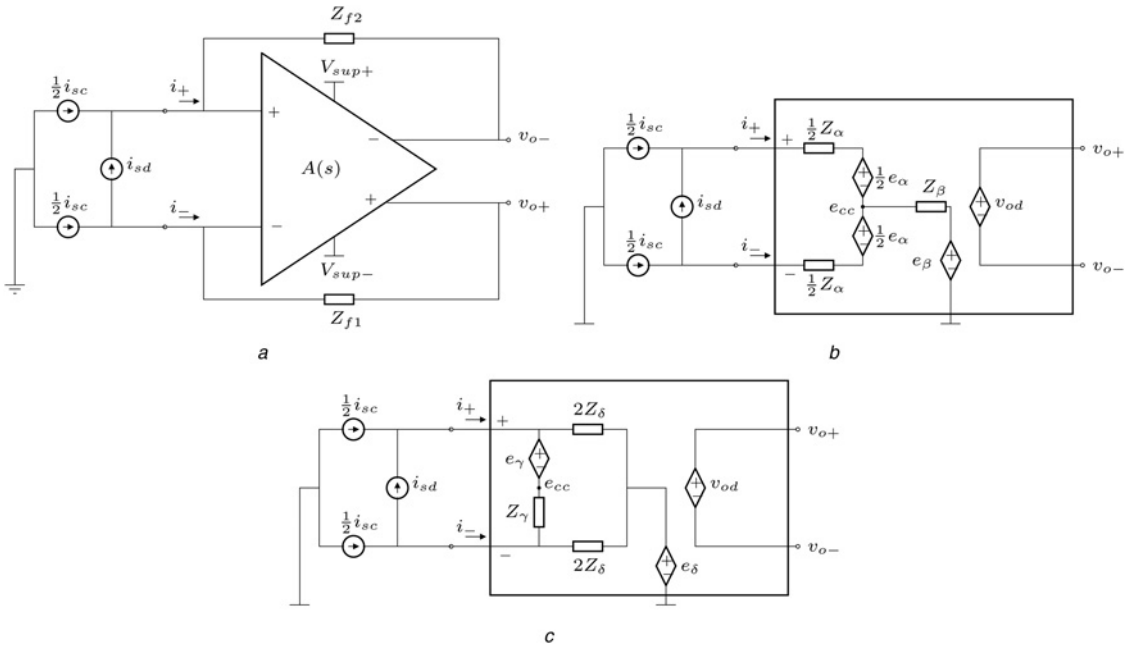

Fig. 4 *FD transimpedance amplifier and two approximate small-signal models*

a FD transimpedance amplifier
b Small-signal T-model
c Small-signal Π-model
T-model and the Π-model differ in the structure of their input network. Each contain an internal node labelled e_{cc}

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4), will approach zero and the multiplicative term, $(Z_d/Z_d\|4Z_c)$, will approach unity. From (28)–(31), Z_d is guaranteed to be small if both a_d and the ratio a_d/a_c are large. Under these assumptions, the model parameters in (32)–(35) reduce to

T-Model: Π-Model:

$$Z_\alpha = Z_d \quad Z_\gamma = Z_d \tag{36}$$

$$Z_\beta = Z_c \quad Z_\delta = Z_c \tag{37}$$

$$e_\alpha = e_d(i_{ic}) \quad e_\gamma = e_d(i_{ic}) \tag{38}$$

$$e_\beta = e_c(i_{id}) \quad e_\delta = e_c(i_{id}) \tag{39}$$

For simplicity, the rest of this analysis assumes that the gain criteria above have been met and proceeds with the approximate model parameters in (36)–(39).

2.4 Transimpedance amplifier model validation

Fig. 5 shows model validation plots for the transimpedance amplifier. In the model validations, the amplifier was driven with a 1 kHz sinusoidal current source with equal CM and DM components each having an amplitude of 1 mA. The calculated results for v_{id}, v_{ic} and v_{od} were overlayed on the simulated results for the T and Π circuit models, a small-signal ('$s-s$') op-amp model and a simulated commercial op-amp. The left column in Fig. 5 shows results for positive-valued mismatches, ΔZ_f. The right column shows results for negative-valued mismatches. The results in Fig. 5 show good agreement among the calculated and simulated results.

2.5 Virtual short-circuit approximation

From (29), the impedance of the DM virtual short-circuit is predominantly $2\overline{Z_f}/(1+a_d)$. The DM gain, a_d, is large by design, so this impedance is small and hence the virtual short-circuit approximation. On the other hand, the CM input impedance in (28) is half the average feedback impedance – approximately equal to $Z_{f1}\|Z_{f2}$ for small mismatch values. These results become intuitive when following the respective current paths (Fig. 2*b*) through the amplifier.

3 Analysis step two: voltage amplifier

In Fig. 6, input elements Z_1 and Z_2 are added onto the Π-model of the transimpedance amplifier circuit model to form a voltage amplifier model. The goal of this section is to find the DM output voltage, v_{od}, that results from the CM and DM input voltages, v_{sc} and v_{sd}. The transimpedances derived in Section 2 reveal the relationships between the input currents, i_{ic} and i_{id}, and the DM output voltage, v_{od}, from (23). The voltage amplifier analysis reduces to finding the relationships between the input voltage sources, v_{sc} and v_{sd}, and the input currents, i_{ic} and i_{id}. This analysis results in four transconductances.

A superposition approach to find the overall DM output voltage yields the following expression

$$v_{od} = i_{id}\left(\frac{v_{od}}{i_{id}}\right)_{i_{ic}=0} + i_{ic}\left(\frac{v_{od}}{i_{ic}}\right)_{i_{id}=0} \tag{40}$$

where the terms in parentheses are the two transimpedances from Section 2. The currents, i_{id} and i_{ic} in (40), may be found using linear superposition of the DM and CM input voltage sources as follows

$$v_{od} = \underbrace{\left(v_{sd}\left(\frac{i_{id}}{v_{sd}}\right)_{v_{sc}=0} + v_{sc}\left(\frac{i_{id}}{v_{sc}}\right)_{v_{sd}=0}\right)}_{i_{id}} \underbrace{\left(\frac{v_{od}}{i_{id}}\right)_{i_{ic}=0}}_{\text{transimpedance}} \tag{41}$$

$$+ \underbrace{\left(v_{sd}\left(\frac{i_{ic}}{v_{sd}}\right)_{v_{sc}=0} + v_{sc}\left(\frac{i_{ic}}{v_{sc}}\right)_{v_{sd}=0}\right)}_{i_{ic}} \underbrace{\left(\frac{v_{od}}{i_{ic}}\right)_{i_{id}=0}}_{\text{cross}-\text{transimpedance}} \tag{42}$$

where the added terms in parentheses are the four transconductances. The two transimpedances and four transconductances can be renamed for brevity as follows

$$Z_{dd} \equiv \left(\frac{v_{od}}{i_{id}}\right)_{i_{ic}=0} \quad Z_{cd} \equiv \left(\frac{v_{od}}{i_{ic}}\right)_{i_{id}=0} \tag{43}$$

$$Y_{dd} \equiv \left(\frac{i_{id}}{v_{sd}}\right)_{v_{sc}=0} \quad Y_{cd} \equiv \left(\frac{i_{id}}{v_{sc}}\right)_{v_{sd}=0} \tag{44}$$

$$Y_{dc} \equiv \left(\frac{i_{ic}}{v_{sd}}\right)_{v_{sc}=0} \quad Y_{cc} \equiv \left(\frac{i_{ic}}{v_{sc}}\right)_{v_{sd}=0} \tag{45}$$

so the expression in (42) can be written as

$$v_{od} = (v_{sd}Y_{dd} + v_{sc}Y_{cd})Z_{dd} + (v_{sd}Y_{dc} + v_{sc}Y_{cc})Z_{cd} \tag{46}$$

and regrouped with the source terms

$$v_{od} = v_{sd}(Y_{dd}Z_{dd} + Y_{dc}Z_{cd}) + v_{sc}(Y_{cd}Z_{dd} + Y_{cc}Z_{cd}) \tag{47}$$

The analysis may be simplified using the virtual short-circuit approximation quantified in Section 2.5. Analysis of the resulting circuit in Fig. 6*c* may be divided into four distinct pieces for the four unknown transconductances needed in the expression for v_{od} (47). Shorting the DM input source results in the set of constraints on the input currents

$$i_+ = \frac{(v_{sc} - e_{cc})}{Z_1} \tag{48}$$

$$i_- = \frac{(v_{sc} - e_{cc})}{Z_2} \tag{49}$$

while shorting the CM input source results in the set of constraints on the input currents

$$i_+ = \frac{((1/2)v_{sd} - e_{cc})}{Z_1} \tag{50}$$

$$i_- = \frac{(-(1/2)v_{sd} - e_{cc})}{Z_2} \tag{51}$$

In either case, the node voltage e_{cc} in Fig. 6*c* is constrained to be

$$e_{cc} = e_c + (i_+ + i_-)Z_c \tag{52}$$

Solving for $i_{id} = (i_+ - i_-)/2$ and $i_{ic} = (i_+ - i_-)$ leads to four permutations of constraints corresponding to the four transconductances. For instance, to find Y_{dd}, the CM input voltage is deactivated according to the definition in (44), and

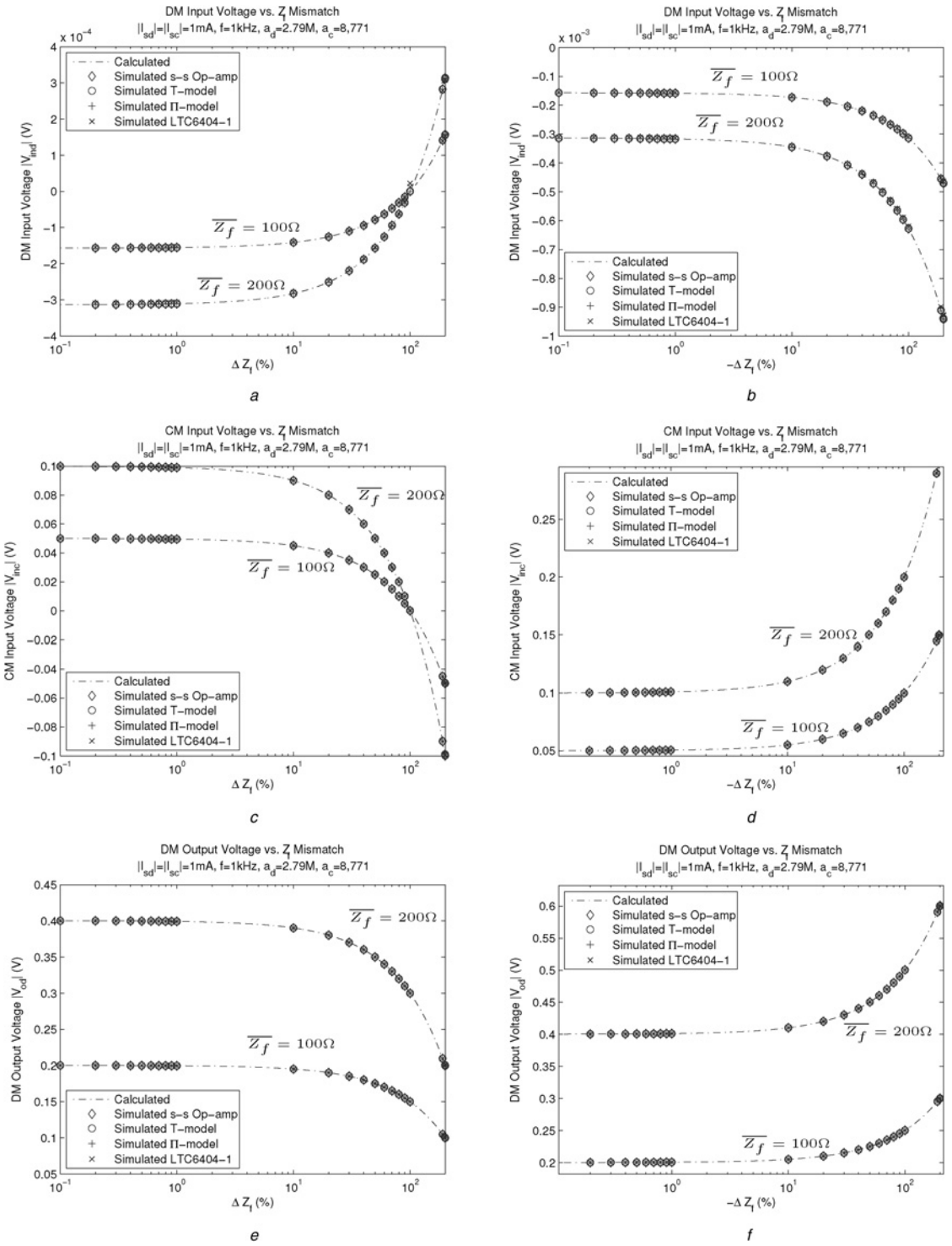

Fig. 5 *Validating the transimpedance amplifier model*

a v_{id} for $\Delta Z_f > 0$
b v_{id} for $\Delta Z_f < 0$
c v_{ic} for $\Delta Z_f > 0$
d v_{ic} for $\Delta Z_f < 0$
e v_{od} for $\Delta Z_f > 0$
f v_{od} for $\Delta Z_f < 0$

the DM input current is found from

$$i_{id} = \frac{i_+ - i_-}{2} \tag{53}$$

with the three constraints from KVL above, (50), (51) and (52). Solving for i_{id}/v_{sd} and simplifying leads to [30]

$$Y_{dd} = \frac{2\overline{Z_f} + Z_1 + Z_2}{4(Z_1||Z_2 + (1/2)\overline{Z_f})(Z_1 + Z_2) + \Delta Z \Delta Z_f} \tag{54}$$

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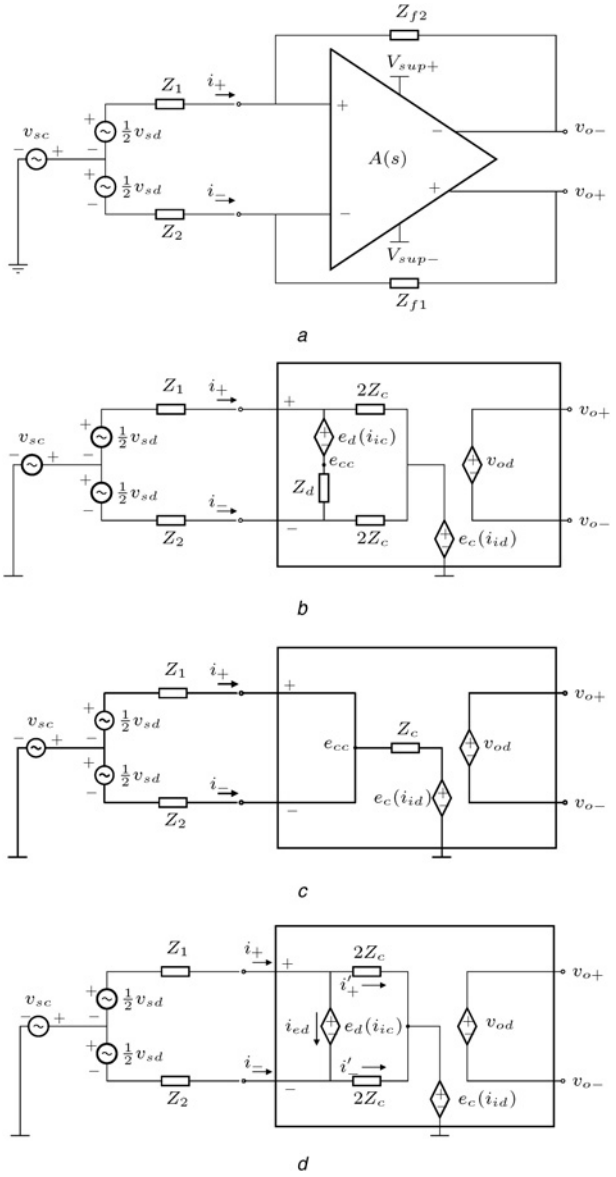

Fig. 6 *Adding the input elements onto the transimpedance amplifier model yields a voltage-mode amplifier model*

a FD voltage-mode amplifier
b Voltage-mode amplifier model built from the Π-model of the transimpedance amplifier
c Voltage-mode amplifier model using the 'virtual short-circuit approximation'
d The model used for deriving the correction in Section 3.1

The denominator in Y_{dd} above appears in all four transconductances. The quantities in that denominator can be identified with respect to physical current paths in the voltage amplifier as follows

$$Z_{dm} = Z_1 + Z_2 \tag{55}$$

$$Z_{cm} = Z_1 || Z_2 + \frac{\overline{Z_f}}{2} \tag{56}$$

For the simplified model of Fig. 6*c*, Z_{dm} is the impedance seen by a purely DM input voltage source driving a purely DM input current and Z_{cm} is the impedance seen by a purely CM input voltage source driving a purely CM input current. That is

$$Z_{dm} = \left(\frac{v_{sd}}{i_{id}}\right)_{\substack{v_{sc}=0 \\ i_{ic}=0}} \tag{57}$$

$$Z_{cm} = \left(\frac{v_{sc}}{i_{ic}}\right)_{\substack{v_{sd}=0 \\ i_{id}=0}} \tag{58}$$

Applying the constraints in the four permutations, simplifying and identifying the impedance terms Z_{dm} and Z_{cm} leads to

$$Y_{dd} = 2\frac{\overline{Z_f} + \overline{Z}}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \tag{59}$$

$$Y_{cd} = 2\frac{-\Delta Z}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \tag{60}$$

$$Y_{dc} = 2\frac{\Delta Z_f - \Delta Z}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \tag{61}$$

$$Y_{cc} = 8\frac{\overline{Z}}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \tag{62}$$

The common denominator in these transconductances aids further analysis when we form linear combinations of these terms (see Section 3.3).

3.1 Model correction

The virtual short-circuit approximation led to some inaccuracy in the results for CM–DM gain, A_{vc}, in the small-mismatch region (Fig. 7*a*). The modularity of the results allows for rapid correction of this inaccuracy. Adding the effect of $e_d(i_{ic})$ is most critical for correcting A_{vc} because it accounts for a DM input voltage in response to a CM input current. Among the two transconductaces that affect CM–DM gain, Y_{cd} quantifies the DM input current, which is most directly affected by the addition of $e_d(i_{ic})$ to the model. This correction re-derives Y_{cd} from the circuit in Fig. 6*d*, while Y_{cc} is assumed sufficiently accurate.

The circuit in Fig. 6*d* leads to the following constraints

$$i_{id} = i_{ed} + \frac{e_d}{4Z_c} = i_{ed} + i'_{id} \tag{63}$$

$$i_{ic} = i_+ + i_- = i'_{ic} \tag{64}$$

where

$$i'_{id} \equiv \frac{1}{2}(i'_+ - i'_-) \tag{65}$$

$$i'_{ic} \equiv i'_+ + i'_- = i_{ic} \tag{66}$$

and the current through the added DM voltage element is

$$i_{ed} = i_+ - i'_+ = i'_- - i_- \tag{67}$$

Finally, applying KVL results in two equations

$$v_{sc} - i_+ Z_1 - e_d - i'_- 2Z_c - e_c = 0 \tag{68}$$

$$v_{sc} - i_- Z_2 + e_d - i'_+ 2Z_c - e_c = 0 \tag{69}$$

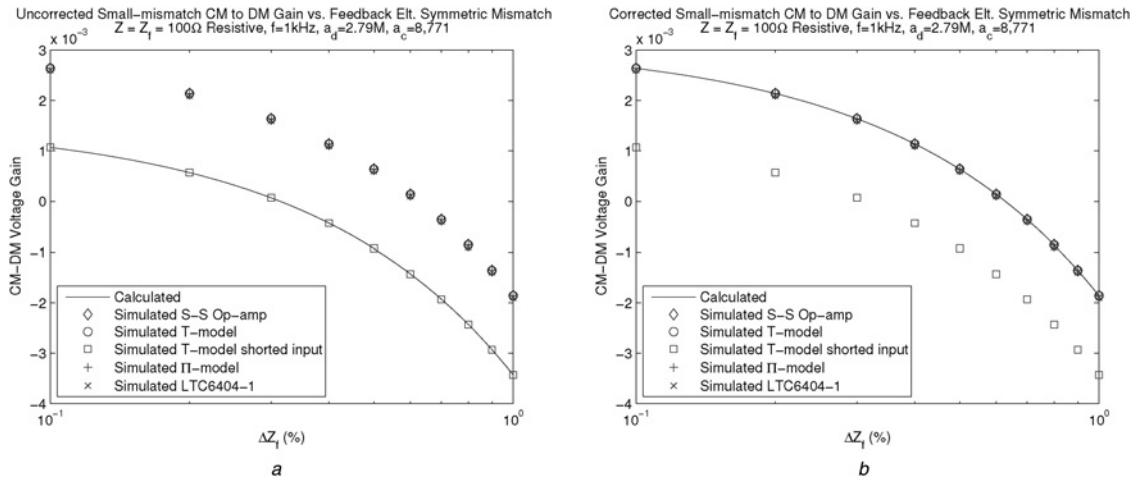

Fig. 7 *Accuracy improvement for small-mismatch A_{vc}*

a Small-mismatch 'zoom-in' of A_{vc} for $\Delta Z_f > 0$ (uncorrected). Plotting A_{vc} for $\Delta Z > 0$ results in a very similar plot. The calculated line falls on the shorted-input model data instead of the more accurate simulated data

b Small-mismatch 'zoom-in' of A_{vc} for $\Delta Z_f > 0$ (corrected). A plot of A_{vc} for $\Delta Z > 0$ is very similar. Small-mismatch CM–DM gain agrees well with simulated circuits after the correction is added

Solving these constraints for the 'corrected transconductance', $Y'_{cd} = (i_{id}/v_{sc})_{v_{sd}=0}$, leads to

$$Y'_{cd} = \frac{Y_{cc}(\overline{Z_f}\Delta Z + \overline{Z}(\Delta Z_f + a_c\overline{Z_f}/1 + a_d)) - \Delta Z}{4Z_1Z_2 + (1/2)\Delta Z_f \Delta Z} \quad (70)$$

which is more complicated than the expressions in (59)–(62). Because the small-mismatch region is of interest here, Y'_{cd} can be simplified with the small-mismatch approximations

$$\Delta Z_f \ll Z_{f1}, Z_{f2}, \overline{Z_f} \quad (71)$$

$$\Delta Z \ll Z_1, Z_2, \overline{Z} \quad (72)$$

which imply that $Z_{f1} \simeq Z_{f2} \simeq \overline{Z_f}$ and $Z_1 \simeq Z_2 \simeq \overline{Z}$. The 'small-mismatch corrected transconductance' becomes

$$Y'_{cds} \simeq \frac{(a_c\overline{Z_f}/1 + a_d) - \Delta Z}{2Z_{dm}Z_{cm}} \quad (73)$$

The denominator in (73) can be forced to match the common denominator from the other three transconductances by multiplying the numerator and denominator by 2 and adding the small quantity, $\Delta Z_f \Delta Z$, back in

$$Y'_{cds} \simeq 2\frac{\overbrace{\overline{Z_f}(a_c/1 + a_d)}^{\text{correction term}} - \Delta Z}{4Z_{dm}Z_{cm} + \Delta Z_f \Delta Z} \quad (74)$$

Comparing Y'_{cds} from (74) to Y_{cd} from (60) reveals that they differ only in the 'correction term' $(\overline{Z_f}(a_c/1 + a_d))$.

Model validation (Fig. 7*b*) with this corrected Y'_{cds} shows good agreement for small mismatch values. Although Y'_{cds} was calculated while assuming small mismatches, model validations will show that the full model, including the corrected Y'_{cds}, agrees for the range 0–200% of resistive element mismatch values. Therefore the following results, including Y'_{cds}, are proposed as the full transconductance–transimpedance descriptive abstraction of the FD voltage amplifier

$$Y_{dd} = 2\frac{\overline{Z_f} + \overline{Z}}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \quad (75)$$

$$Y'_{cds} = 2\frac{\overline{Z_f}(a_c/1 + a_d) - \Delta Z}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \quad (76)$$

$$Y_{dc} = 2\frac{\Delta Z_f - \Delta Z}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \quad (77)$$

$$Y_{cc} = 8\frac{\overline{Z}}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \quad (78)$$

and the transimpedance amplifier results are repeated here for convenience

$$Z_{dd} = 2\frac{a_d\overline{Z_f} - a_c\Delta Z_f/2}{(1 + a_d)} \quad (79)$$

$$Z_{cd} = \frac{1}{2}\frac{a_c\overline{Z_f} - a_d\Delta Z_f}{(1 + a_d)} \quad (80)$$

The results in (75)–(80) yield the full expression for the DM output voltage when substituted into the following expression

$$v_{od} = v_{sd}(Y_{dd}Z_{dd} + Y_{dc}Z_{cd}) + v_{sc}(Y'_{cds}Z_{dd} + Y_{cc}Z_{cd}) \quad (81)$$

3.2 Voltage amplifier input impedance

CM and DM input impedances for the voltage-mode amplifier may be taken directly from the transconductances as follows

$$Z_{ind} \equiv \left(\frac{v_{sd}}{i_{id}}\right)_{v_{sc}=0} = Y_{dd}^{-1} \quad (82)$$

$$Z_{inc} \equiv \left(\frac{v_{sc}}{i_{ic}}\right)_{v_{sd}=0} = Y_{cc}^{-1} \quad (83)$$

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so that the DM input impedance is

$$Z_{\text{ind}} = \frac{1}{2}\frac{4Z_{\text{cm}}Z_{\text{dm}} + \Delta Z \Delta Z_f}{\overline{Z_f} + \overline{Z}} \tag{84}$$

and the CM input impedance is

$$Z_{\text{inc}} = \frac{1}{8}\frac{4Z_{\text{cm}}Z_{\text{dm}} + \Delta Z \Delta Z_f}{\overline{Z}} \tag{85}$$

Simplifying the expressions for DM and CM input impedance with the small-mismatch approximations in (71) and (72) leads to the 'small-mismatch DM input impedance'

$$Z_{\text{ind s}} = Z_{\text{dm}} = Z_1 + Z_2 \tag{86}$$

and the 'small-mismatch CM input impedance'

$$Z_{\text{inc s}} = Z_{\text{cm}} = Z_1 \| Z_2 + \frac{\overline{Z_f}}{2} \tag{87}$$

which can be approximated for intuition as

$$Z_{\text{inc s}} \simeq Z_1 || Z_2 + Z_{f1} || Z_{f2} \tag{88}$$

The DM and CM input impedance expressions, especially (86) and (88), are intuitive when following the respective current paths (Fig. 2*b*) through the amplifier. As one might expect, the special-case impedances, Z_{dm} and Z_{cm} from (55) and (56), are related to the input impedances, Z_{ind} and Z_{inc} in (84)–(87). In fact, Z_{dm} and Z_{cm} are, by definition, special cases of Z_{ind} and Z_{inc}

$$Z_{\text{dm}} = Z_{\text{ind}}|_{i_{\text{ic}}=0} \tag{89}$$

$$Z_{\text{cm}} = Z_{\text{inc}}|_{i_{\text{id}}=0} \tag{90}$$

Moreover, the results in (86) and (87) suggest that those special cases are coincident with small mismatches in the external homologous elements.

3.3 Discussion

Familiar quantities such as DM–DM gain, A_{vd}, and common-mode rejection ratio (CMRR) are readily extracted and simplified from the modularised result. For instance, DM–DM gain in the result from (81) is

$$A_{\text{vd}} \equiv \left(\frac{v_{\text{od}}}{v_{\text{sd}}}\right)_{v_{\text{sc}}=0} = Y_{\text{dd}}Z_{\text{dd}} + Y_{\text{dc}}Z_{\text{cd}} \tag{91}$$

and expanding this leads to the full DM voltage gain expression (see (92))

This full-gain expression can be simplified to suit the particular non-idealities of interest. For instance, if mismatches are small, the difference between them is smaller ($\Delta Z_f - \Delta Z \simeq 0$), and the second term in the numerator of (92) can be disregarded leaving only $A_{\text{vd}} \simeq Y_{\text{dd}}Z_{\text{dd}}$. In the small-mismatch approximation this becomes

$$A_{\text{vd}} \simeq \frac{4(\overline{Z_f} + \overline{Z})(a_{\text{d}}\overline{Z_f} - (1/2)a_{\text{c}}\Delta Z_f)}{(4Z_{\text{cm}}Z_{\text{dm}})(1 + a_{\text{d}})} \tag{93}$$

where the small second-order mismatch term in the denominator has been left out. Expanding the impedances, Z_{dm} and Z_{cm}, the DM voltage gain above reduces to

$$A_{\text{vds}} = \frac{(a_{\text{d}}\overline{Z_f} - (1/2)a_{\text{c}}\Delta Z_f)}{\overline{Z}(1 + a_{\text{d}})} \tag{94}$$

where we define A_{vds} as the 'small-mismatch DM voltage gain.' In the fully ideal limit, $a_{\text{d}} \to \infty$ and $a_{\text{c}} \to 0$

$$A_{\text{vdo}} = \frac{\overline{Z_f}}{\overline{Z}} \tag{95}$$

where we define A_{vdo} as the 'fully-ideal voltage gain.' The form of A_{vdo} is consistent with intuition that we bring from SE amplifier cases.

Also from (81), the CM–DM cross-coupling gain is

$$A_{\text{vc}} \equiv \left(\frac{v_{\text{od}}}{v_{\text{sc}}}\right)_{v_{\text{sd}}=0} = Y'_{\text{cds}}Z_{\text{dd}} + Y_{\text{cc}}Z_{\text{cd}} \tag{96}$$

and dividing this quantity by the DM–DM gain yields the common-mode rejection

$$\text{CMR} \equiv \left(\frac{A_{\text{vc}}}{A_{\text{vd}}}\right) = \frac{Y'_{\text{cds}}Z_{\text{dd}} + Y_{\text{cc}}Z_{\text{cd}}}{Y_{\text{dd}}Z_{\text{dd}} + Y_{\text{dc}}Z_{\text{cd}}} \tag{97}$$

which can be simplified by neglecting small terms to obtain the approximate CMR

$$\text{CMR} \simeq \frac{4(\overline{Z_f}(a_{\text{c}}/1 + a_{\text{d}}) - \Delta Z)a_{\text{d}}\overline{Z_f} + 4\overline{Z}(a_{\text{c}}\overline{Z_f} - a_{\text{d}}\Delta Z_f)}{4(\overline{Z_f} + \overline{Z})a_{\text{d}}\overline{Z_f} + (\Delta Z_f - \Delta Z)(a_{\text{c}}\overline{Z_f} - a_{\text{d}}\Delta Z_f)} \tag{98}$$

The common denominator in the transconductances (75)–(78) divides out, simplifying the calculation above. Collecting terms, approximating $(1 + a_{\text{d}}) \simeq a_{\text{d}}$, and rewriting (98) gives

$$\text{CMR} \simeq \frac{(a_{\text{c}}/a_{\text{d}}) - ((\overline{Z}/Z_f)\Delta Z_f + \Delta Z/\overline{Z_f} + \overline{Z})}{1 + ((\Delta Z_f - \Delta Z)(a_{\text{c}}/a_{\text{d}} - \Delta Z_f/\overline{Z_f})/4(\overline{Z} + \overline{Z_f}))} \tag{99}$$

Reducing (99) further with the small-mismatch approximations in (71) and (72), the denominator approaches 1, leaving the numerator and we arrive at the 'small-mismatch common-mode rejection'

$$\text{CMR}_{\text{s}} = \underbrace{\frac{a_{\text{c}}}{a_{\text{d}}}}_{\text{'op-amp gains'}} - \underbrace{\frac{(\overline{Z}/\overline{Z_f})\Delta Z_f + \Delta Z}{\overline{Z_f} + \overline{Z}}}_{\text{'external elements'}} \tag{100}$$

$$A_{\text{vd}} = \frac{4(\overline{Z_f} + \overline{Z})(a_{\text{d}}\overline{Z_f} - (a_{\text{c}}\Delta Z_f/2)) + (\Delta Z_f - \Delta Z)(a_{\text{c}}\overline{Z_f} - a_{\text{d}}\Delta Z_f)}{(4Z_{\text{cm}}Z_{\text{dm}} + \Delta Z \Delta Z_f)(1 + a_{\text{d}})} \tag{92}$$

which is neatly separable into an 'op-amp gain term' and an 'external element term'.

Model validation plots for CMR_s in Fig. 8 show good agreement for symmetric mismatches up to about 100% in the feedback and input elements. CMRR is defined here as the logarithmic version of CMR measured in decibels, CMRR $\equiv 20\log_{10}|CMR|$. For calculating CMR with larger mismatches, the expression in (99) can be used for better accuracy as it is shows good agreement for large percentage mismatch (200%). Numerical results from the half-circuit decomposition analysis in [28] are overlaid on the lower plots. Note that in Figs. 8*a* and *b*, the results from [28] are somewhat trivial due to the limitations of the analytical approach employed there.

The model validations also support the well-known fact that the optimal mismatch, yielding the smallest CMR, occurs for non-zero-valued mismatches (see the nulls in Figs. 8*a* and *c*). Although significant, the analysis from [28] does not predict this behaviour. The cancellation effect at non-zero-valued mismatch results from the finite DM and CM gains of the op-amp, a_d and a_c, as is clear from the CMR expression in (100). For example, with $\overline{Z_f} = 100\,\Omega$, the optimal mismatch for the LTC6404-1 for either the feedback or input element mismatch alone is about 0.61% as shown in Fig. 8. In theory, arbitrarily small CMR values could be obtained by adjusting the mismatches to achieve zero-valued CM–DM gain. In practice, such control over the mismatch is perhaps difficult. The zero-crossing of the CM–DM gain, which leads to the null in the CMRR, is also evident in the plot of Fig. 7*b* from Section 3.1. Note that the plots for CMRR in Fig. 8 approach the CMRR of the op-amp, −50 dB, for zero-valued mismatches and are also in agreement with (100).

3.4 Sensitivity

The results in Sections 2 and 3 have shown good model accuracy having considered op-amp gain parameters, a_d and a_c. Examining the sensitivity of the mathematical model to those parameters may reveal the amount of modelling error caused by uncertainties in our knowledge of the op-amp gain parameters. It may also reveal the amount that particular performance metrics change as op-amp gain parameters vary in time due to temperature effects, and so on. In either case, the simple derivative may be employed to examine the effect of changes in the op-amp gain parameters.

For example, starting from (100), the value of feedback impedance mismatch corresponding to the null in CMRR varies with op-amp gain parameters as follows

$$a_d \frac{\partial \Delta Z_f}{\partial a_d}\bigg|_{\substack{\text{CMRR}\to-\infty \\ \Delta Z=0}} = -\frac{a_c}{a_d}\frac{\overline{Z_f}}{\overline{Z}}(\overline{Z_f}+\overline{Z}) \tag{101}$$

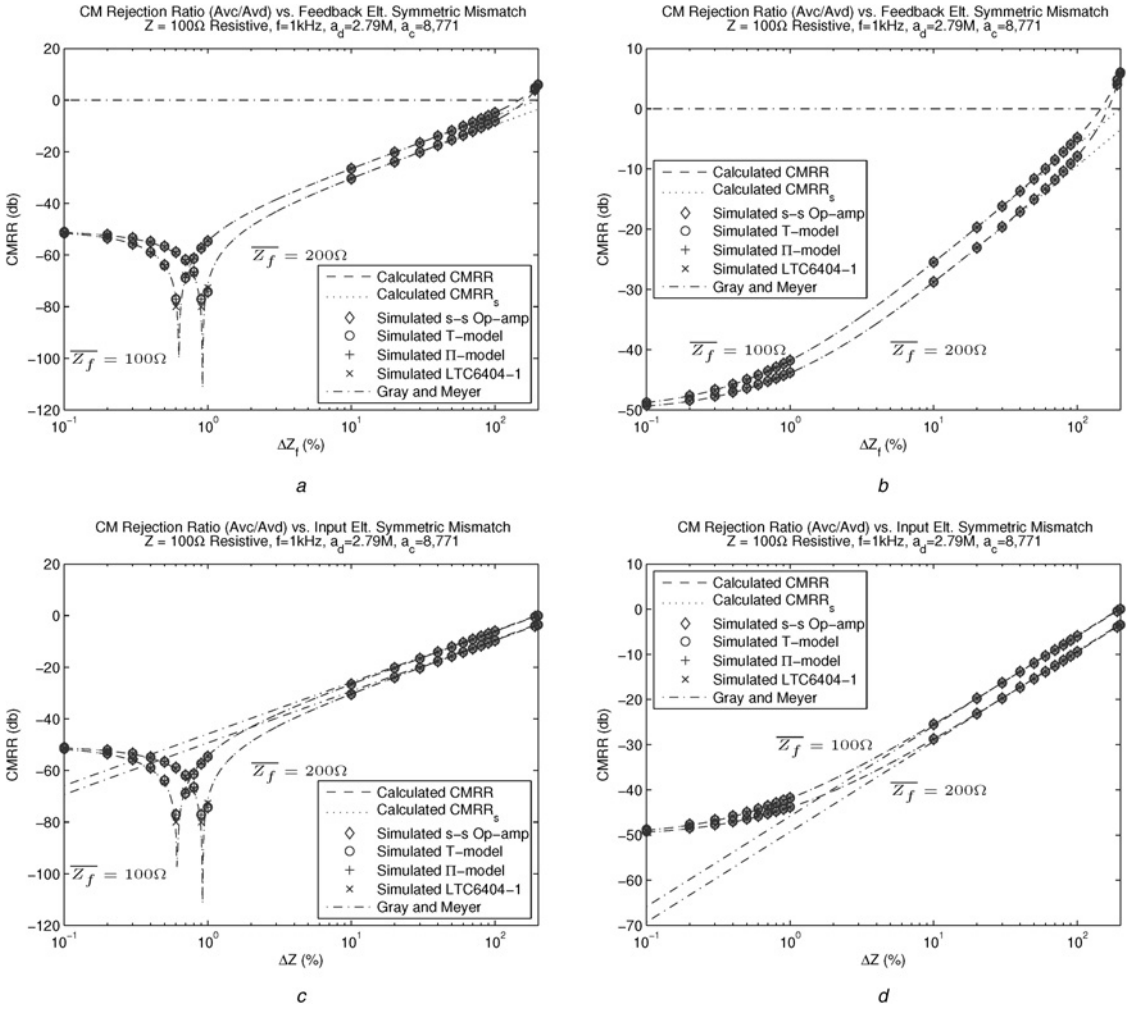

Fig. 8 *Finite op-amp CM gains, a_d and a_c, lead to a null in the CMRR at non-zero mismatch values*

a CMRR for $\Delta Z_f > 0$
b CMRR for $\Delta Z_f < 0$
c CMRR for $\Delta Z > 0$
d CMRR for $\Delta Z < 0$

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$$a_c \frac{\partial \Delta Z_f}{\partial a_c}\bigg|_{\substack{\text{CMRR}\to-\infty \\ \Delta Z=0}} = \frac{a_c}{a_d}\frac{\overline{Z_f}}{\overline{Z}}(\overline{Z_f}+\overline{Z}) \tag{102}$$

Analysis regarding the value of input-element mismatch leads to similar results. Note that the error due to changes in a_d is simply the negative of the error due to changes in a_c.

As a numerical example, consider the nominal impedances $\overline{Z_f} = \overline{Z} = 100\,\Omega$ and op-amp gain parameters from the simulations above. Using (101), a fractional change in DM op-amp gain, $\partial a_d/a_d = -0.15$, corresponding to a multiplicative error of 0.85, leads to an error in the location of the null of approximately $+0.09\%$ in agreement with the results plotted in Fig. 9. Fig. 9 also illustrates the effect of larger changes in a_d. Naturally, the zero-mismatch CMRR should increase as a_d decreases, also in agreement with Fig. 9.

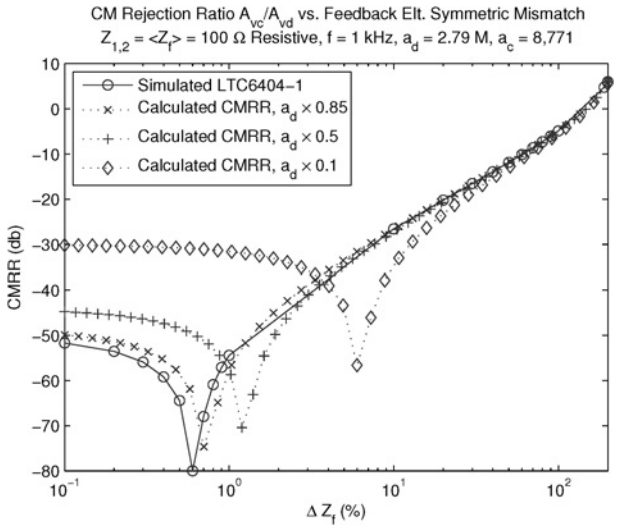

Fig. 9 *Plots of CMRR for various multiplicative errors in op-amp gain a_d compared to the actual CMRR for the linear technology part LT6404-1*

3.5 Finite op-amp input impedance

The results above were calculated based on the op-amp model in Fig. 3 and the assumptions described in Section 1.3. Model validation showed excellent agreement among the calculated results and the behaviour of a commercial FD op-amp. In general, there may be a need to include other aspects in the op-amp model. The versatility of the transimpedance amplifier abstraction developed in Section 2 was demonstrated in a first example, by adding to it the input elements, Z_1 and Z_2, yielding a voltage amplifier. Here, we consider the addition of finite op-amp input impedance to the idealised op-amp model of Fig. 3.

The op-amp input impedance elements can be modelled as shunt impedances at the op-amp input nodes to incremental ground. The addition of those impedances can be viewed as a modification of the voltage amplifier analysis in Section 3 leading to the four transconductances, Y_{dd}–Y_{cc}. Since the transimpedance amplifier model responses were derived in terms of the input currents i_+ and i_-, only the voltage amplifier analysis needs to be iterated.

Using the Thevenin equivalent circuits comprising the input voltage sources and impedances Z_1, Z_2 and the additional op-amp input impedance elements, (48)–(51) become

$$i_+|_{v_{sd}=0} = \frac{(v_{sc}(Z_{in\,1}/Z_{in\,1}+Z_1)-e_{cc})}{Z_1||Z_{in\,1}} \tag{103}$$

$$i_-|_{v_{sd}=0} = \frac{(v_{sc}(Z_{in\,2}/Z_{in\,2}+Z_2)-e_{cc})}{Z_2||Z_{in\,2}} \tag{104}$$

$$i_+|_{v_{sc}=0} = \frac{((1/2)v_{sd}(Z_{in\,1}/Z_{in\,1}+Z_1)-e_{cc})}{Z_1||Z_{in\,1}} \tag{105}$$

$$i_-|_{v_{sc}=0} = \frac{(-(1/2)v_{sd}(Z_{in\,2}/Z_{in\,2}+Z_2)-e_{cc})}{Z_2||Z_{in\,2}} \tag{106}$$

Starting from these modified constraints, one can re-derive the four tranconductances in terms of op-amp input impedances,

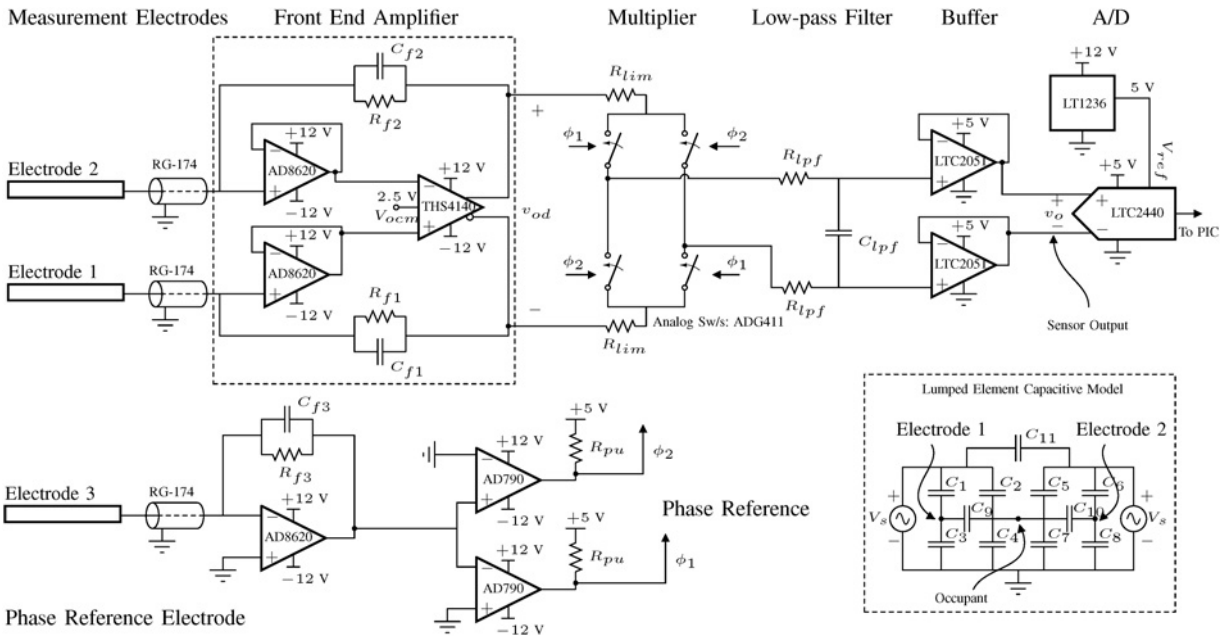

Fig. 10 *Simplified schematic of the FD signal conditioning electronics*

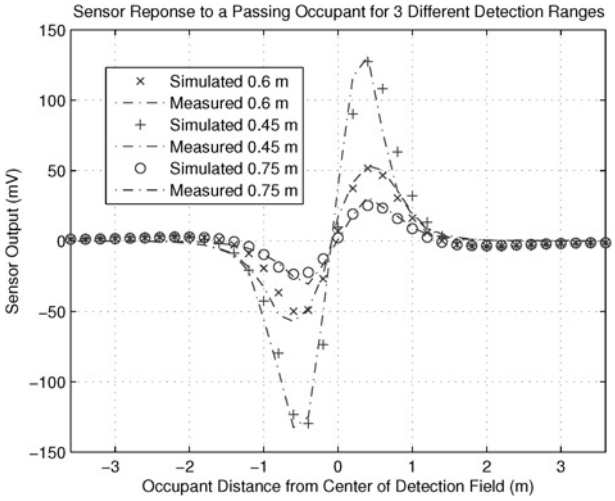

Fig. 11 *Plot of simulated and measured occupancy sensor output data from [25]*

$Z_{\text{in }1}$ and $Z_{\text{in }2}$, while keeping the same results for the two transconductances found in Section 2.

4 Experimental validation

This treatment of FD amplifiers was motivated by an investigation of a particular capacitive occupancy sensor. The sensor, presented in [25], employs a FD amplifier connected between two electrodes, to measure changes in a physically balanced bridge network comprising the lumped capacitances between conducting bodies in the detection field. A half-circuit representation of the FD amplifier was not suitable for capturing the effect of the arbitrarily varying capacitive impedances in the bridge network nor was it sufficient to account for the effects of the amplifier's separate DM and CM current paths. Only a generalised model with an unbroken structure could accurately represent these effects. In this application example, the distributed capacitances comprising the bridge network in the capacitive sensor take the place of the impedance elements, Z_1 and Z_2 from Fig. 1. Imbalances in the complicated capacitive bridge network indicate a detection of an occupant. It is precisely those imbalances that must be captured accurately by our model of the FD amplifier. The power of the intermediate FD transimpedance amplifier circuit model from Section 2 is highlighted in this example because it accurately captures the behaviour of the FD structure and its effect on a complicated and intentionally asymmetric impedance network.

Fig. 10 shows a schematic of the signal conditioning electronics for this capacitive sensor including the FD front-end amplifier. The signal processing scheme represented by the electronics in Fig. 10 is synchronous detection, a well-known approach to isolating baseband signals in amplitude modulated carrier signals. Also shown in the figure is a simplified depiction of the lumped element capacitive bridge network. The capacitive impedances in the bridge network correspond to the input impedance elements Z_1 and Z_2 in Fig. 1. The FD front-end amplifier is loaded by a FD multiplier circuit used to synchronously detect modulations of the high-frequency carrier signal caused by the presence of the occupant. More details can be found in [25].

A comparison of experimental and simulated data further validated the analytical modelling in this paper. Experimental data was taken from an implemented capacitive sensor using the electronics shown in Fig. 10. Simulated data was taken from a SPICE simulation of the experimental setup having replaced the front-end amplifier with the circuit model of the FD amplifier in Fig. 4*b*. Finite op-amp input impedances as well as coaxial shield stray capacitances were included in the simulated model as shunt impedances at the input terminals to the transimpedance amplifier circuit model. In the experimental system from [25], the Texas Instruments FD op-amp part THS4140 was used. Model parameters, a_d and a_c, for the FD front-end circuit model were taken from the datasheet for the THS4140 FD op-amp at the signal frequency, 50 kHz in this example. Based on the gain bandwidth product of the THS4140 part, the signal frequency is well below the cross-over frequency for that op-amp and so the basic assumptions stated at the beginning of this paper are valid. Significantly, the model validation in this section will serve to prove the utility of the circuit models and analysis developed in this paper for yet another commercial FD op-amp.

Finite-element modelling software, FastCap®, was used to determine the values of the lumped element capacitances needed for the SPICE simulation. To simulate a passing occupant, the FastCap® simulation was re-run for several different configurations of the system corresponding to different time steps as the occupant passed through the detection field. Details can be found in [25].

Model validation results showing excellent agreement are plotted in Fig. 11. Data and simulation are shown for three different detection ranges as the occupant passes through the detection field. The detection range is defined as the smallest perpendicular distance between the transmitting (source) electrode in the capacitive sensor and the occupant as the occupant passes through the detection field. Refer to [25] for more details.

5 Conclusion

A new approach for small-signal analysis of FD closed-loop op-amp circuits is presented. The approach is built upon the development of a circuit model for a FD transimpedance amplifier. The circuit model of the FD transimpedance amplifier enables analysis and simulation of practical FD circuits and captures the distinct CM and DM paths through the amplifier. Simulated model validation showed excellent agreement between the calculated results and the performance of a commercial FD op-amp. Experimental model validation showed excellent agreement between the behaviour of the simulated FD transimpedance amplifier circuit model and an implemented capacitive sensor employing a FD front-end amplifier.

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