Power Electronic Circuits for Magnetic Energy Harvesters

Jinyeong Moon, *Student Member, IEEE*, and Steven B. Leeb, *Fellow, IEEE*

***Abstract*—Compared to many other energy harvesting schemes, harvesting energy from magnetic fields offers potential advantages for energy extraction and sensing. A magnetic energy harvester provides great flexibility for sensors and monitoring applications for condition-based monitoring of electromagnetic actuators, including vibration and thermal monitoring. A core must be managed or operated with carefully timed saturation to ensure maximum power extraction, a complex problem given the nonlinear saturation characteristics of a magnetic core [1]. This paper presents a simulator-friendly "circuit model" for a magnetic core, and uses this model to design and demonstrate several power electronic circuit solutions for harvesting energy. The circuit model has an excellent accuracy to represent the core regardless of the level of saturation. The design techniques to enhance power harvest are proposed, and verified through simulation and experiments, substantially boosting the amount of power harvest.**

***Index Terms*—Current driven, energy harvester, flux-shaping capacitor (FSC), magnetic, rectifier, saturation, transfer window, transfer window alignment (TWA).**

I. Introduction

ENERGY available to a sensor or monitoring hardware may be limited in situations where the sensor is only powered by an environmental energy harvester [3]–[6]. Available energy and power from the harvester may profoundly limit sample rate, data precision, signal processing, transmission bandwidth, and data storage capacity and rates [7]. The selection of environmental parameter from which to harvest energy (e.g., vibration [8]–[11], thermal gradients [12], [13], light [14], etc.) can limit the performance and even the feasibility of a power-harvesting sensor node. This paper considers the design of magnetic field energy harvesters and associated power electronic circuits. These circuits are used to create a sensor node called vibration assessment monitoring point with integrated recovery of energy for measuring *in situ* vibration, temperature, and other environmental parameters for motors [3]. The design techniques and power harvesting circuits presented in this paper could be applied to many other sensing and actuation problems.

This approach uses a magnetic core configured similarly to a traditional current-sense transformer. A line powering a load of interest passes through the center of the core. A relatively high-turns secondary winding is used for recovering energy for a monitoring circuit. This paper presents three new circuit designs to enhance the amount of extracted energy: the flux-shaping capacitor (FSC) method, the transfer window alignment (TWA) method, and an active rectifier. An important analytical concept for designing these harvesters is the "transfer window," explained in the next section. The proposed rectifier is to reduce the switching loss, caused by nonideal diodes in a rectifier. To validate and verify the design of energy harvester circuits using any of these methods, it is convenient to have an analytical model of the highly nonlinear magnetic core. This paper therefore begins with the development of a "circuit-friendly" core model based on the analytical model presented in [1]. The model will be shown to have excellent prediction on power harvest, and will be used to design and evaluate demonstrations of the harvesting techniques.

Manuscript received March 17, 2014; revised October 29, 2014; accepted February 4, 2015. Date of publication February 6, 2015; date of current version September 21, 2015. This work was supported by the Kwanjeong Educational Foundation and the Office of Naval Research Structural Acoustics Program. Recommended for publication by Associate Editor C. K. Tse.

The authors are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139, USA (e-mail: jinmoon@mit.edu; sbleeb@mit.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2401336

II. Background

The analysis in [1] involves two load types: resistive loads and constant voltage loads. The resistive load model is simple and illustrative of core behaviors, but not appropriate for a magnetic energy harvester, especially when the load is a dc–dc converter or a supercapacitor powering a sensor suite. The resistive load model will be used where appropriate to illustrate techniques, but the "constant voltage" load will be used to design and evaluate the behavior of circuits.

The core in the magnetic energy harvester is energized by a primary winding that is effectively acting as a current source. The insertion impedance of the harvester transformer is generally extremely low; therefore, the load under observation, for example, a motor, sets or commands the current flowing through the primary of the harvester. Saturation of the harvester core is determined by the interaction of this primary current with the time and level of voltage applied to the secondary winding of the harvester.

When a magnetic core is saturated, the secondary-side voltage across the core becomes essentially zero, because the time derivative of the magnetic flux density in the core (B) is near zero in saturation. The magnetizing inductance (referred to the secondary side) is therefore extremely low during this period, and little power is coupled from the primary winding. With a high permeability core, when the core is not saturated, the impedance of the magnetizing inductance is relatively high, and significant power transfer can occur to the load in the secondary. The "transfer window" is introduced in [1] to describe this distinct region when significant power flow occurs through the core across the transformer. Circuit design methods are developed based on this concept of the transfer window in order to permit control and maximization of harvested energy.

III. Circuit Model

The Maxwell model discussed in [1] is complete for simulating a circuit if all the components are described in a numerical solver. The model provides little intuitive insight, and requires a custom-designed numerical solver that quickly becomes undesirable when combined with power electronic circuits on the secondary that consist of nonlinear switching devices. Here, a model for a magnetically saturating core that can be directly employed in SPICE is developed. This model will be used to validate experimental results for our power harvester converters.

A. Circuit Model

Denoting a number of windings of the secondary, the saturation flux density, outer radius, inner radius, and height of a toroidal core by N, A_{CORE}, B_{SAT}, r_{OD}, r_{ID}, and h, respectively, the flux linkage in the toroidal core of the magnetic energy harvester can be described as

$$\Lambda(t) = N \cdot h \cdot \int_{r_{\mathrm{ID}}}^{r_{\mathrm{OD}}} B(r,t)\ \mathrm{d}r. \tag{1}$$

Here, the spatial integration is approximated by modeling the core flux density at every radius as equal to the core flux density at $r_{\mathrm{mid}} = (r_{\mathrm{OD}} + r_{\mathrm{ID}})/2$. Then, using the same saturation function as in [1], the expression for the flux can be approximated as

$$\begin{aligned}\Lambda(t) \approx\ & B_{\mathrm{SAT}}\,(r_{\mathrm{OD}} - r_{\mathrm{ID}})\,h\,N \\ & \times \frac{2}{\pi}\arctan\left(\frac{I_{\mathrm{P}}\sin(\omega\,t) - N\cdot I_{\mathrm{S}}(t)}{2\,\pi\,r_{\mathrm{mid}}\,\alpha}\right).\end{aligned} \tag{2}$$

This equation can be written compactly as

$$\Lambda(t) = \Lambda_{\mathrm{MAX}} \cdot \frac{2}{\pi}\arctan\left(\frac{N}{\beta}\,I_{\mu}(t)\right) \tag{3}$$

using the parameters defined as

$$\Lambda_{\mathrm{MAX}} = B_{\mathrm{SAT}}\,(r_{\mathrm{OD}} - r_{\mathrm{ID}})\,h\,N = B_{\mathrm{SAT}}\ A_{\mathrm{CORE}}\ N \tag{4}$$

$$\beta = 2\,\pi\,r_{\mathrm{mid}}\ \alpha = l_{\mathrm{FLUX}}\ \alpha \tag{5}$$

$$I_{\mu}(t) = \frac{I_{\mathrm{P}}}{N}\sin(\omega\,t) - I_{\mathrm{S}}(t). \tag{6}$$

By interpreting (6) as a KCL constraint, a node with three branches can be virtually created for the representation of the magnetic core. The first branch is $I_{\mathrm{P}}/N \cdot \sin(\omega\,t)$, supplying the current into the node. This can be easily represented by an ideal current transformer with the winding ratio of $1:N$ and primary current of $I_{\mathrm{P}}\sin(\omega\,t)$. The second branch is $I_{\mathrm{S}}(t)$, taking the current out of the node. It can be treated as the load current supplied from the core. The third branch is the current remainder $I_{\mu}(t)$ as defined, and the (3) describes the relationship between current and flux of the third branch. The relationship between voltage and current of this branch can be obtained by time differentiation of the flux

$$V_{\mathrm{CORE}}(t) = \frac{\partial}{\partial t}\left[\Lambda_{\mathrm{MAX}} \cdot \frac{2}{\pi}\arctan\left(\frac{N}{\beta}\,I_{\mu}(t)\right)\right]. \tag{7}$$

Considering the derivative of $\arctan(x)$ is $1/(1+x^2)$, the flux (3) indicates that the third branch is in the general form of an inductor. The inductance is nonlinear and time varying in an application with an ac current in the primary winding. This is consistent with intuition about the core as for an unsaturated core with constant permeability, we would expect the core to appear from winding terminals as an inductance.

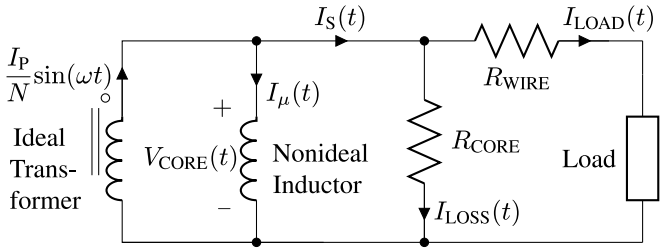

Fig. 1. Circuit model.

Summarizing branch descriptions, the circuit configuration can be presented as in Fig. 1. The circuit model builds from an ideal transformer and adds a nonideal inductor in parallel with it, while the Maxwell method has a lumped nonideal transformer that includes the effects of both. Using either a nonideal inductor element that supports a flux description or a behavioral voltage element, the (7) can be directly used in SPICE with ease. The circuit model is attractive because it is easier to mix with power electronic components, such as MOSFETs and diodes in SPICE. A concern remains in determining core loss, which affects the overall performance of the harvester. A SPICE simulation can track the voltage across and current through the nonideal magnetizing inductance and use these waveforms to calculate the area under a B–H curve as a scaled ratio of the maximum loss presented by the full hysteresis curve for the materials

$$P_{\mathrm{LOSS}} = P_{\mathrm{LOSS-MAX}} \cdot \frac{I_{\mathrm{PEAK}}}{I_{\mathrm{SAT}}} \cdot \frac{B_{\mathrm{PEAK}}}{B_{\mathrm{SAT}}} \tag{8}$$

as described in [1]. A circuit simulator can therefore, also accurately model core loss by updating the value of R_{CORE} with a numerical estimate. Additional loss mechanisms like conduction loss can also be modeled, e.g., by R_{WIRE}, as shown in Fig. 1.

In the following sections, the accuracy of the circuit model will be verified, and circuit design techniques based on this circuit model will be introduced to enhance power harvest of a magnetic energy harvester.

B. Model Accuracy

The accuracy of this circuit model can be verified by comparison to experimental data, and to a full Maxwell model of the core described in [1]. Assuming the same core, Vacuumschmelze (VAC) VITROPERM 500F W380, the estimated parameter values, B_{SAT}, $P_{\mathrm{LOSS\text{-}MAX}}$, α, β, and dimensional properties of the core are listed in Table I.

In Fig. 2, four plots are presented to compare the accuracy of the circuit model to the Maxwell model and the experiments. Model accuracy is considered for two load types. The top two plots represent cases with a resistive load, and the bottom two plots represent cases with a constant voltage load. For the resistive load cases, a rectifier is not required to measure the

TABLE I
CORE PARAMETERS

B_{SAT}	1.190 T
$P_{\mathrm{LOSS\text{-}MAX}}$	0.125 mW
α	2.2
β	0.142
Outer Radius (r_{OD})	12.25 mm
Inner Radius (r_{ID})	8.25 mm
Height (h)	9 mm
Flux Area (A_{CORE})	3.6×10^{-5} m^2
Flux Length (l_{FLUX})	6.44×10^{-2} m

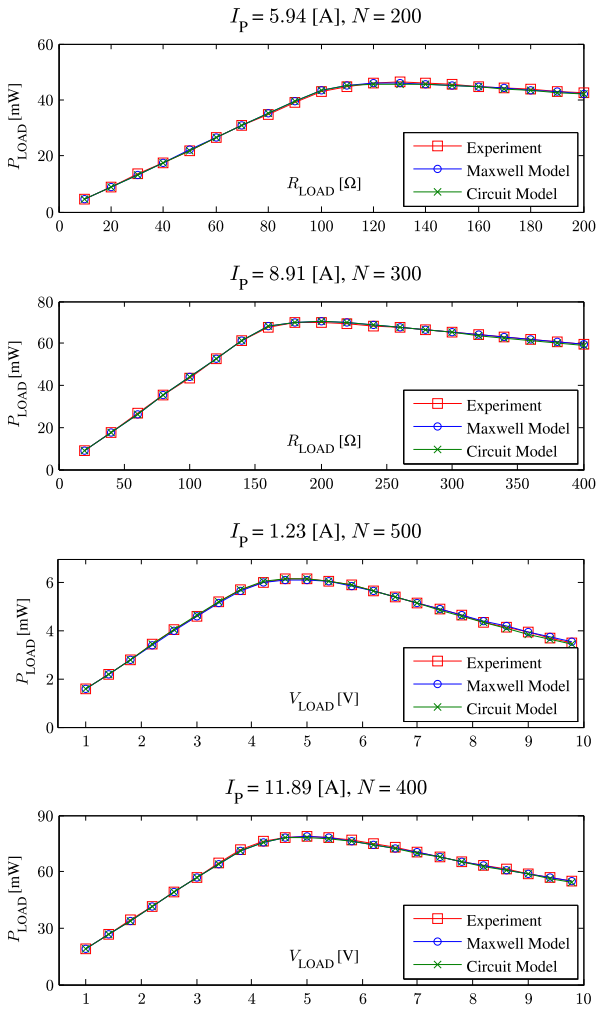

Fig. 2. Experimental verification of the circuit model.

power delivered to the load. Direct measurements of the RMS voltage across the load resistor were used to quantify the power delivered. For the constant voltage load cases, a rectifier is required to measure the power harvest. To prevent or minimize any changes to the core flux (and power loss calculation), an active rectifier with 95% utilization of active devices is used. Each diode in a conventional full-bridge diode rectifier is replaced with a Schottky diode (PMEG2010ER [18]) and a FET (PMV30UN [20] or DMG3415U [19]) in parallel to mimic an ideal rectifier. The next section discusses the experimental configuration in greater detail.

For the tests, different I_{P} and N configurations are used. As illustrated in the figure, regardless of the load type, I_{P}, and N, the circuit model is as accurate as the Maxwell model, closely tracking the experiments. Approximations made in the modeling, e.g., uniformity of the magnetic flux density throughout the core and approximating the saturation characteristic with an $\arctan$ function provide excellent accuracy for designing energy harvesting systems.

IV. MAXIMIZING THE POWER HARVEST

The duration and level of the voltage applied to the secondary winding by the harvester circuitry determines when the flux in the core will build to saturation levels. At a high level, maximizing the power harvest boils down to the problem of keeping the core out of saturation for a "best" period of time. This window or period of time would ideally allow the fixed secondary current to flow for the longest period of time with the highest secondary voltage. This time period when current flows through the transformer action (while the core is not fully saturated) is the transfer window. Of course, the core could always be operated so that it never saturates. Fig. 2 demonstrates that the unsaturated core, which is in a strictly linear region in lower R_{LOAD} or V_{LOAD}, always corresponds to a less-than-maximal power harvest. Permitting the core to eventually saturate over the course of a primary waveform cycle provides maximum power harvest. The trick is to time this saturation to maximize the energy extraction.

Three different circuit techniques can be used to maximize the extent and precise timing of the power transfer window. The first involves placing a capacitance in series with the core before a rectifier stage. The capacitor shapes the flux developed across the core, and lengthens the transfer window. The second is to connect the load to the core such that the middle of the transfer window is aligned with the peak of the transformer current. At other times, the load is disconnected from the core, and the core is externally shorted to prevent itself from accumulating flux. The two techniques cannot be used at the same time; however each technique is capable of substantially enhancing the power harvest compared to an unmodified current transformer. The third technique is to use a rectifier with active gate control instead of passive rectifiers. If the gate control is available at relatively low cost, e.g., from a microcontroller already serving in the sensor system, active rectification can be used with either one of the first two techniques.

A. Flux-Shaping Capacitor

Since the magnetizing inductor is not an ideal inductor, the load receives power only when the core is not saturated. This means that the transfer window is active when the magnetizing inductance appears as a large shunt impedance across the secondary. To lengthen the transfer window, a way to manipulate the volt–seconds applied to this inductor is sought. The net voltage applied to the magnetizing inductance can be reduced by placing a capacitor C_{F} in series with the load. This capacitor charges during any particular half cycle. During the next half cycle, the capacitor is charged with a voltage polarity opposite to that of the constant voltage load. By reducing this net

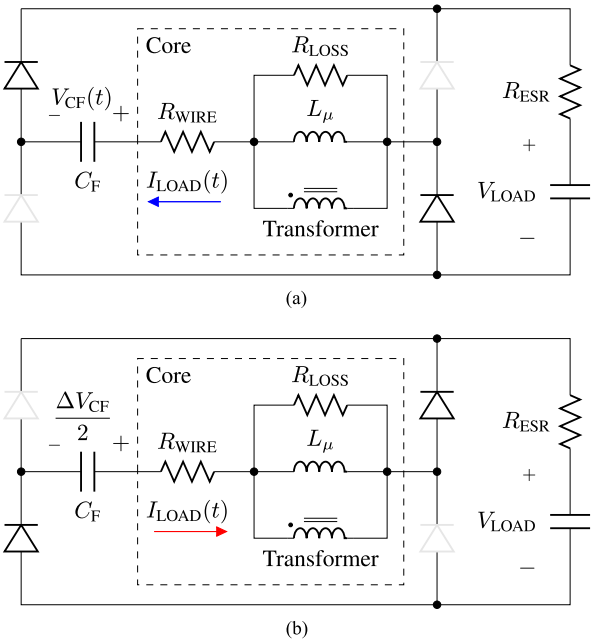

Fig. 3. Circuit example with an FSC. (a) Before the current path reversal. (b) Right after the current path reversal.

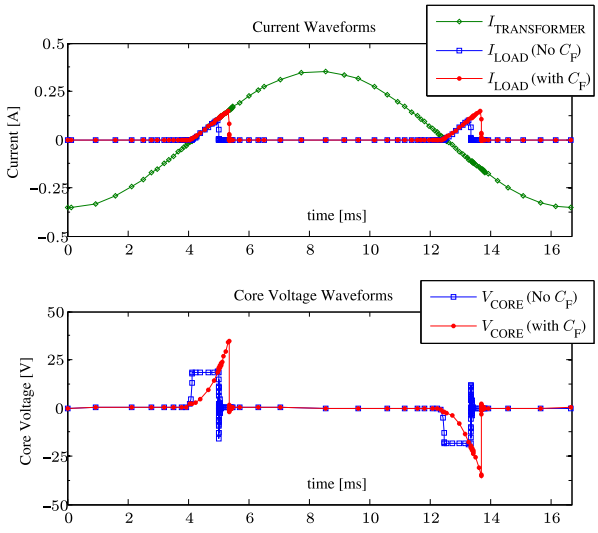

Fig. 4. FSC simulation example in hard saturation ($I_{\mathrm{P}} = 50\,\mathrm{A_{RMS}}$, $N = 200$, $V_{\mathrm{LOAD}} = 18\,\mathrm{V}$, $C_{\mathrm{F}} = 2.9\,\mu\mathrm{F}$).

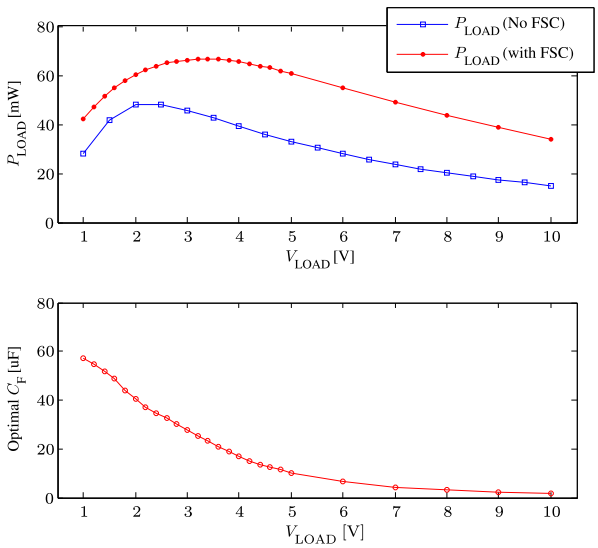

Fig. 5. Simulation of the FSC method ($I_{\mathrm{P}} = 6.27\,\mathrm{A_{RMS}}$, $N = 200$).

voltage applied to the magnetizing inductance, flux accumulation becomes slower, lengthening the power transfer window and increasing the power delivered to the load.

When C_{F} is added to the circuitry, it is no longer possible to obtain a simple expression for the maximum power harvest point, as presented eq. (19)]. Instead of finding a numerical solution through a simulator, it is practical to develop an insight by analyzing the core behavior in a qualitative way. In Fig. 3(a), where the current flows to the left, the current charges up the FSC, increasing $V_{\mathrm{CF}}(t)$ until the core is saturated. When the core is saturated, the voltage across the magnetizing inductance becomes zero, preventing the transformer current from going into the load. At this instant, depending on the voltage across C_{F}, the diodes may either all turn-off or briefly switch to the alternate conduction path. If $V_{\mathrm{CF}}(t)$ is higher than V_{LOAD}, then the current path briefly switches and supplies current from C_{F} into the load until $V_{\mathrm{CF}}(t)$ is equal to V_{LOAD}, at which point the diodes turn off. This brief period continues power delivery to the load. If $V_{\mathrm{CF}}(t)$ is not higher than V_{LOAD}, the diodes are all disconnected, keeping $V_{\mathrm{CF}}(t)$ constant until the core recovers from the saturation and reverses the current direction. In the steady-state, net charge into the FSC is zero. Therefore, both positive and negative voltage peaks will have the same magnitude of $\Delta V_{\mathrm{CF}}/2$.

Right after the reversal of the main current path, as illustrated in Fig. 3(b), the voltage across the core starts from $V_{\mathrm{LOAD}} - \Delta V_{\mathrm{CF}}/2$, whereas it is always V_{LOAD} if we do not use a FSC. For a sinusoidal primary current, $V_{\mathrm{CF}}(t)$ is a cosine wave, and, therefore, $V_{\mathrm{LOAD}} - V_{\mathrm{CF}}(t)$ becomes convex. Starting from a lower voltage and developing it in a convex manner due to the flux-shaping actions of the capacitor indicate that the transfer window is lengthened in the tail. Lengthening the transfer window by a small amount can result in a great boost in power harvest. Fig. 4 illustrates a simulation example, where the transfer window is visibly lengthened by an FSC. To illustrate the effect, Fig. 4 shows simulated results with an operating point of $I_{\mathrm{P}} = 50\,\mathrm{A_{RMS}}$, $N = 200$, $V_{\mathrm{LOAD}} = 18\,\mathrm{V}$, and $C_{\mathrm{F}} = 2.9\,\mu\mathrm{F}$. The power harvest is increased by 107.12% compared to the case with no FSC.

In a real design, the optimal V_{LOAD} and C_{F} must be found, subject to a given I_{P} and N configuration. Since it is not analytically possible to predict the peak, both parameters were swept to find the maximum power harvest as in Fig. 5. The lower plot represents the corresponding C_{F} that yields the maximum power harvest for each V_{LOAD}. In this example, $I_{\mathrm{P}} = 6.27\,\mathrm{A_{RMS}}$, $N = 200$, and a nonideal diode rectifier with a manufacturer provided SPICE model is used. The diode rectifier in the simulation consists of four Schottky diodes with an approximate forward voltage drop of $0.19\,\mathrm{V}$ in a milliampere range. The maximum harvestable power of $48.6\,\mathrm{mW}$ without the FSC now

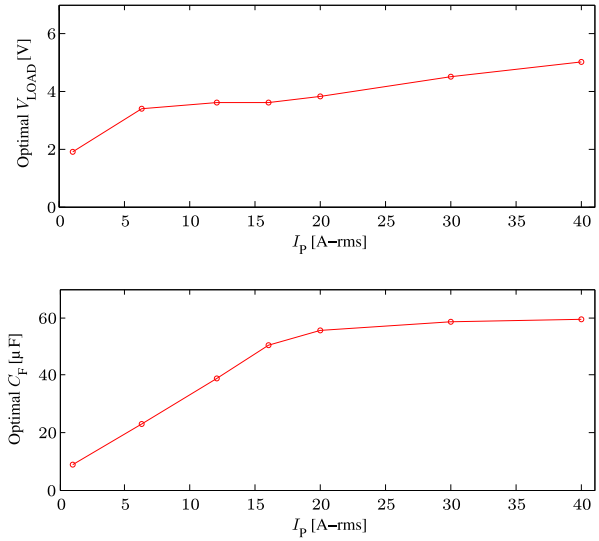

Fig. 6. Simulation of optimal V_{LOAD} and C_{F} versus I_{P}, with $N = 200$.

reaches 66.6 mW, which is a net increase of 37.04%. However, there is a major issue in this method that if the RMS of the primary current continuously changes, for example, in case of periodic motor speed control, optimal V_{LOAD} and C_{F} for the maximum power harvest also continuously change. An example is illustrated in Fig. 6 with $N = 200$. Changing V_{LOAD} can be relatively easily accomplished by connecting a power converter with programmable duty cycle control as a load. However, two concerns associated with changing capacitance remain. First, the optimal capacitance spans a wide range as illustrated in Fig. 6. Second, an attempt to tune the capacitance, e.g., by selecting a capacitor from a bank of choices, requires a circuit that can effectively operate with the capacitor in a "floating" position in the circuit, complicating switch implementation.

If the primary current is extremely low such that the core never saturates during operation, adding a capacitor in series with the core, which maintains constant inductance in this case, can be viewed as a power factor corrector. This makes the waveform of the load current more rectangular, and results in higher average current. Due to this effect, the amount of power harvest is boosted even in the nonsaturated region with the FSC, as shown near the initial linear region in Fig. 5. Since the load is a constant voltage source, the average power harvest is directly proportional to the average current, not the RMS current.

B. Transfer Window Alignment

Alternatively, it is possible to actively control the connection between the magnetic core and the load, and manipulate the starting point of the transfer window relative to the zero crossing of the primary current. This manipulation is possible because the load voltage is independent of the primary current for the case of a constant voltage load. Assuming ideal rectifiers, the duration of the transfer window in the first-order approximation is

$$t_{\mathrm{SAT}} = \frac{2\,B_{\mathrm{SAT}}\,A_{\mathrm{CORE}}\,N}{V_{\mathrm{LOAD}}}. \tag{9}$$

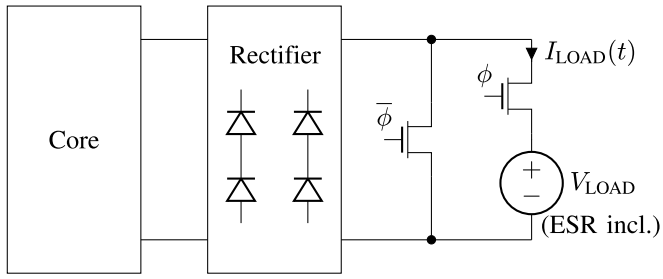

Fig. 7. TWA circuit.

That is, the core will be saturated if V_{LOAD} is connected to the core for t_{SAT} seconds, regardless of when the transfer window begins relative to the zero crossing of the primary current. Given this understanding, the transfer window, which permits the greatest energy harvest corresponds with a window of time when the average primary current is as large as possible. This is achieved when the middle of the transfer window is aligned with the peak of the transformer current, and the core is "shorted out," reducing the voltage on the secondary winding to zero, during times outside the transfer window in order to prevent the core from developing unnecessary flux. Without a detailed nonlinear description of the magnetic core, an estimate for the average power harvest using this TWA method is

$$\begin{aligned} P_{\mathrm{LOAD,\,avg}} &= V_{\mathrm{LOAD}} \times \frac{2}{T} \int_{\frac{T}{4}-\frac{t_{\mathrm{SAT}}}{2}}^{\frac{T}{4}+\frac{t_{\mathrm{SAT}}}{2}} \frac{I_P}{N} \sin(\omega\, t)\ \mathrm{d}t \\ &= P_{\mathrm{TWA}} \cdot \frac{\sin(J)}{J} \end{aligned} \tag{10}$$

where

$$P_{\mathrm{TWA}} = \frac{2\,I_{\mathrm{P}}\,\omega\,B_{\mathrm{SAT}}\,A_{\mathrm{CORE}}}{\pi}$$

$$J = \omega\,\frac{B_{\mathrm{SAT}}\,A_{\mathrm{CORE}}\,N}{V_{\mathrm{LOAD}}} = \omega\,\frac{t_{\mathrm{SAT}}}{2}. \tag{11}$$

Since $\sin(J)/J$ has an asymptote of 1 as $J \to 0$, P_{TWA} is the maximum value of $P_{\mathrm{LOAD,\,avg}}$. This indicates that J must be minimized to maximize the power harvest. However, J cannot be arbitrarily small, as t_{SAT} would become proportionally small as well. As t_{SAT} becomes smaller, the portion of the cycle that is mainly described by (9)—the first-order approximation—becomes smaller. In this case, the power harvest deviates from the first-order predictions, and in fact becomes smaller. Nonideal effects cause this reduction in power. For example, the magnetizing inductance, which has been already reset once the primary current became sufficiently low in the previous cycle, carries a small remnant current from the previous cycle in the opposite direction to the load current at the beginning of the transfer window. This results in a slight boost in the load current. On the other hand, before full saturation, the magnetizing inductance gradually drops to zero, causing a smoother roll-off of the load current at the end of the transfer window, resulting in a lower load current than the transformer current (these two nonideal effects can be seen in Fig. 8). These two deviations are not perfectly balanced—the loss is higher—, and reduce the power harvest from the first-order estimate. Furthermore, with smaller

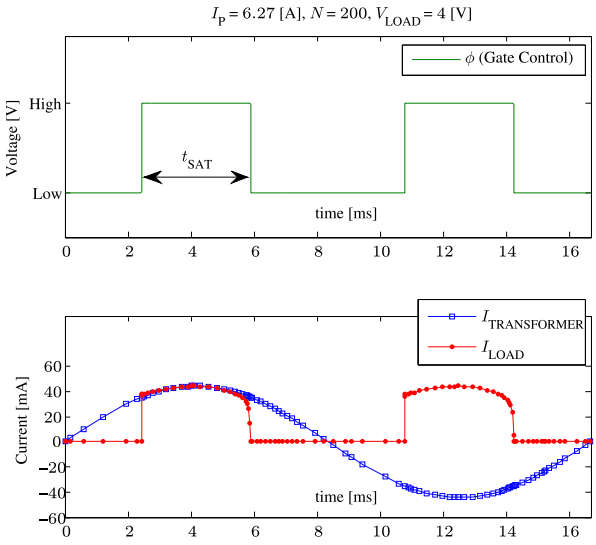

Fig. 8. Time domain waveform with the TWA.

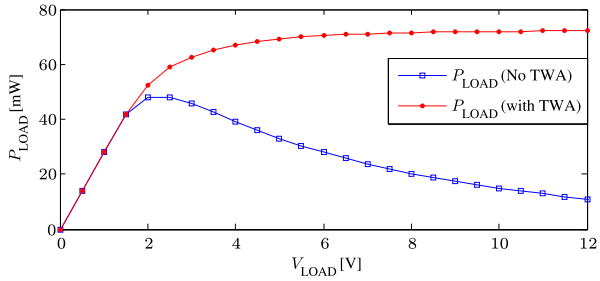

Fig. 9. Power harvest enhancement with the TWA ($I_P = 6.27\,A_{RMS}$, $N = 200$).

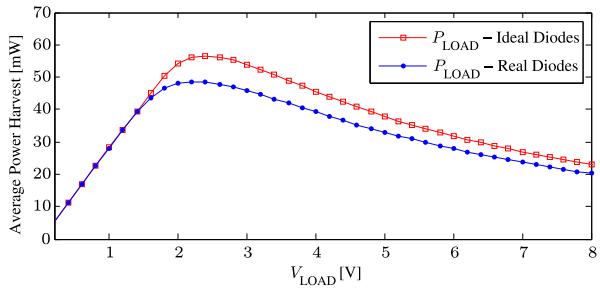

Fig. 10. Effect of real diodes in a rectifier on harvestable power ($I_P = 6.27 A_{RMS}$, $N = 200$).

t_{SAT}, a finer time resolution is required for generation of control signals, and at a certain limit, the gate control is no longer completely accurate because of the fixed timing margins for the edge transitions of the TWA switches to avoid a short-circuit path from the load to the ground. A practical rule of thumb for design is to select $t_{SAT} \geq T/10$, in which case $J \geq 0.314$, based on our experimentation with high permeability cores at utility line frequencies.

Given a core material with known magnetic properties and size, there are essentially two parameters available to the designer N and V_{LOAD} for minimizing J. Decreasing N increases the secondary-side current and amplifies losses in the switches and diodes. The voltage V_{LOAD} cannot be arbitrarily high due to the voltage ratings of the switching devices in the rectifier. Raising V_{LOAD} may also incur unnecessary losses in the digital circuits that would typically form the sensor and communication load if they are directly powered by V_{LOAD}. Therefore, N and V_{LOAD} must be carefully chosen to minimize J without incurring unnecessary losses in the rest of the harvester circuit. One aspect that can aid to loosen the design constraint is that since minimizing J has a diminishing return on the amount of power harvest, the value of J can actually settle at a more reasonable level. It may be tolerable to slightly increase J in order to optimize overall system losses. For example, a circuit designer can pick $J = 0.6$, providing approximately 94% of the maximally achievable power harvest P_{TWA}, while reducing the control power and the switching losses.

The TWA method requires only two additional switches after the rectifier, as shown in Fig. 7, and does not require any on-the-fly component change as was needed for the FSC method. In Fig. 7, ϕ indicates a phase where we connect the load to the core, and $\overline{\phi}$ indicates the opposite phase. The simulation, presented in Fig. 8, clearly illustrates the shifted transfer window. Note both plots in Fig. 8 are generated with the same time reference. Using the same $I_P = 6.27\,A_{RMS}$ and $N = 200$, Fig. 9 demonstrates the enhancement of power harvest with the TWA method. The maximum power harvest is much higher with TWA. For Fig. 9, a diode full-bridge rectifier based on the manufacturer provided SPICE model of the same Schottky diode mentioned in Section III-B is used. Effects of nonideal diodes will be discussed in the following section.

The TWA method drives the core into saturation more definitively than the FSC method. As J is minimized for enhancing the power harvest, t_{SAT} becomes shorter, which means the core goes deeper into the saturation regime.

C. Rectifier With Active Gate Control

Using either of the above methods, to extract power from the core, the switching devices in a rectifier must be operated in accordance with the polarity of the transformer current so that the current flows only from the core into the load. Diodes naturally enforce this condition. However, a rectifier implemented with diodes actually has an unavoidable diode voltage drop V_{DIODE}. Because the core is a current-driven transformer, the load current always sees two diode voltage drops with no dead time, except for saturation where the load current is zero. Therefore, the power dissipation in these diodes must be accounted

$$P_{SWITCH} = 2\,I_{LOAD,avg} \cdot V_{DIODE}. \tag{12}$$

The core sees $V_{LOAD} + 2\,V_{DIODE}$ instead of V_{LOAD} alone. The rectification contributes to the effectively higher core voltage, so t_{SAT} from the first-order estimate is at least slightly overestimated. Fig. 10 illustrates the effect of real diodes in a rectifier. In this example with $I_P = 6.27\,A_{RMS}$ and $N = 200$, neither the FSC method nor the TWA method is applied. The P_{LOAD} versus V_{LOAD} response with nonideal diodes shifts to the left due to faster saturation, and is lowered by P_{SWITCH} due to diode loss. Note that P_{SWITCH} is generally different in every

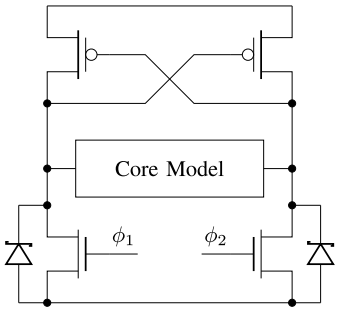

Fig. 11. Rectifier with active gate control.

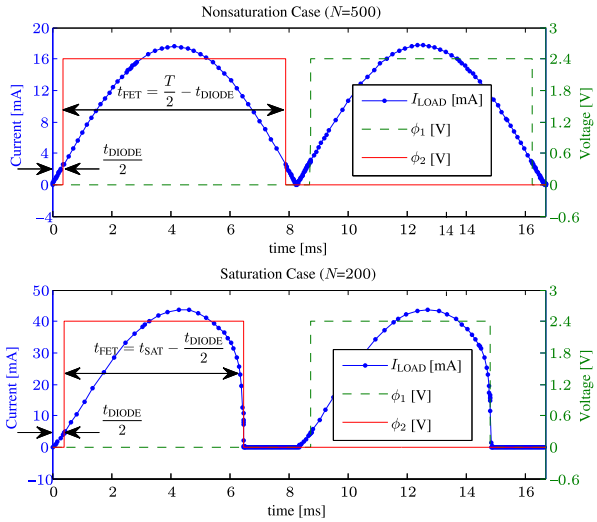

Fig. 12. ϕ_1 and ϕ_2 controls in two possible cases.

point along the $V_{\rm LOAD}$ axis, since $I_{\rm LOAD,avg}$ is affected by the level of core saturation.

In order to minimize this loss, active rectification can be used as shown in Fig. 11, which uses transistors instead of diodes for lower on-resistance. Once the appropriate switching devices are selected for the correct current path, the cross-coupled PFET pair reduces the switching loss by one diode stage loss without any burden on gate control efforts, because the load voltage connected to the core is also powering the PFETs consistently with the selected current path. However, since a FET is a bidirectional device, it cannot block backward conduction, and automatic switching of the current paths based on the cross-coupled pair itself is not possible. That is, unless externally controlled (by diodes, for example), the PFET turns off when $|V_{{\rm GS},p}|$ becomes lower than $|V_{{\rm TH},p}|$ regardless of the direction of the transformer current. Therefore, the voltage of the rectifier output will fall until the FET is in the cut-off region. This leads to power flow from the load into the core, and significantly undermines the power harvest. For this reason, cross-coupled pairs in both top and bottom cannot be used to completely eliminate gate control. (however, if the core is a voltage-driven transformer, complete elimination of the gate control is possible by using cross-coupled pairs in both positions, as shown in [15] and [16]).

This issue can be avoided by applying gate control ϕ_1 and ϕ_2 to the lower NFET pair. Alternatively, PFETs can be placed as a top pair with accordingly adjusted gate controls, and NFETs as

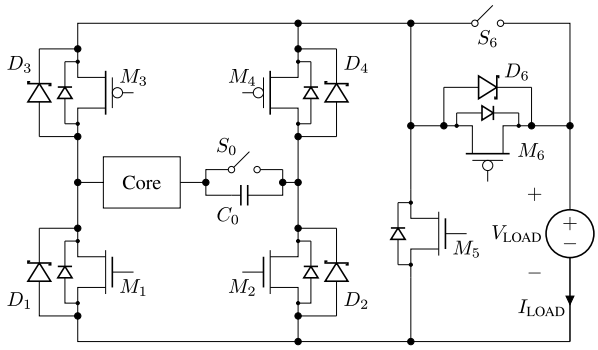

Fig. 13. Test board schematic.

a cross-coupled pair in the bottom. To avoid short circuiting, the output of the rectifier to ground through the FETs, it is required to ensure a finite-nonoverlap period between ϕ_1 and ϕ_2. During this period, the polarity crossover of the transformer current happens, and the switching of the current paths is automatically handled by the diodes. Denoting the diode operated duration, the FET operated duration, and the on-resistance of the FET as $t_{\rm DIODE}$, $t_{\rm FET}$, and $R_{\rm ds-on}$, respectively, the switching loss can be written as

$$\begin{aligned} P_{\rm SWITCH} = {} & V_{\rm DIODE} \cdot \frac{2}{T} \int_0^{t_{\rm DIODE}/2} I_{\rm LOAD}(t)\ {\rm d}t \\ & + R_{\rm ds-on} \cdot \frac{2}{T} \int_{t_{\rm DIODE}/2}^{t_{\rm DIODE}/2+t_{\rm FET}} I_{\rm LOAD}^2(t)\ {\rm d}t \\ & + V_{\rm DIODE} \cdot \frac{2}{T} \int_{t_{\rm DIODE}/2+t_{\rm FET}}^{t_{\rm DIODE}+t_{\rm FET}} I_{\rm LOAD}(t)\ {\rm d}t \\ & + R_{\rm ds-on} \cdot \frac{2}{T} \int_0^{T/2} I_{\rm LOAD}^2(t)\ {\rm d}t \end{aligned} \tag{13}$$

where

$$t_{\rm FET} = \min\left[t_{\rm SAT} - \frac{t_{\rm DIODE}}{2}, \frac{T}{2} - t_{\rm DIODE}\right]. \tag{14}$$

If the proposed active gate control method is applied to the peak point of the graph with dot marks in Fig. 10, where the nominal diode voltage drop ($V_{\rm DIODE}$) is 0.19 V in milliampere range using the same Schottky diode, and $I_{\rm LOAD,avg} = 22.07\,{\rm mA}$, the switching loss is decreased from 8.387 to 0.176 mW, which is 97.9% in reduction. Here assumed are $t_{\rm DIODE}/T = 5\%$ and $R_{\rm ds-on} = 0.1\,\Omega$. Compared to the power harvest with a diode rectifier providing $48.5\,{\rm mW}$, the active gate control increases the power harvest by 16.9%.

Fig. 12 illustrates two possible cases of ϕ_1 and ϕ_2 control based on the circuit of Fig. 11. The upper case illustrates a situation with sufficiently low $V_{\rm LOAD}$ that the core does not saturate during the entire cycle. The lower case exhibits saturation. In this case, the transformer current is going through the left PFET and the right NFET (ϕ_2) in the first half cycle, and then the right PFET and the left NFET (ϕ_1) in the second half cycle. When the core goes into saturation, both NFETs need to be turned off slightly before the actual saturation. Otherwise, one of the PFETs will be turned on due to the NFET providing a ground, and the saturated core would complete a short circuit

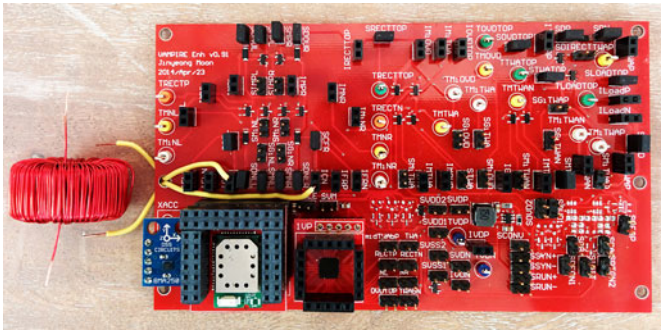

Fig. 14. Test board and the harvesting core (VAC W380).

TABLE II
OPERATION MODES OF THE TEST BOARD

Mode	Associated Devices in Each Mode						
Base (Diode Full-bridge)	S_0	D_1	D_2	D_3	D_4	–	S_6
Base + AR (Active Rectification)	S_0	M_1	M_2	M_3	M_4	–	S_6
Base + FSC	C_0	D_1	D_2	D_3	D_4	–	S_6
Base + TWA	S_0	D_1	D_2	D_3	D_4	M_5	M_6
Base + AR + FSC	C_0	M_1	M_2	M_3	M_4	–	S_6
Base + AR + TWA	S_0	M_1	M_2	M_3	M_4	M_5	M_6

path between the output and the ground by forcing zero voltage between two drain terminals of the turned-on transistors. Since this severely harms the power harvest, t_{FET} has a limit value of $t_{\mathrm{SAT}} - t_{\mathrm{DIODE}}/2$ in saturation (moreover, a small timing margin of several μs before the actual saturation needs to be allocated to avoid the short-circuit path in practice). To incorporate this with a nonsaturating case, the min function is used in (14).

D. Experimental Verification of the Proposed Methods

A prototype was constructed as shown in Figs. 13 and 14 to verify analytical predictions. By choosing appropriate devices along the current path and correctly adjusting necessary gate controls, single and combinatory operations of three methods are tested. Applying a constant voltage source as a load, measurements of the voltage across the load (V_{LOAD}) and the current through the load (I_{LOAD}) can be used to calculate power harvest. Note that PFET devices in the rectifier are generally represented as gate-controllable devices, as the cross-coupled mode can be thought as a special kind of active gate control. Small diodes next to FETs represent body diodes of the devices, and large diodes next to FETs indicate explicit Schottky diodes. Switches S_0 and S_6 are mechanical switches to bypass the FSC (C_0) or the devices used in the TWA method (D_6 and M_6) in which case M_5 is also turned off by gate control. Table II describes associated devices in each mode. Switches S_0 or S_6 described in a mode in Table II provide a short for bypass operation. For experimentation, the test board includes components that might not be needed in a final implementation. The test board includes a full set of components to explore experimental options for comparison to analytical predictions.

The test board also includes interfaces to digital sensor packages and a wireless radio package in addition to the power electronic circuits. Features added for testing increase the volume of the experimental prototype, but, of course, the practical dimensions of a real harvester application can be very small, close to the dimensions of the core itself as illustrated in [3, Fig. 1].

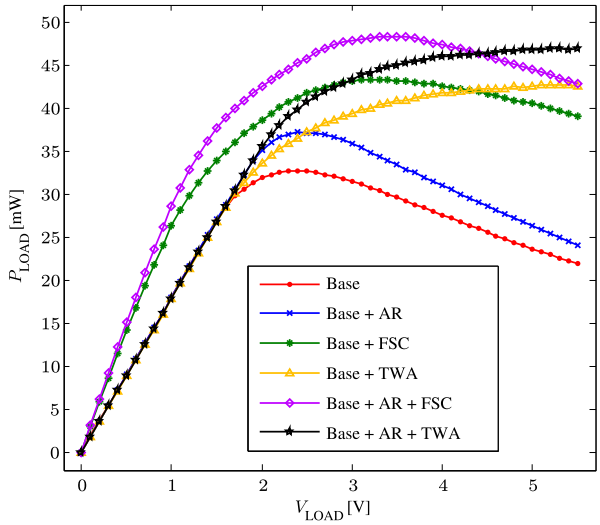

Fig. 15. Experimental results ($I_{\mathrm{P}} = 4.0\,\mathrm{A_{RMS}}$, $N = 200$).

Unselected FETs in a mode are turned off by appropriate gate signals, for example, M_1 and M_2 in "Base" mode will have logic-0 signals as gate inputs, while M_3 and M_4 will have logic-1 signals as gate inputs. Also, M_5 will be gated with logic-0 as the base case does not employ the TWA method.

Experimental results associated with different operating modes are illustrated in Fig. 15. The RMS current of the primary sinusoid is $I_{\mathrm{P}} = 4.0\,\mathrm{A_{RMS}}$, and the number of secondary windings is $N = 200$. Active rectification, if applicable, is performed with 95% utilization of active devices, and is performed even for the voltage range where V_{LOAD} is less than the minimum supply voltage of the microcontroller by using an external power rail for the microcontroller in such cases, even though these operating regimes may not be practical in real harvester applications. The results are included to show the full range of predictions. Microchip's PIC18F14K50 microcontroller [17] is used here, with a minimum supply voltage of 1.8 V. The Schottky diodes are PMEG2010ER by NXP Semiconductors [18], the PFETs are DMG3415U by Diodes Inc. [19], and the NFETs are PMV30UN by NXP Semiconductors [20].

Active rectification alone boosts the maximum power harvest from that of the "Base" case by 13.72%, from 32.71 to 37.19 mW. The peak harvest occurs at a slightly higher load voltage due to reduction in core voltage from elimination of diode voltage drops. Individually, both the FSC and the TWA methods greatly boost the maximum power harvest from the "Base" case by 32.47% and 30.57%, yielding maximum power harvests of 43.33 and 42.70 mW, respectively. As mentioned, the FSC method increases the power harvest in the nonsaturated region by acting as a power factor corrector, and as can be inferred from the figure, the maximum power harvest of the TWA method will be higher at higher V_{LOAD}. Finally, when combined with active rectification, the FSC and the TWA methods result in 47.81% and 43.60% increase to the maximum power harvest

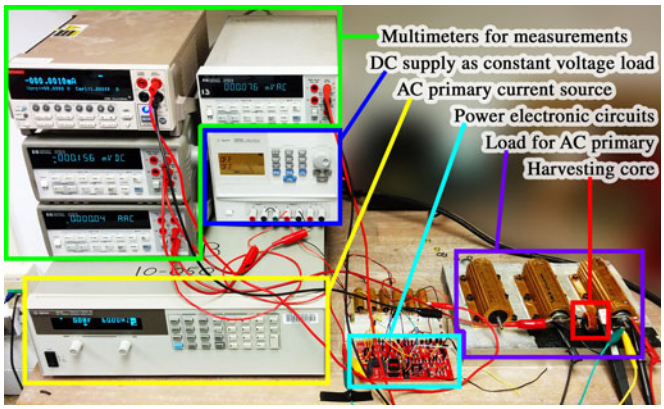

Fig. 16. Testing environment for power efficiency measurement.

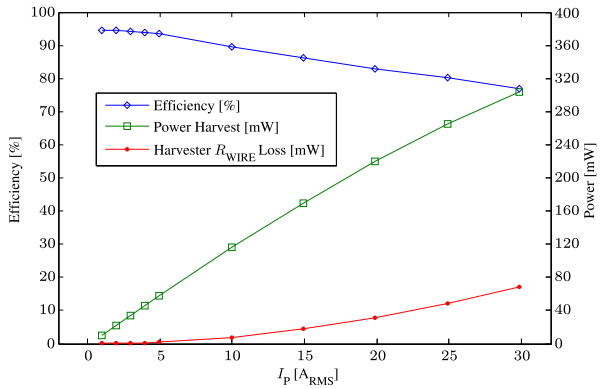

Fig. 17. Efficiency of the harvester across I_{P} ($V_{\mathrm{LOAD}} = 5.0\,\mathrm{V}$, $N = 200$, active rectification + TWA).

from the "Base" case, with actual maximum power harvests of 48.34 and 46.97 mW, respectively.

To demonstrate circuit performance, the most complex combination of the proposed methods (active rectification with the TWA method) was tested, and the performance of the experimental hardware was experimentally evaluated for primary currents ranging up to $I_{\mathrm{P}} = 30.0\,\mathrm{A_{RMS}}$. The testing environment is depicted in Fig. 16, and results are illustrated in Fig. 17. The *y*-axis on the right side of the plot represents the actual amount of power harvested, and the *y*-axis on the left side indicates power efficiency defined as a ratio of harvested power in the secondary to real power dissipated in the primary side due to the harvester. In the figure, the same amorphous nanocrystalline core was used with $N = 200$ and $V_{\mathrm{LOAD}} = 5.0\,\mathrm{V}$. The wire gauge for secondary windings is AWG28.

Equation (11) predicts that the power harvest will be directly proportional to I_{P}, and this is essentially true, staying linear up to a certain point ($I_{\mathrm{P}} = 10\,\mathrm{A_{RMS}}$) as shown in the figure. However, as I_{P} further increases, the power harvest clearly starts to develop a curvature, making the amount of power harvested less than ideal, due to a second-order effect that has been neglected so far, the dc resistance of the secondary windings. The gradual reduction in efficiency for increasing levels of primary current occurs because of t_{SAT}'s dependence on the primary-side current I_{P} as opposed to the assumption of total independence presented in the TWA analysis. Even with active rectification, t_{SAT} is shorter than ideal because there is always a voltage drop due to nonzero dc wire resistance. Normally the wire resistance is at most several ohms; therefore, the secondary core current of tens of milliampere does not cause severe deviation from the ideal linear graph. However, in cases of very high primary current, flux accumulation due to the voltage drop across the dc wire resistance can be significant compared to the main flux accumulation due to the load voltage, causing shorter t_{SAT}. An even more important point is that during the time where the core is intentionally shorted to prepare for the next transfer window, the voltage drop across the wire resistance is still seen by the core, and accelerates flux accumulation, directly reducing a major portion of t_{SAT}. This can be easily mitigated by using a thicker wire for the secondary windings. However, since the thickness of the windings impacts cost and the area of the free window in the center of the core, a careful choice is needed during design. Clearly, however, practically useful levels of energy can be harvested with wires as thin as AWG28.

E. Control Power

Startup and regulation circuits are required in a practical harvester, and their performance and impact on overall circuit operation is discussed here. Examples of power-efficient implementations for these circuits and functions are presented in [2], where their power dissipations are on a microwatt level. Since this is negligible to the milliwatt level harvesting as in this paper, the control power is essentially governed by the microcontroller.

For sensor applications, many relevant sensing problems will be well served by existing microcontrollers for collecting and processing sensor data. In our experiments, a microcontroller was used to time-division multiplex acquisition of sensor data and also power electronic control. Since the microcontroller runs at full frequency for sensing purposes, the power consumption added by generating gate controls for power electronic circuits was extremely small. Even if a new microcontroller is assumed for controlling power electronic circuits, the overhead is still low. In experiments conducted here, the power consumption of the microcontroller running at 8 MHz ranged from 2.63 mW (at 1.8 V) to 10.51 mW (at 5.5 V). Since the supply voltage of the digital circuits, including the microcontroller and sensor suites, is usually set to the lowest supply voltage to minimize the power consumption in real applications, the overhead of the entire microcontroller operations is at most 2.63 mW. Harvesting energy from the primary current of as low as $0.3\mathrm{A_{RMS}}$ is sufficient for sustaining the microcontroller, using the same core discussed previously.

V. Conclusion

This paper has presented a core model for accounting for saturation behavior in magnetic energy harvesters. This model is different from the model of [1] in that it does not require a custom numerical solver and is suitable for direct use in circuit simulators like SPICE. Compared to [1], appropriate model simplifications ease computational burden, and the model continues to show excellent accuracy across various I_{P} and N configurations, and on two different load types. This remains true even for cores with a large ratio of outer radius to inner radius.

Three new techniques to enhance the extraction of energy from a magnetic core are introduced and verified through

analyses, simulation, and experiments. The first involves a FSC. This capacitor, in series with the core, shapes the flux accumulation of the core in a convex manner with a lower starting point, lengthening the transfer window. The second approach uses switches to align the transfer window with the peak transformer current. By exploiting the core's indifference to the starting point of the transfer window, the load can be connected to the core when the load can receive the maximum power during the transfer time segment. The third technique uses an active rectifier to minimize losses where appropriate for the harvester application. This drastically reduces the switching loss, and realizes the circuit environment as if ideal diodes are used, as done in the transfer window analysis.

In practice, the harvester is likely to face one of three cases for the primary current. First is when the RMS current in the primary side is well defined, and does not change much. In this case, a fixed FSC can be used reliably, eliminating control efforts. Second, the primary current may exhibit substantial change over time, and a microcontroller is likely to be available as part of the sensor package powered by the harvester. In this case, the TWA method permits adaptive control of the transfer window to optimize power transfer, much like finding the maximum power point for a solar panel. Of course, if a controller cannot be deployed, a basic rectifier with two diodes and two cross-coupled FETs can be used without enhancement to harvest some power. Combining the active rectification with any of the two methods, FSC or TWA, may also be desirable for higher power harvest. Moreover, for high power applications, the thickness of the core windings must be carefully considered so that the width of the transfer window is not much affected by the level of the primary current.

ACKNOWLEDGMENT

The authors would like to thank D. Nalchajian for guidance.

REFERENCES

[1] J. Moon, S. Leeb, "Analysis model for magnetic energy harvesters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, Aug. 2015.
[2] J. Moon, S. Leeb, "Power flow control and regulation circuits for magnetic energy harvesters," in *Proc. IEEE 15th Workshop Control Model. Power Electron.,* Jun. 2014, pp. 1–8.
[3] J. Moon, J. Donnal, J. Paris, S. Leeb, "VAMPIRE: A magnetically self-powered sensor node capable of wireless transmission," in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 3151–3159.
[4] F. Simjee and P. Chou, "Everlast: Long-life, supercapacitor-operated wireless sensor node," in *Proc. Int. Symp. Low Power Electron. Des. ACM*, 2006, pp. 197–202.
[5] P. Stanley-Marbell and D. Marculescu, "An $0.9 \times 1.2''$, low power, energy-harvesting system with custom multi-channel communication interface," in *Proc. Conf. Des., Autom. Test Eur. Consortium*, 2007, pp. 15–20.
[6] M. Minami, T. Morito, H. Morikawa, and T. Aoyama, "Solar biscuit: A battery-less wireless sensor network system for environmental monitoring applications." in *Proc. 2nd Int. Workshop Netw. Sens. Syst.*, 2005.
[7] S. Sudevalayam and P. Kulkarni, "Energy harvesting sensor nodes: Survey and implications," *IEEE Commun. Surv. Tuts.*, vol. 13, no. 3, pp. 443–461, Jul.–Sep. 2011.
[8] S. Meninger, J. Mur-Miranda, R. Amirtharajah, A. Chandrakasan, and J. Lang, "Vibration-to-electric energy conversion," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 9, no. 1, pp. 64–76, Feb. 2001.
[9] G. Ottman, H. Hofmann, A. Bhatt, and G. Lesieutre, "Adaptive piezoelectric energy harvesting circuit for wireless remote power supply," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 669–676, Sep. 2002.
[10] A. Fowler, S. Moheimani, and S. Behrens, "A 3-DoF MEMS ultrasonic energy harvester," in *Proc.IEEE Sens. Conf.*, Oct. 2012, pp. 1–4.
[11] J. Paradiso and T. Starner, "Energy scavenging for mobile and wireless electronics," *IEEE Pervasive Comput.*, vol. 4, no. 1, pp. 18–27, Jan. 2005.
[12] I. Stark, "Thermal energy harevsting with thermo life," in *Proc. IEEE Int. Workshop Wearable Implantable Body Sens. Netw.*, Apr. 2006, pp. 19–22.
[13] Y. Tan and S. Panda, "Energy harvesting from hybrid indoor ambient light and thermal energy sources for enhanced performance of wireless sensor nodes," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4424–4435, Sep. 2011.
[14] D. Brunelli, C. Moser, L. Thiele, and L. Benini, "Design of a solar harvesting circuit for battery less embedded systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 11, pp. 2519–2528, Nov. 2009.
[15] A. Facen and A. Boni, "Power supply generation in CMOS passive UHF RFID tags," in *Proc. 2nd Conf. Ph.D. Res. Microelectron. Electron.*, Jun. 2006, pp. 33–36.
[16] S. Mandal and R. Sarpeshkar, "Low-power CMOS rectifier design for RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 6, pp. 1177–1188, Jun. 2007.
[17] Microchip Technology Inc. (2010, Nov. 2). *PIC18F/LF1XK50 20-Pin USB Flash Microcontrollers With NanoWatt XLP Technology.* [Online]. Available: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en533924
[18] NXP Semiconductors. (2008, Dec. 29). *PMEG2010ER 1A Low V_F MEGA Schottky Barrier Rectifier* [Online]. Available: http://www.nxp.com/products/automotive/discretes/schottky_rectifiers/PMEG2010ER.html
[19] Diodes Inc. (2014, Feb. 20). *DMG3415Y P-Channel Enhancement Mode MOSFET.* [Online]. Available: http://diodes.com/catalog/p_channel_20v_145/dmg3415u.html
[20] NXP Semiconductors. (2003, Jun. 25). *PMV30UN μTrenchMOS Ultra Low Level FET.* [Online]. Available: http://www.nxp.com/products/mosfets/standard_mosfets/PMV 30UN.html

Jinyeong Moon (S'12) received the B.S. degree in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2005, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2007. He is currently working toward the Ph.D. degree in electrical engineering and computer science at the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA.

He was with Hynix Semiconductor Inc. from 2007 to 2011 as a Senior Research Engineer, designing circuits for DDR4 SDRAM. Since 2011, he has been affiliated with the Research Laboratory of Electronics and the Laboratory for Electromagnetic and Electronic Systems, MIT. His research interests include modeling, design, and analysis of circuits and systems in the fields of power conversion, energy harvesting, electromagnetics, and renewable energy. He has authored 17 registered U.S. and international patents.

He received the Kwanjeong Scholarship in 2011. He was the grand prize winner of the MIT Clean Energy Prize in 2014, and he received the Hynix Strategic Patent Award in 2010.

Steven B. Leeb (S'89–M'91–SM'01–F'07) received the Ph.D. degree from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 1993.

He served as a Commissioned Officer with the USAF Reserved. He has been a Member with the MIT faculty at the Department of Electrical Engineering and Computer Science, since 1993. He also holds a joint appointment with the MITs Department of Mechanical Engineering. He currently serves as a MacVicar Fellow and a Professor of electrical engineering and computer science at the Laboratory of Electromagnetic and Electronic Systems. In his capacity as a Professor at MIT, he is concerned with the design, development, and maintenance processes for all kinds of machinery with electrical actuators, sensors, or power electronic drives. He is the Author or the coauthor of more than 100 publications and 15 U.S. patents in the fields of electromechanics and power electronics.