Fast Controller for a Unity-Power-Factor PWM Rectifier

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***Abstract*— This paper presents an analog implementation of a fast controller for a unity-power-factor (UPF) PWM rectifier. The best settling times of many popular controllers for this type of converter are on the order of a few line cycles, corresponding to bandwidths under 20 Hz [1]. The fast controller demonstrated in this paper can exercise control action at a rate comparable to the switching frequency rather than the line frequency. In order to accomplish this while maintaining unity power factor during steady-state operation, the fast controller employs a ripple-feedback cancellation scheme.**

I. Introduction

CONVENTIONAL ac/dc power converters that are connected to the line through full-wave rectifiers draw a nonsinusoidal input current. Harmonic content in a current waveform flowing through the impedances in the electric utility distribution system can create harmonic voltages. These harmonics distort the local voltage waveform, potentially interfering with other electrical equipment connected to the same electrical service [2]–[4]. Also, a distorted input current waveform prohibits the extraction of the maximum possible real power from the utility service. Unity-power-factor converters (UPF) employ active waveshaping of the input current to ensure a sinusoidal current shape, while delivering a dc output voltage. The primary tasks of a controller for a UPF converter are to:

- achieve high power factor during steady-state operation with a constant load;
- maintain an output voltage waveform $v_o(t)$ around a specified average value $V_o(t)$ with low ripple;
- respond quickly to load disturbances; and
- with a modest implementation effort, provide robust performance in the presence of uncertainties in component values and operating conditions.

Some of these goals are conflicting, e.g., speed of response versus robustness, and we will comment on trade-offs in the following sections. Typical control schemes employed in state-of-the-art UPF converters have fairly low bandwidth in order to limit the impact of output voltage ripple on input power factor. In such controllers, disturbances are attended by control actions taken at most on the order of twice per line cycle.

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The fast controller presented here exercises control action at a much faster rate. As a result, the fast controller achieves a much smaller response time to disturbances. A key feature of this controller is its ability to reject feedback of the ripple on the bus capacitor by actively canceling it, so that high-bandwidth control can be maintained without distorting the input current during steady-state operation. Several control techniques for the boost UPF converter that employ active output voltage ripple cancellation have been reported in the literature; see [5] for a recent example. The controller described in this paper is unique in that it additionally facilitates very high bandwidth voltage loop control. A large-signal periodically varying *linear* model of a UPF boost converter serves as the basis for the design of the fast controller. The large-signal linear model permits reliable, well characterized control action in the presence of large deviations from a nominal operating point, which is not the case for controllers designed on the basis of a small-signal model.

The need for a fast, large-signal linear controller for UPF converters will increase. Power supplies with actively shaped input currents are a popular way to meet desirable or mandated [4] power quality standards. With the rapid proliferation of uninterruptible power supplies, output voltage hold-up time requirements are decreasing for UPF power supplies in loads such as personal computers and workstations. Large value bus capacitors used in conventional UPF converters could conceivably be replaced with smaller, less expensive capacitors. The fast controller provides sufficient control bandwidth to maintain comparable dynamic response in the presence of load changes, even with a substantially reduced level of energy storage at the output bus. Furthermore, while low-bandwidth controllers are adequate for *regulation* applications, they may have entirely inadequate *tracking* performance. In a regulation application, the UPF controller is tasked with maintaining the average output voltage at a fixed, unchanging reference point. This situation is typical, for example, in a computer with a point-of-load, distributed power supply system with a UPF converter serving as the utility interface. In tracking applications, the UPF controller causes the average output voltage to follow or track a desired reference waveform as a function of time or some other variable. Consider, for example, a UPF converter serving as part of an electric vehicle battery charger. In a charging application, unity power factor operation is essential to ensure maximum power delivery and the fastest possible charging. Depending on the battery, the charger may be required to follow large changes in

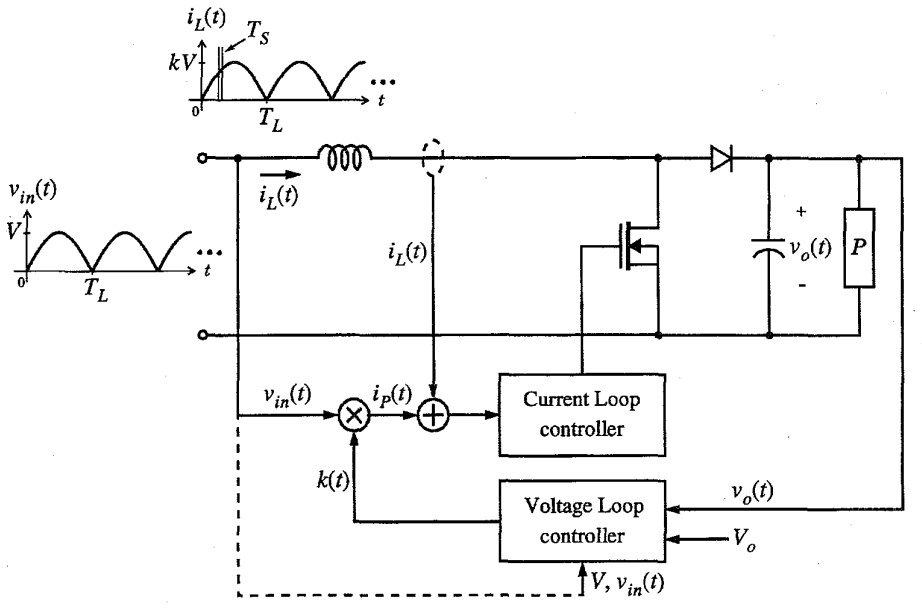

Fig. 1. A unity-power-factor ac/dc switching preregulator.

an output voltage reference. In advanced battery systems requiring pulsatile charging profiles, these changes may also be rapid. A high-bandwidth, large-signal linear UPF controller could be essential in such applications.

II. System Operation and Modeling

A popular scheme for implementing a UPF utility interface is based on a boost converter, as shown in Fig. 1. The inner current loop controls the inductor current (input current) to the shape and phase of the input voltage, $v_{\text{in}}(t) = V|\sin(\frac{\pi t}{T_L})|$, where T_L denotes the period of the rectified line voltage. The switching sequence for the controllable switch forces the local average of the inductor current $i_L(t)$ to essentially equal the commanded current $i_p(t)$, where this local average is computed over the switching period, T_S. The current $i_p(t)$ is made proportional to the input voltage, $i_p(t) = k(t)v_{\text{in}}(t)$, in order to obtain essentially unity power factor. The voltage loop or outer loop in turn regulates the average output voltage by appropriately adjusting $k(t)$ to vary the amplitude of the commanded current and, hence, the amplitude of the input current. In the conventional approach, the average output voltage is evaluated over a sliding interval of length T_L, and the reference value for this T_L-averaged output voltage is a constant, V_o. The corresponding variation in $k(t)$ typically occurs at the maximum rate of once per rectified line cycle [6]. In contrast to the conventional approach, the fast controller designed and implemented here instead regulates the local, T_S averaged voltage around an appropriate *periodically varying* reference, with $k(t)$ allowed to vary significantly within each line cycle.

III. System Modeling and Control Design

As outlined in [7], the development of the large-signal, linear, fast controller begins with a model of the UPF converter based on a power balance equation. The model assumes that the current loop is working ideally (i.e., $i_L = i_p$) and ignores the ripple at the switching frequency, i.e., the model deals with the local averages of variables over one switch period, which we have already referred to as T_S-averaged values. The fact that a "power" balance holds for T_S-averaged quantities follows directly from Tellegen's theorem [8]. The desired power balance equation is

$$\frac{1}{2}C\frac{dv_o(t)^2}{dt} = k(t)v_{\text{in}}^2 - \frac{1}{2}L\frac{d(k^2(t)v_{\text{in}}(t)^2)}{dt} - P \quad (1)$$

where we have assumed a constant-power load, P; other loads, e.g., a resistive load, can be incorporated into the modeling, but are omitted here (see [9] for more details). We have used $v_o(t)$ to denote the T_S-averaged output voltage and have also taken the T_S-averaged version of $v_{\text{in}}(t)$ to be approximately $v_{\text{in}}(t)$ itself. To transform this T_S-averaged model to a state-space form, we define the state variable

$$y(t) = v_o^2(t) + \frac{L}{C}k^2(t)v_{\text{in}}^2(t). \quad (2)$$

Substituting this choice of state variable in (1) results in a state-space model that, although periodically varying, is *linear*

$$\dot{y}(t) = \frac{2v_{\text{in}}^2(t)k(t)}{C} - \frac{2P}{C}. \quad (3)$$

The energy stored in the inductor is typically small compared to the energy stored in the capacitor. As a result, $y(t) \approx v_o^2(t)$, and we can make the approximation that the nominal or desired trajectory, $Y_d(t)$, for the quantity $y(t)$ can be expressed in terms of a desired output voltage waveform $v_{od}(t)$

$$Y_d(t) \approx v_{od}^2(t). \quad (4)$$

If a constant T_L-averaged output voltage V_o is desired, it can be shown [7] that

$$Y_d(t) \approx V_o^2 - \frac{2P}{C\omega_2}\sin(\omega_2 t) \quad (5)$$

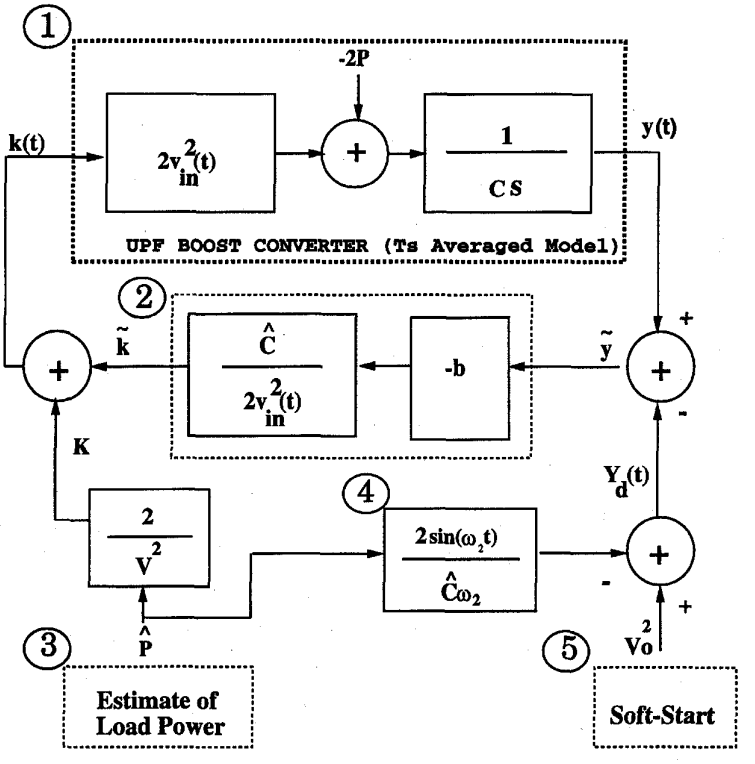

Fig. 2. Block diagram.

where ω_2 is the output ripple frequency (twice the line frequency) given by $2\pi/T_L$, with T_L denoting the period of the rectified line input. With the T_S-averaged model, therefore, the nominal output voltage is not just a dc term. Instead, the nominal output consists of a desired dc voltage, V_o, plus an unavoidable ac ripple due to the finite size of the bus capacitor.

IV. Control Design

One approach to the compensation of a time-dependent system is to choose feedback gains that vary with time, so that the overall closed-loop system is time-independent. For the UPF boost converter, we propose the control law $k(t) = \tilde{k}(t) + K$. The feedforward component K guarantees unity power factor in the steady-state and is given by

$$K = 2P/V^2 \tag{6}$$

where V represents the peak input voltage. The term $\tilde{k}(t)$ serves to respond to deviations in the output voltage and to cancel out the time-varying term in (3)

$$\tilde{k}(t) = -\frac{C}{2v_{\text{in}}^2(t)} b\tilde{y}(t) \tag{7}$$

where $\tilde{y}(t) = y(t) - Y_d(t)$ and b is a constant selected by the designer to achieve a desired closed-loop transient response. Substituting this choice of $k(t) = \tilde{k}(t) + K$ into (3) yields a closed-loop system governed by the following linear and time-invariant equation

$$\dot{\tilde{y}}(t) = -b\tilde{y}(t). \tag{8}$$

Schemes in which (1) is averaged over at least T_L, and where $k(t)$ is assumed essentially constant over a rectified line cycle [6] yield controllers that have inherently lower achievable closed-loop bandwidths than are possible with the above fast controller. The fast controller, which incorporates a periodically varying feedback gain, can achieve a significant decrease in the transient response time.

Fig. 2 shows a block diagram of the UPF converter with the fast controller. Box 1 contains the blocks that represent the T_S-averaged state-space model (3) of the converter. The sequence of blocks in Box 2 takes as input the error $\tilde{y}(t)$ and computes $\tilde{k}(t)$, the periodically varying feedback gain of (7) that yields a time-invariant closed-loop system. Fast response to disturbances is achieved through careful selection of the constant b. In addition to $\tilde{k}(t)$, the controller computes the constant K of (6) from a feedforward estimate of the load power (Box 3) and a feedforward measurement of the RMS input voltage, making the controller insensitive to changes in both. The constant K is computed to guarantee UPF operation in the steady-state.

The fast controller employs active cancellation to prevent feedback of the ripple voltage on the bus capacitor. The computation indicated in Box 4 determines the nominal trajectory for $y(t)$ according to (5).

Finally, the controller requires a dc reference, shown in Box 5, to set the average component of the desired output voltage, i.e., V_o in (5). The hardware prototype, to be discussed in detail in the next section, incorporates a soft-start circuit to gradually build this average component of the desired output

voltage during the turn-on transient. This soft-start protects components in the boost converter from excessive stress during start-up, when the controller is correcting for a large initial error.

V. Hardware Implementation

A hardware prototype of the fast controller has been constructed and tested [9]. For convenience in developing the prototype, the inner current loop and parts of the outer voltage loop were implemented with a Unitrode power factor correction (PFC) controller chip (UC3854) [10]. While not intended to serve as a fast UPF controller, a UC3854 can be augmented with additional circuitry to implement a fast analog controller. Our prototype serves, therefore, not only to illustrate the performance of the fast controller in practice, but also to show how useful customizations may be made to off-the-shelf commercial components.

The hardware implementation of Block 1 in Fig. 2, with $k(t)$ as input and $y(t)$ as output, is realized in the prototype with the UC3854 PFC IC and a 250 W boost converter circuit. On the input side, the UC3854 incorporates a multiplier block that computes the current reference $i_p(t)$ for the inner current loop from a scaled measure of the input voltage and the output of the fast controller, $k(t)$. The output of the IC directly controls the power MOSFET switch in the boost converter.

As mentioned previously, the fast controller utilizes a periodically varying feedback gain to counteract the time varying component of the T_S-averaged model of the UPF converter. This gain, shown as the output of Block 2 of Fig. 2, is primarily calculated outside of the UC3854 by squaring a measure of the line voltage and using an analog divider to compute the reciprocal. Final computation of this time varying term is completed inside the UC3854, which scales its input command by dividing by the square of the RMS input voltage.

Equation (1) assumes a constant-power load at the output of the converter. This assumption is reasonable because the UPF converter is often employed in a system in which one or more regulated switching power supplies comprise the load. In testing the actual implementation, a resistive load was used for convenience. As noted earlier, a resistive load could have been incorporated into the analysis and design; see [9] for a development of the power balance model and fast controller in the presence of a resistive load. The satisfactory performance of our controller reflects the robustness of the fast controller to load model assumptions. This robustness is partly the result of the use of a measured load power in the prototype controller. In order to calculate the load power (Block 3 of Fig. 2), the average load current was calculated by measuring the voltage across a current-sense resistor in series with the resistive load. The load power was then calculated by multiplying the load current with a scale factor representing the average load voltage.

The ripple on the output voltage is essentially sinusoidal with a frequency of 120 Hz, corresponding to double the line frequency. The fast controller prototype uses a convenient estimate of this ripple to actively cancel out its distorting effect on the input current in the steady-state. The sinusoid required to generate the ripple component of Y_d in (5), see Block 4 of Fig. 2, is calculated by squaring a measure of the 60-Hz line voltage, eliminating the dc offset, and then using an all-pass filter to ensure the correct phase.

The hardware prototype also incorporates a soft-start mechanism during the initial start-up transient, when the error between the desired voltage and the actual voltage is large. The key features of Block 5 in Fig. 2 include the following:

- a voltage reference, derived from an internal precision reference available on the UC3854, that sets the desired steady-state bus voltage;
- an additive offset signal that accounts for the rectified line voltage present on the boost bus capacitor before boost operation can commence; and
- an RC circuit with a gradually rising output voltage that sets the reference during the start-up transient. The RC circuit is used in conjunction with a diode clamp that ultimately locks the reference at a steady-state value.

Empirical results from the hardware prototype are presented in the next section.

VI. Experimental Results

The component values used in the boost converter in the prototype are $C = 47$ μF, $L = 1$ mH. The input voltage to the converter for the tests described in this section was $v_{\text{in}}(t) = 165|\sin(\frac{\pi t}{T_L})|$, with $T_L = 8.333$ ms. The steady-state voltage reference was set to provide a nominal output voltage of $V_o = 350$ V to a resistive load. The performance of the prototype was examined during two different transient conditions: a start-up transient and a doubling in load power.

The experimental UPF converter was activated in our experiments by first energizing the main supply to the boost converter. With no active control, the output voltage rises to slightly under the peak input voltage, and the input current to the boost converter is, of course, noticeably distorted. The fast controller was then activated, and the output voltage regulated by the controller to the desired average of 350 V. As expected, the input current in steady-state is in phase and of the same shape as the input voltage. Fig. 3 shows the start-up response of the fast controller. The input current (lower trace) rises to a steady-state value of approximately 0.4 A peak. The load voltage (upper trace) rises to the desired steady-state voltage of 350 V. In Fig. 3, and also in Figs. 4 and 5, output voltages are plotted at 50 V per division, and input currents are plotted at 0.5 A per division.

Fig. 4 shows the response of the controller to an approximate doubling of the load power. The output voltage (upper trace) starts to dip while the controller commands more current to match the new output power requirement. The lower trace in Fig. 4 shows the input current during the transient. The maximum current during this transient is approximately 0.7 A peak. As expected, the ripple on the output voltage is higher at the new power level.

Note that the fast controller only ensures a distortion-free input current waveform during steady-state operation. This is illustrated in Fig. 5, which shows that before and after a transient the current (lower trace) is of the same shape as the input voltage, whereas during the transient, it is distorted. In

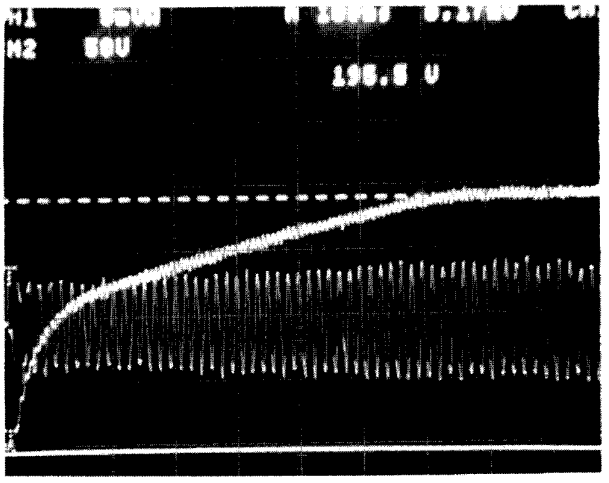

Fig. 3. Start-up transient.

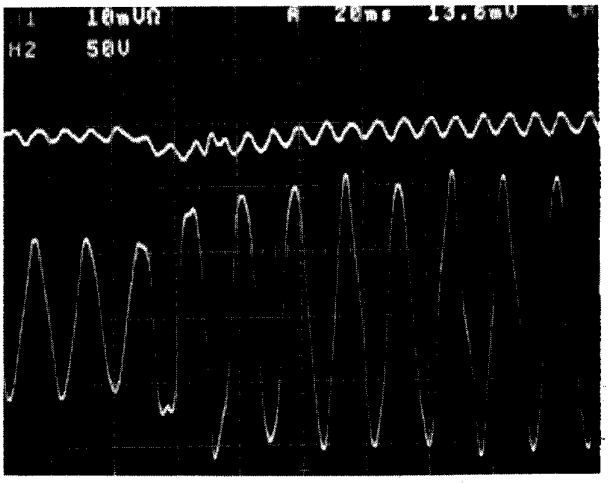

Fig. 5. Distortion of input current during a doubling of load power.

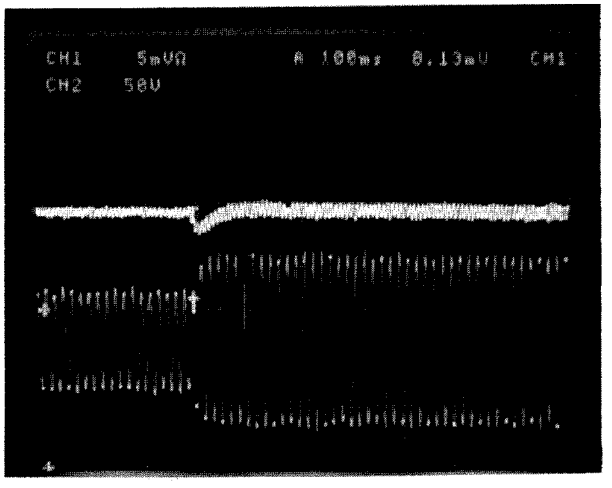

Fig. 4. Response of fast controller to a doubling of load power.

the steady-state, $\tilde{k}(t)$ is zero and the input current is a scaled copy of the input voltage. The upper trace in Fig. 4 shows the output voltage during the transient.

A point of interest in these experiments is the size of the bus capacitor. The relatively small bus capacitance (approximately one-tenth the bus capacitance used in the design example in [10]) incorporated in the prototype is not a problem for the fast controller because its active ripple feedback cancellation scheme allows the controller to prevent the feedback of the output voltage ripple. The insensitivity of the fast controller to output voltage ripple permits good regulation of the dc component of the output voltage even with very small bus capacitors. By enabling the use of a small bus capacitor, the fast controller can potentially reduce the overall cost of a UPF converter.

VII. Robustness Issues and Adaptive Control

Unlike classical linear time-invariant (LTI) controllers, the fast controller employs a periodically varying feedback gain and a feedforward estimate of the load power. In principle, the fast controller can achieve zero steady-state error in the output state variable $y(t)$. However, the fast controller is sensitive to computation errors in the feedback gain and also to measurement errors in the feedforward estimate of the load power. Inaccurate measurements could result in an erroneous Y_d, since the ripple component would not match the ripple on the output voltage, causing the controller to regulate the output voltage to an incorrect "desired" trajectory. More important, this represents a transient state for the controller in which the input current is distorted by the periodically varying gain. As a result, unity power factor would be compromised. An alternative solution would be to regulate the dc component of the output voltage with an appropriate LTI compensator, such as a proportional-integral controller, to guarantee zero steady-state error and to use a second faster control loop to regulate the ripple on the output voltage.

If the available estimate $\hat{C}$ does not agree with the actual value of C, but the feedback gain b is relatively small in comparison to the line input frequency, then the response of the system to perturbations in $v_o(t)$ is relatively sluggish. In this case, the input current waveform will not be distorted and the feedfoward of load power will take care of steps in $P(t)$ to ensure appropriate steady-state operation. If, on the other hand, b is relatively large, i.e., the feedback loop is faster, then the ω_2 component of the desired trajectory Y_d will be inadequate to cancel observed output ripple. The fast feedback loop will be forced to follow an incorrect reference signal, resulting in distorted input current waveforms.

A solution to this problem is to build a real-time estimator for $\hat{C}$ and then to use the estimated value in computing the control input $\tilde{k}(t)$, enabling faster closed loop control response without steady-state input current distortion. In [7] and [11], a recursive least-square-error estimator for the bus capacitance based on the amplitude

$$\epsilon \approx \frac{P}{\omega_2 V_o C}$$

of the output voltage ripple is presented and analyzed. This technique is demonstrated in [7] to allow substantial im-

provement in the closed loop response, even in the presence of significant capacitance uncertainty. Particularly for a T_S-based controller implemented in digital hardware, addition of a parameter estimator might be an advantageous alternative requiring little increase in overall controller complexity.

VIII. Conclusion

In this paper, we have presented a novel control scheme designed on the basis of a periodically varying, large-signal linear model of a unity-power-factor ac/dc converter. The prototype presented here employed a controller with a periodically varying feedback gain and a feedforward estimate of the load power and demonstrated fast response to load disturbances. The fast controller's unique ability to reject the feedback of the bus capacitor ripple facilitates the reduction of the output bus capacitor. As a result, a cheaper UPF boost converter with superior transient response could replace many current designs.

The high closed-loop control bandwidths made possible by the fast controller make it an ideal choice for use in tracking problems where the average output voltage is required to follow a reference with a time varying average component. We anticipate exploring in the near future a digital implementation of a fast UPF controller intended for tracking applications. A digital implementation will also facilitate the exploration of adaptive fast control but will also require the examination of quantization and other effects on the fast controller.

Acknowledgment

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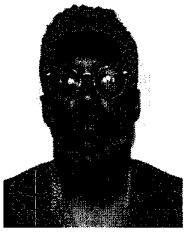

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