An Energy Buffer for Controllable Input Impedance of Constant Power Loads

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***Abstract*—Power electronic circuits often regulate load power and present a constant power profile to the utility or other electrical source. These constant power loads therefore exhibit a negative incremental input impedance and pose stability challenges when present in either dc or ac systems. This paper presents an energy buffer power converter for a constant power LED lighting load that presents a controllable input impedance to the electrical source. The use of an energy buffer allows the converter to independently control input and output power. The input power is controlled to resemble a resistive load, ensuring that the device exhibits a positive incremental input impedance over short-term input disturbances. Simultaneously, the output power is held constant through high-bandwidth regulation. The control scheme balances the power flow in the long term. Experimental results are presented that demonstrate independence between input and output performance, as well as long-term power balance.**

***Index Terms*—Energy storage, light-emitting diodes, negative resistance devices, power converter, stability.**

I. Introduction

CONSTANT power loads (CPLs) are significant power consumers on the electric grid. For example, actively controlled components of HVac systems can demand constant power from the utility over certain time intervals, as can uninterruptible power supplies. Modern fluorescent and solid-state lighting loads often present a constant power profile to the electrical source. Fig. 1 shows a converter that is designed to supply constant current to a fixed resistive load, in turn supplying it with constant power. The consequence, however, is that if there is a decrease in input voltage, the power converter responds by increasing input current demand. The resulting negative incremental input impedance can cause unstable performance unless certain stability criteria concerning CPLs in dc and ac systems are met [1]–[4]. Adding sufficient damping or active stabilization can help meet these criteria and stabilize the system when interfacing with the source [5]–[8].

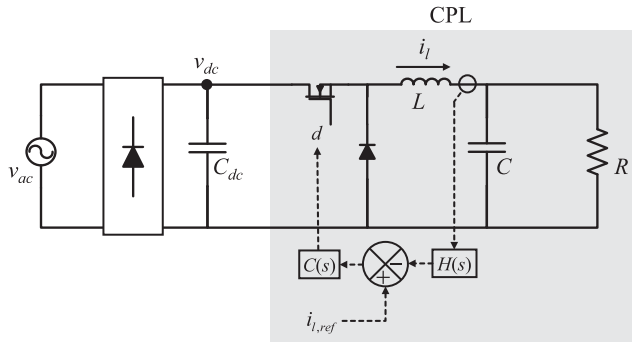

Fig. 1. Averaging filter $H(s)$ and compensator $C(s)$ allow a step-down power converter to supply constant current to a fixed load. The converter behaves as a CPL, and it exhibits negative incremental input impedance.

The power converter presented in this paper further explores lighting applications. The stability concern of lighting CPLs is currently relevant in smaller multi-converter systems, such as those found in automotive settings [9]. This paper presents a control strategy for an electronic energy buffer that maintains constant output power to an LED load while making more reasonable, relaxed demands for input power over the short time intervals of a utility disturbance. The light output of the LED lamp is impervious to input voltage fluctuations, but by controlling the input to resemble a resistive load, the need for significant passive damping or active stabilization can be minimized in stabilizing the CPL.

The presented converter and its application are an example. There are many ways to implement the power electronics, as well as uses for such an energy buffer [10]. A key point here is the control scheme, which enables regulated load operation, reduces transient requirements on the input power, and can be applied to many different circuit configurations. Here, the lighting driver presented as an example consists of two cascaded stages separated by an energy buffer. A boost step-up stage is designed to ensure that the lamp input mimics a resistive load for slow input voltage disturbance frequencies, while a buck

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step-down stage implements aggressive feedback control to provide constant power to the lighting load for constant, flicker-free operation. A capacitor between the two stages serves as the energy storage element. It buffers short-term input and output power imbalances with a combination of analog and digital active control.

In this paper, we present our design process by first analyzing energy flow in the converter. Then, linearized small-signal models are used to analytically design the controllers. We then present test results and performance data of the prototype lamp.

Mathematical Notation

1) Large-signal dc quantities are denoted by capital letters, e.g., $Y_{\rm in}$.
2) Constant quantities or parameters are also denoted by capital letters.
3) A small-signal quantity is denoted by a hatted lowercase letter, e.g., $\hat{y}_{\rm in}$.
4) A total quantity, comprised of both large-signal and small-signal quantities, is denoted by a lowercase letter, e.g., $y_{\rm in} = Y_{\rm in} + \hat{y}_{\rm in}$.

II. Power Flow and Energy Buffering

Different load types present different input impedances to the source. This section compares three load types, their small-signal incremental impedances, and discusses the instability concerns caused by CPLs. Then, from the perspective of an energy balance, we describe power converter operation that mitigates transient input power demands while still providing constant output power.

A. Power Profiles

Consider the range of different load behaviors for loads operating around a nominal input voltage V_0. For example, a resistive load, e.g., an incandescent lamp, obeys Ohm's law so that the load's power p_r relates to its resistance R and the supplied voltage v as

$$p_r = \frac{v^2}{R}. \tag{1}$$

Alternatively, a constant current load demands constant current I, and consumes power proportionally to the supplied voltage. Finally, a CPL consumes constant power $P_{\rm cpl}$, and the supplied voltage and load current i follow an inverse relationship as

$$P_{\rm cpl} = vi. \tag{2}$$

Each of these loads presents an incremental admittance when operating at some nominal voltage and current V_0 and I_0 as

$$\hat{y}\,(V_0, I_0) = \left.\frac{di}{dv}\right|_{(V_0, I_0)}. \tag{3}$$

For resistive loads, the incremental admittance is $\frac{I_0}{V_0}$, while for constant current loads, it is zero. For CPLs, noting that $P_{\rm cpl} = V_0 I_0$, the incremental admittance is $-\frac{I_0}{V_0}$. The incremental resistance is $-R_0 = -\frac{V_0}{I_0}$, negative that of a resistive load with the same operating point. While the negative resistance could be canceled out by placing a resistance greater than R_0 in series with the CPL, this would dramatically increase losses by effectively doubling power consumption.

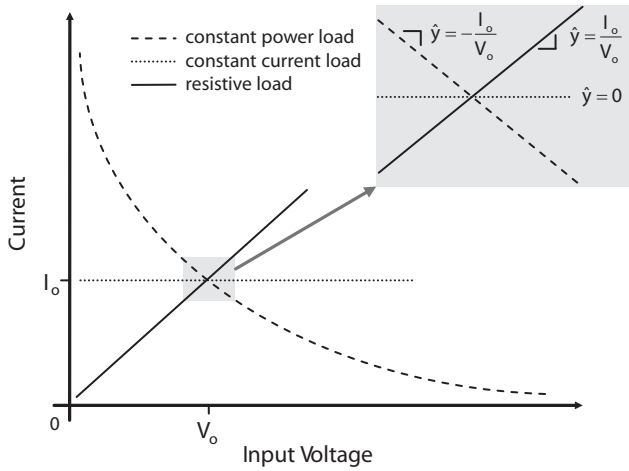

Fig. 2. Incremental admittances for different load types.

Fig. 2 shows the operating point and incremental admittances for the three load types. Since the CPL has an inverse I–V characteristic, its incremental admittance is negative. A load that exhibits a negative incremental impedance can destabilize a dc or ac system. For dc systems, stability criteria can determine the level of CPL penetration, which will cause instabilities [11], [12]. In ac systems, CPLs generally interface through either a passive or active rectifier. Nonlinear operation of the rectifiers can complicate a stability analysis. However, under certain scenarios, there are methods that can be applied to determine the stability criteria [13]–[15]. Mitigating constant power demand tends to stabilize an ac system [1], [16]. Our goal in this paper is to demonstrate an approach for providing a selectable or programmable input behavior over short times while maintaining load regulation.

B. AC Power to Rectified Loads

Loads with single-phase passive bridge rectifiers draw distorted current waveforms from the ac system if power factor correction (PFC) is not implemented. This can make it difficult to find the rectified load's ac impedance, which can determine if it will cause system instability. However, it is useful to consider the ac and dc power in estimating this impedance. Consider the distorted rectifier current from Fig. 3, driven by an ac voltage with rms $v_{\rm ac,rms}$. The active power $p_{\rm ac}$ can be determined from the rms of the in-phase fundamental current $i_{d,\,\rm rms}$, while the reactive power $q_{\rm ac}$ can be determined from the rms of the quadrature fundamental current $i_{q,\,\rm rms}$ as

$$p_{\rm ac} = v_{\rm ac,\,rms}\, i_{d,\,\rm rms}, \quad \text{and} \quad q_{\rm ac} = v_{\rm ac,\,rms}\, i_{q,\,\rm rms}. \tag{4}$$

In principle, the harmonic content in the current contributes no active power since it is all orthogonal to the ac voltage. Thus, neglecting diode losses in the rectifier, the dc power $p_{\rm dc}$ provided to the rectified load equals the ac active power $p_{\rm ac}$. Since these

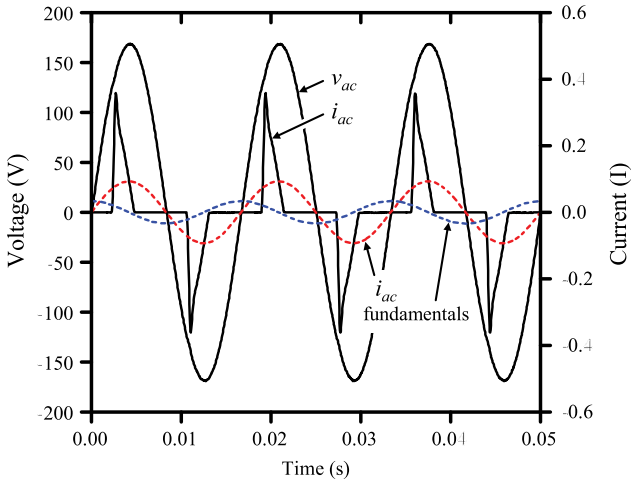

Fig. 3. AC voltage and corresponding rectified load current. The in-phase (red) and quadrature (blue) current fundamentals are shown, from which active and reactive ac power are determined, respectively.

terms are interchangeable and ultimately describe the overall input power, they are referred to as p_{in}.

In this way, the component of ac impedance contributing to active power can be determined if the impedance and power of the dc system following the rectifier is known. More thorough techniques have been developed to determine the ac impedance of rectified loads, but they require specific operating conditions. For example, [17]–[19] present an impedance mapping method to determine the ac impedance from the dc impedance, along with stability criteria. However, these methods assume continuous current through the rectifier diodes, unlike the discontinuous current shown in Fig. 3. Another method presented in [20] and [21] uses small-signal current injection to determine ac impedance. However, this analysis relies on active rectifiers.

Here, we simplify this analysis by considering power flow. For temporary input fluctuations, the converter or driver will resemble a resistive input impedance if its active power demand resembles the relationship in (1). For an ac system, this can be interpreted as the active power versus the voltage rms as

$$p_{\text{in}} = \frac{v_{\text{ac, rms}}^2}{R}. \tag{5}$$

The CPL response time to recover power, or CPL bandwidth, determines up to what frequency the load resembles a negative resistance. This negative resistance will not be present at frequencies higher than the CPL bandwidth, and it will instead resemble a resistive load. Fig. 4 and the associated parameters from Table I describe an example ac system with an equivalent source impedance, resistive loads, and CPLs. Fig. 5 shows a simulation of how the example system's stability depends on the bandwidth of the CPLs. The source current is stable when the CPLs operate at 50 Hz bandwidth, but unstable when operating at a more aggressive 500 Hz. In this paper, an energy buffer is used to lower the effective CPL bandwidth seen at the input, without affecting the load.

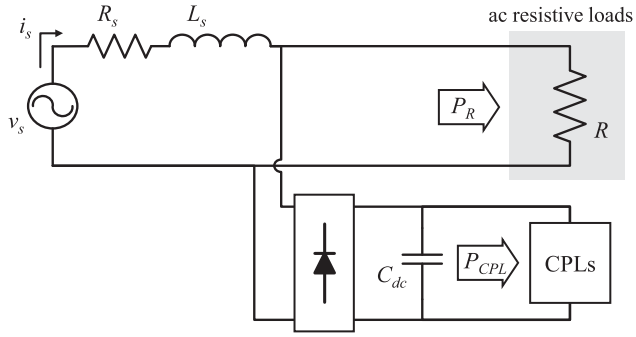

Fig. 4. Example ac system with line impedance, resistive loads, and CPLs that interface through passive rectification.

TABLE I
PARAMETERS FOR EXAMPLE AC SYSTEM

v_s	R_s	L_s	P_R	R	C_{dc}	P_{CPL}
120 V, 60 Hz	0.1 Ω	1 mH	1.3 kW	10 Ω	2 mF	5 kW

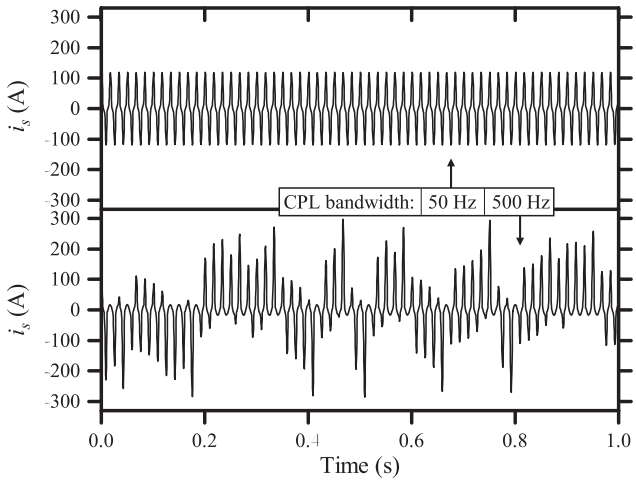

Fig. 5. Simulated source current for the example system from Fig. 4 with parameters from Table I for two CPL bandwidths. Unstable performance occurs when CPL bandwidth is too high.

C. Energy Buffer Circuit

To enforce or command the relationship (5), the input power p_{in} must be allowed to vary. However, if we intend for the load to always consume some constant power P_{load}, then the converter must be capable of buffering short-term input and output power imbalances. An energy buffer, implemented here with a capacitor and a two-stage converter, accomplishes this. Other storage elements and methods have also been used. For example, Cooley *et al.* [22] discusses a parallel multi-converter system, using batteries and fuel cells as main and parallel sources. In [23], an adaptive active capacitor converter is connected in parallel between cascaded power converters in order to stabilize the system. Other energy buffer methods have been used to manage energy storage in converters with an ac and dc port [24]–[27].

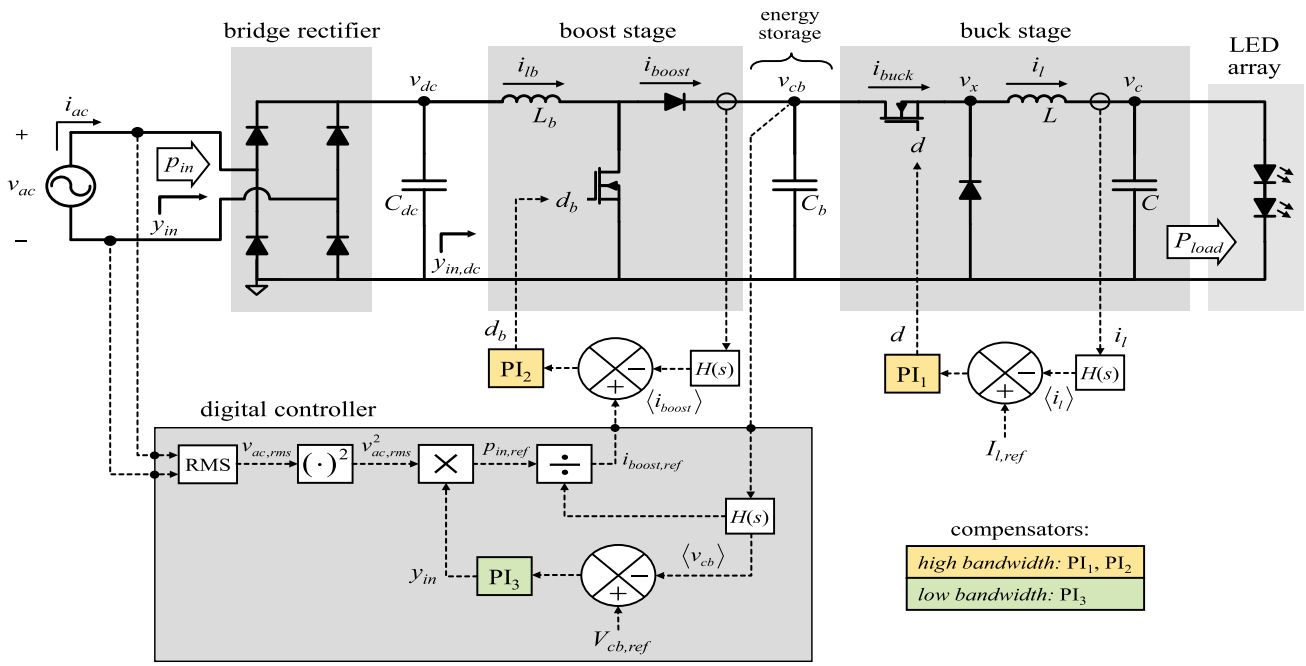

Fig. 6. Overall energy buffer circuit and control scheme.

However, these converters only buffer the power imbalance between ac and dc power. Therefore, they are designed to buffer power at bandwidths only down to twice the line frequency. The presented design focuses the energy buffering capabilities on larger time scale disturbances that can cause traditional CPLs to destabilize the ac line. In general, any energy storage element can be used as long as it can sustain a power flow imbalance for the desired amount of time.

Fig. 6 shows an energy buffer circuit with a capacitor for energy storage using a cascade boost and buck converter topology. The boost stage at the front end steps up the rectified input voltage to maintain the energy storage capacitor C_b charged. Note that this is not a PFC preregulator. In contrast to a PFC, the controllers are designed to safely allow the capacitor voltage v_{cb} to fluctuate dramatically so that it may act as an energy buffer over time scales much larger than is needed in PFCs, which usually require energy buffering only down to frequencies that are twice the ac line.

The buck stage at the output regulates power to the load. For the application of an LED driver, the load is an LED array which is fixed and has a non-linear *I–V* characteristic that does not vary significantly. Therefore, it will consume constant power $P_{\rm load}$ if it delivered a constant current. This is done with a feedback controller that maintains constant inductor current i_l. The load current will become constant since it lags i_l, resulting in $P_{\rm load}$ remaining constant as well. This produces flicker-free lighting that is impervious to input voltage fluctuations. However, the overall input power $p_{\rm in}$ is allowed to vary through a high-bandwidth controller in the boost stage, which is designed to present a resistive input impedance over adjustable times. The imbalance in input and output power is absorbed by C_b, and its voltage v_{cb} determines how much energy remains stored in the energy buffer.

A third, digital feedback loop implemented as a discrete-time PI controller acts at low bandwidth to ensure that over large time scales, the charge on the energy storage capacitor C_b remains balanced. For long-term imbalances, e.g., a complete power outage, a negative imbalance drains the capacitor of charge, while a positive imbalance overcharges it. Therefore, the energy buffer's digital controller monitors this charge and protects against damage by suspending boost stage operation during such scenarios.

III. Feedback Design

Circuit averaging provides a well known and powerful tool for modeling and analyzing the stability of switched converters [28]. A switching circuit is simplified by transforming it into its average linearized small-signal model by taking partial derivatives of nonlinear expressions. Classical control design methods can be used to determine controller gains for stable and desired performance. Other control design techniques can also be applied.

Both stages of the prototype converter operate at a switching frequency of $f_{\rm sw} = 80$ kHz. The low-pass filters $H(s)$ are used to extract the average of the switched signals in the converter. They are first-order filters all with the same bandwidth $f_c = 10$ kHz. The dc circuit input voltage $v_{\rm dc}$ is the output of the passive rectifier and its output capacitor $C_{\rm dc}$, and is approximated as a 160 V source during the design process, though the completed converter is designed to operate over a wide range of input voltages. The boost stage maintains a nominal voltage of 200 V on the energy buffer capacitor C_b while the buck stage regulates the LED array load to the operating point of 65 V, 85 mA.

A. Topology Overview

Here, the buck stage operates in a continuous conduction mode in order to avoid having the duty ratio dependent on the load [29]. The boost stage is designed to operate in discontinuous conduction mode (DCM) to minimize requirements for magnetic energy storage in inductor L_b. This also allows improved control bandwidth over the current $i_{\rm boost}$ flowing into the boost capacitor [30], [31].

The capacitor C_b is both the output capacitor for the boost stage and the energy buffer storage element. Sizing C_b is crucial as this determines how much of an energy buffer the boost stage can provide between the CPL and the variable input power. Two parameters related to the extent of an input voltage disturbance help to determine an appropriate size for C_b: the relative drop in input voltage δ_v (the percentage input voltage decrease), and the voltage drop duration $t_{\rm drop}$. The converter input power $p_{\rm in}$ is the power provided to C_b by the boost stage. The buck stage draws power $P_{\rm load}$ from C_b. Then the net power p_{cb} into C_b is

$$p_{cb} = p_{\rm in} - P_{\rm load}. \tag{6}$$

Under steady-state operation and neglecting losses, the input power matches the load power ($p_{\rm in} = P_{\rm load}$) and there is no net power into C_b. However, for the input to behave dynamically as a resistive load with an admittance $Y_{\rm in}$, $p_{\rm in}$ for an ac supplied converter should depend on $v_{\rm ac,rms}$ as

$$p_{\rm in} = v_{\rm ac,rms}^2\, Y_{\rm in}. \tag{7}$$

Then, to reconcile that $p_{\rm in} = P_{\rm load}$ when there is no input voltage drop, i.e., when $\delta_v = 0$ as

$$p_{\rm in} = (1-\delta_v)^2\, P_{\rm load}. \tag{8}$$

The net power into the capacitor is then

$$p_{cb} = \left((1-\delta_v)^2 - 1\right) P_{\rm load}. \tag{9}$$

If an input voltage drop lasts $t_{\rm drop}$ seconds, then the capacitor, acting as the energy buffer, must provide $E_{\rm eb}$ energy to the load as

$$E_{\rm eb} = -\left((1-\delta_v)^2 - 1\right) P_{\rm load}\, t_{\rm drop}. \tag{10}$$

The capacitor voltage v_{cb}, which is V_{cb} =200 V in a steady state in our example, will decrease as it provides energy to the load. However, the diode in the boost stage prevents the output voltage from falling below the peak input voltage. If v_{cb} drops to this value, then the boost stage will no longer operate as intended. Therefore, a constraint on the controller is that v_{cb} may not decrease below $V_{{\rm ac},pk}$ =170 V, the maximum voltage at the input, equal to the peak input ac voltage. The maximum energy $E_{\rm eb,\,max}$ that C_b can provide to the load is then

$$E_{\rm eb,\,max} = \frac{1}{2}\, C_b\, (V_{cb}^2 - V_{{\rm ac},pk}^2). \tag{11}$$

Substituting (10) into (11) and solving for C_b describes the minimum capacitor size needed as

$$C_{b,\,\rm min} = \frac{2\left(1-(1-\delta_v)^2\right) P_{\rm load}\, t_{\rm drop}}{(V_{cb}^2 - V_{{\rm ac},pk}^2)}. \tag{12}$$

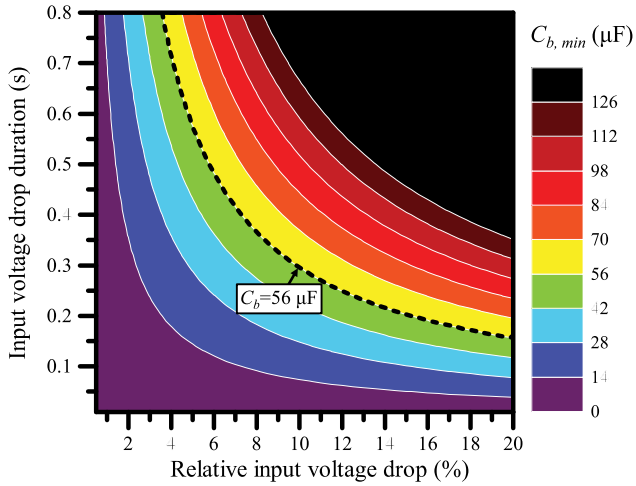

Fig. 7. Minimum C_b for various δ_v and $t_{\rm drop}$.

TABLE II
CONVERTER OPERATING POINT AND PASSIVE COMPONENT VALUES

Parameter	Value	Unit	Parameter	Value	Unit
T_{sw}	12.5	μs	D_b	0.102	
P_{load}	5.53	W	D	0.325	
V_{dc}	160	V	C_{dc}	8.2	μF
V_{cb}	200	V	L_b	1.5	mH
V_c	65	V	C_b	56	μF
I_{lb}	34.5	mA	L	6.8	mH
I_{boost}	27.6	mA	C	2	μF
			R	100	Ω

Fig. 7 provides the minimum C_b needed corresponding to a range of values for δ_v and $t_{\rm drop}$ according to (12). For the converter design described in this paper, we chose a capacitor C_b sized 56 μF to provide enough storage to completely buffer a 5% input voltage drop for up to 0.5 s, or a 10% drop for up to 0.3 s. Table II provides values for the converter's passive components along with the corresponding nominal operating characteristics. All voltages and currents refer to the average values over a switching period. The resistance R is the incremental resistance of the nonlinear LED array at the operating point.

B. Buck Stage Feedback Design

The design of the buck stage is completely focused on satisfying the needs of the load, i.e., providing high-bandwidth constant-power operation. The audio susceptibility of the buck stage is minimized by implementing a high-bandwidth control loop $\rm PI_1$ to maintain a constant current on the inductor L [32], [33], as shown in Fig. 6. A control bandwidth of 1 kHz ensures no voltage fluctuations at the stage input can produce noticeable flickering at the LED output. The high-bandwidth compensator $\rm PI_1$ has a proportional gain K_1 and an integral gain to proportional gain ratio α_1. The light output is flicker free, but the buck stage presents a negative incremental input impedance to the output of the boost stage.

C. Boost Stage Feedback Design

The boost stage is designed to shape the input impedance at the interface between the ac source and the bridge rectifier. Specifically, for this application it is designed to present a resistive power profile with a control bandwidth equal to that of the buck stage by drawing input power $p_{\rm in}$ that is proportional to the ac rms voltage squared:

$$p_{\rm in} = v_{\rm ac,rms}^2\, Y_{\rm in} \tag{13}$$

where $Y_{\rm in}$ is the desired input admittance.

To determine controller gains, $v_{\rm ac,rms}$ is assumed to be proportional to the rectifier output voltage $v_{\rm dc}$, and the commanded input power is instead considered as it relates to $v_{\rm dc}$. The linearized small-signal model for the boost stage is more conveniently found in this way. Neglecting rectifier losses and assuming that power absorbed or provided by $C_{\rm dc}$ is much less than $p_{\rm in}$, power into the boost stage is equal to the overall input power $p_{\rm in}$ calculated as

$$p_{\rm in} = v_{\rm dc}^2\, Y_{\rm in,dc} \tag{14}$$

where $Y_{\rm in,dc}$ is the desired input admittance at the interface between $C_{\rm dc}$ and the boost stage. Then, (13) and (14) imply

$$Y_{{\rm in},dc} = \frac{v_{\rm ac,rms}^2}{v_{\rm dc}^2} Y_{\rm in}. \tag{15}$$

The switching duty ratio in this stage controls the average diode current $i_{\rm boost}$. This is tantamount to controlling input power since (neglecting switching and rectifier losses) input power is equal to the power absorbed by the boost capacitor and buck stage as

$$p_{\rm in} = i_{\rm boost} v_{cb}. \tag{16}$$

For the moment, we assume that v_{cb} is constant (V_{cb}). In Section III-D, this assumption is removed and a third control loop is designed to stabilize the capacitor voltage v_{cb}.

We can use the following observation to solve for the necessary average diode current by substituting (16) into (14):

$$i_{\rm boost,ref} = \frac{v_{\rm dc}^2\, Y_{\rm in,dc}}{V_{cb}}. \tag{17}$$

If the controller is able to track this quantity, then the input impedance will correspond to the desired admittance $Y_{\rm in}$. This control scheme is shown within the boost stage and controller $\rm PI_2$ in Fig. 6. The small-signal perturbation of (17) is

$$\hat{i}_{\rm boost,\,ref} = \underbrace{\frac{2V_{\rm dc}\, Y_{\rm in,dc}}{V_{cb}}}_{A_1}\, \hat{v}_{\rm dc}. \tag{18}$$

Here, A_1 combines the constant terms in (18).

The average diode current $i_{\rm boost}$ for the boost stage operating in DCM is given by

$$i_{\rm boost} = \frac{T_{\rm sw}}{2\,L_b}\, \frac{v_{\rm dc}^2}{V_{cb} - v_{\rm dc}}\, d_b^2. \tag{19}$$

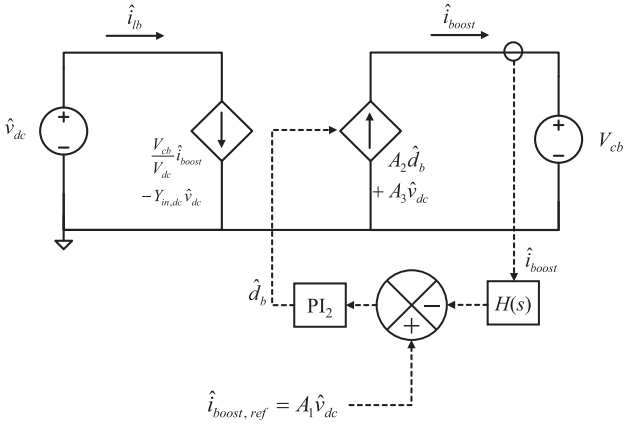

Fig. 8. Linearized small-signal boost stage feedback loop. $H(s)$ filters the switching current waveform.

The linearized small-signal form of (19), expressed in terms of the constants A_2 and A_3, is

$$\hat{i}_{\rm boost} = \underbrace{\frac{D_b\, T_{\rm sw}\, V_{\rm dc}^2}{L_b(V_{cb} - V_{\rm dc})}}_{A_2}\, \hat{d}_b + \underbrace{\frac{D_b^2\, T_{\rm sw}}{2L_b}\left(\frac{2V_{\rm dc}}{V_{cb} - V_{\rm dc}} + \frac{V_{\rm dc}^2}{(V_{cb} - V_{\rm dc})^2}\right)}_{A_3}\, \hat{v}_{\rm dc}. \tag{20}$$

The inductor current i_{lb} is the boost stage input current. Assuming negligible switching losses

$$i_{lb} = \frac{i_{\rm boost} V_{cb}}{v_{\rm dc}} \tag{21}$$

and the small-signal perturbation is

$$\hat{i}_{lb} = \frac{V_{cb}}{V_{\rm dc}}\, \hat{i}_{\rm boost} - \frac{I_{\rm boost} V_{cb}}{V_{\rm dc}^2}\, \hat{v}_{\rm dc}. \tag{22}$$

With these assumptions, the control loop that commands $i_{\rm boost}$ takes the form shown in Fig. 8. The high-bandwidth compensator $\rm PI_2$ has a proportional gain K_2 and an integral gain to proportional gain ratio α_2. For the design presented in this paper, we chose a gain $K_2 = 0.7$ to ensure stable high-bandwidth tracking of the commanded current $i_{\rm boost,\,ref}$. With this design, the controller can track $i_{\rm boost,\,ref}$ with a 1 kHz bandwidth.

D. Energy Buffer Feedback Design

In practice, a third control loop is used to keep v_{cb} at the desired nominal 200 V, while permitting deviations to ease the constant power demand from the utility on short time scales. This third loop balances the conflicting demands of the two loops controlling the buck and boost stages. The buck stage draws a constant $P_{\rm load}$ from the capacitor, while the boost stage provides $v_{\rm dc}^2 Y_{\rm in}$ power to the capacitor. The net power into the boost capacitor is then

$$p_{cb} = v_{\rm dc}^2 Y_{\rm in} - P_{\rm load}. \tag{23}$$

If the input and output power are not balanced, i.e., $p_{cb} \neq 0$, then v_{cb} will either increase or decrease without bound. This balance is not guaranteed from the input voltage alone, so adding a controller that adjusts the converter input admittance $y_{\rm in}$ ensures v_{cb} settles to 200 V in the long term. This control loop has a relatively low bandwidth to preserve the favorable resistive input impedance that the control loop from Section III-C achieves. The controller bandwidth determines the frequencies at which the converter's input resembles either a CPL or a resistor, and will depend on what size energy buffer C_b was selected. Choosing a larger energy buffer results in a lower minimum $\rm PI_3$ bandwidth needed for stability.

This feedback loop is implemented as a discrete-time PI controller using a Cypress PSoC microcontroller with a sampling rate of 7.2 kHz. It can be approximated as a continuous PI controller since it operates with a low bandwidth relative to the sampling rate. The PI compensator outputs $y_{\rm in}$. The reference current $i_{\rm boost,ref}$, which depends on $y_{\rm in}$, is computed and sent as an analog signal to the boost stage controller to command $i_{\rm boost}$ in order to present resistive input impedance. This control scheme is shown in the digital controller block in Fig. 6. The low-bandwidth compensator $\rm PI_3$ has a proportional gain K_3 and an integral gain to proportional gain ratio α_3. It is expressed as $K_3C_3(s)$, where $C_3(s)$ is

$$C_3(s) = \frac{s+\alpha_3}{s}. \tag{24}$$

Because this controller operates at frequencies lower than either of the previous control loops, the low-frequency approximations of the two high-bandwidth control loops can be used to simplify the analysis. The buck stage is replaced with an ideal CPL, and the boost diode current $i_{\rm boost}$ is replaced by an ideal tracking of the reference current $i_{\rm boost,\,ref}$ from (17). That is,

$$i_{\rm buck} = \frac{P_{\rm load}}{v_{cb}}, \quad \text{and} \quad i_{\rm boost} = \frac{v_{\rm dc}^2\, y_{\rm in}}{v_{cb}}. \tag{25}$$

The buck stage input current $i_{\rm buck}$ only depends on v_{cb}. Its linear approximation in terms of the constant B_4 is

$$\hat{i}_{\rm buck} = \underbrace{\frac{-P_{\rm load}}{V_{cb}^2}}_{B_4}\hat{v}_{cb}. \tag{26}$$

From (25), $i_{\rm boost}$ is a function of three variables. The linear approximation in terms of the constants B_1, B_2, and B_3 is

$$\hat{i}_{\rm boost} = \underbrace{\frac{V_{\rm dc}^2}{V_{cb}}}_{B_1}\hat{y}_{\rm in} + \underbrace{\frac{-V_{\rm dc}^2 Y_{\rm in}}{V_{cb}^2}}_{B_2}\hat{v}_{cb} + \underbrace{\frac{2V_{\rm dc}Y_{\rm in}}{V_{cb}}}_{B_3}\hat{v}_{\rm dc}. \tag{27}$$

The current i_{lb} is $v_{\rm dc}\, y_{\rm in}$, so its linear approximation is

$$\hat{i}_{lb} = V_{\rm dc}\,\hat{y}_{\rm in} + Y_{\rm in}\hat{v}_{\rm dc}. \tag{28}$$

These approximations are shown in the small-signal feedback loop diagram in Fig. 9. A perturbation reference of zero implies that the controller aims to always eliminate any perturbation in v_{cb}, thereby maintaining it at 200 V.

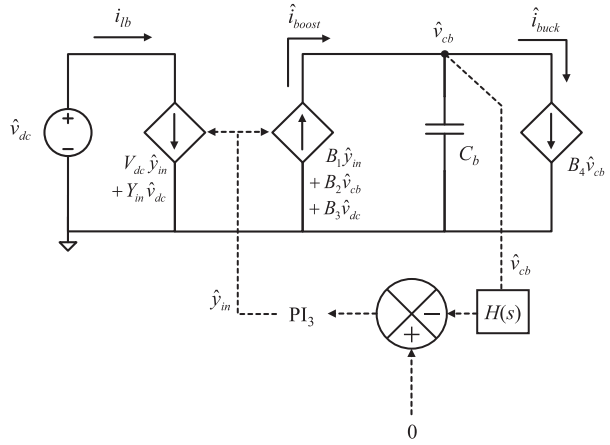

Fig. 9. Linearized small-signal boost capacitor feedback loop.

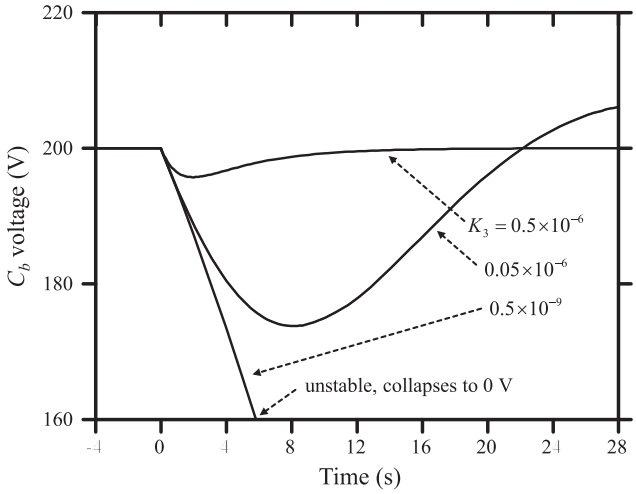

Fig. 10. Energy buffer voltage v_{cb} during a negative step in input voltage $v_{\rm dc}$ for various gains K_3. Minimum gain for stability is $K_{3,\rm min} = 5 \times 10^{-9}$. Voltage v_{cb} collapses with $K_3 < K_{3,\rm min}$. Gain $K_3 = 0.5 \times 10^{-6}$ is selected to avoid an under-damped response.

The capacitor voltage is described in the Laplace domain by

$$\hat{v}_{cb} = \frac{1}{s\,C_b}(\hat{i}_{\rm boost} - \hat{i}_{\rm buck}). \tag{29}$$

The $\hat{v}_{\rm dc}$ to $\hat{v}_{cb}$ transfer function is

$$\frac{\hat{v}_{cb}}{\hat{v}_{\rm dc}} = \frac{B_3}{sC_b - B_2 + B_4 + B_1K_3C_3(s)H(s)} \tag{30}$$

which can be rearranged to a canonical form for root locus analysis as

$$\frac{\hat{v}_{cb}}{\hat{v}_{\rm dc}} = \frac{\frac{B_3}{sC_b - B_2 + B_4}}{1 + K_3\frac{B_1C_3(s)H(s)}{sC_b - B_2 + B_4}}. \tag{31}$$

Fig. 10 shows the energy buffer voltage v_{cb} versus a negative step in input voltage $v_{\rm dc}$ for various gains K_3. When $K_3 < K_{3,\rm min}$, a decrease in input voltage results in the energy buffer collapsing as input power is reduced and the $\rm PI_3$ controller does not act fast enough to restore it. The CPL buck stage drains the energy

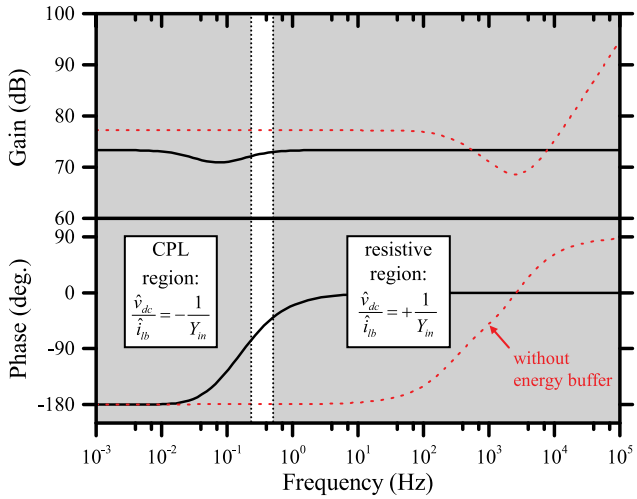

Fig. 11. Overall converter small-signal input impedance Bode plot. Fully resistive at frequencies above 0.5 Hz. Negative resistance at frequencies below 0.2 Hz (-180° phase).

buffer. A gain $K_3 = 0.5 \times 10^{-6}$ is selected for a 2 s settling time response.

The chosen gain produces real poles and an overdamped response. Increasing the gain does not immediately destabilize the system. In fact, there is a negative stability gain margin. There are scenarios where even though the converter is stable, increasing the gain is needed to prevent v_{cb} from reaching critically high levels.

The overall input impedance is found by substituting the PI controller output $\hat{y}_{\rm in}$ into (28), i.e.,

$$\hat{i}_{lb} = V_{\rm dc}\left(-K_3 H(s) C_3(s)\,\hat{v}_{cb}\,\right) + Y_{\rm in}\hat{v}_{\rm dc}. \tag{32}$$

Then, dividing (32) by $\hat{v}_{\rm dc}$ and substituting the transfer function (30) reveals the incremental input admittance as

$$\frac{\hat{i}_{lb}}{\hat{v}_{\rm dc}} = \frac{-V_{\rm dc} B_3 K_3 H(s) C_3(s)}{sC_b - B_2 + B_4 + B_1 K_3 C_3(s) H(s)} + Y_{\rm in}. \tag{33}$$

The inverse of (33) is the incremental input impedance. The limits at low and high frequencies are

$$\lim_{s\to 0} \frac{\hat{v}_{\rm dc}}{\hat{i}_{lb}} = -\frac{V_{\rm dc}}{I_{lb}}, \quad \text{and} \quad \lim_{s\to \infty} \frac{\hat{v}_{\rm dc}}{\hat{i}_{lb}} = \frac{V_{\rm dc}}{I_{lb}}. \tag{34}$$

From the nominal operating point values from Table II, this corresponds to a 73 dB gain with -180° and 0° phases, respectively. Fig. 11 shows the incremental impedance Bode plot and compares it with the incremental impedance if the energy buffer were not in use (shown in dotted red). At frequencies above 0.5 Hz, the impedance magnitude is as desired, with a resistive 0° phase. In the long term, the converter's input must present a negative incremental impedance to maintain the nominal charge in the boost capacitor. However, with the energy buffer and the presented control techniques, this is only present for frequencies under 0.2 Hz. The energy buffer increases the bandwidth of resistive input impedance by three decades compared to the input impedance of the CPL buck stage alone. The complete controller gains used in the design in order to produce this performance are shown in Table III.

TABLE III
COMPENSATOR GAINS

K_1	α_1	K_2	α_2	K_3	α_3
1	5000	0.7	2×10^4	0.5×10^{-6}	0.2

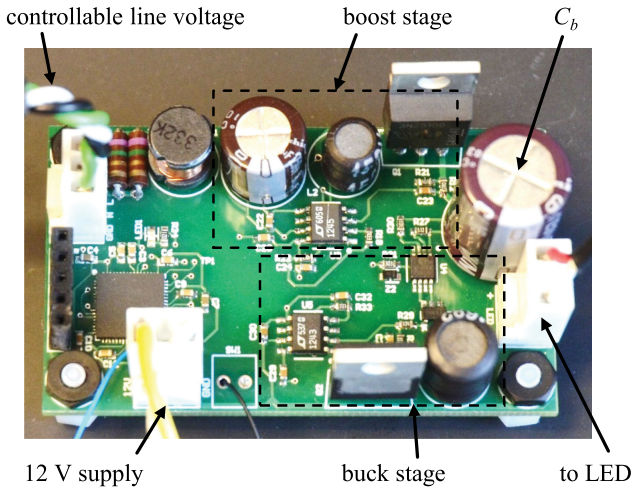

Fig. 12. Energy buffer power converter and connections.

IV. ASSEMBLY AND DIGITAL CONTROL

For design and testing purposes, the converter has been assembled in a PCB separate to the LED array. The board contains both converter stages and a microcontroller for digital control. Fig. 12 shows the PCB and its connections. A PSoC microcontroller digitally implements the control loop from Section III-D and calculates and commands the reference current $i_{\rm boost,ref}$ needed to present the input admittance $y_{\rm in}$. In terms of the rms of the ac input voltage $v_{\rm ac,\,rms}$, the current $i_{\rm boost}$ needed to present an input admittance $y_{\rm in}$ is

$$i_{\rm boost,\,ref} = \frac{v_{\rm ac,\,rms}^2\, y_{\rm in}}{v_{cb}}. \tag{35}$$

The PSoC measures v_{cb} and the ac input voltage absolute value $|v_{\rm ac}|$. Using a sampling rate of 7.2 kHz, a moving average of $|v_{\rm ac}|^2 = v_{\rm ac}^2$ is computed. This average is $v_{\rm ac,\,rms}^2$, the quantity needed in (35).

The PSoC also implements overvoltage protections for the boost stage, which prevents integrator windup. During a decrease in input voltage, the energy buffer discharges as it supplements the load, and the controller increases the input admittance $y_{\rm in}$ to recharge C_b. If the input voltage decrease is drastic, C_b will fully discharge and thus will no longer provide the power demanded by the CPL. In turn, the controller will continue to increase the input admittance. If the input voltage then quickly increases back to its original level, the new higher input admittance can cause excessive input power to overcharge the boost capacitor.

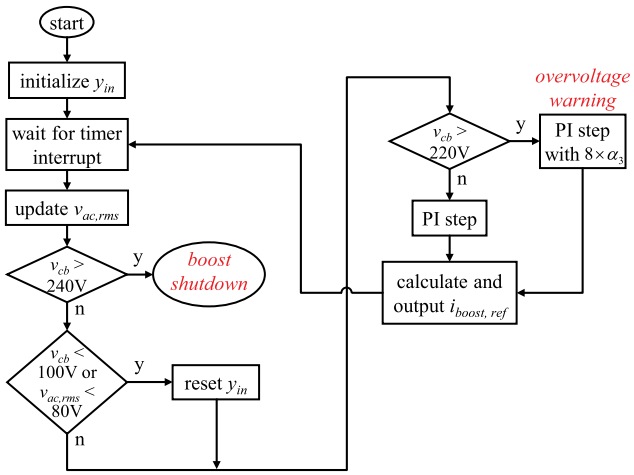

Fig. 13. Boost stage digital control flowchart. Implemented using PSoC 5LP microcontroller.

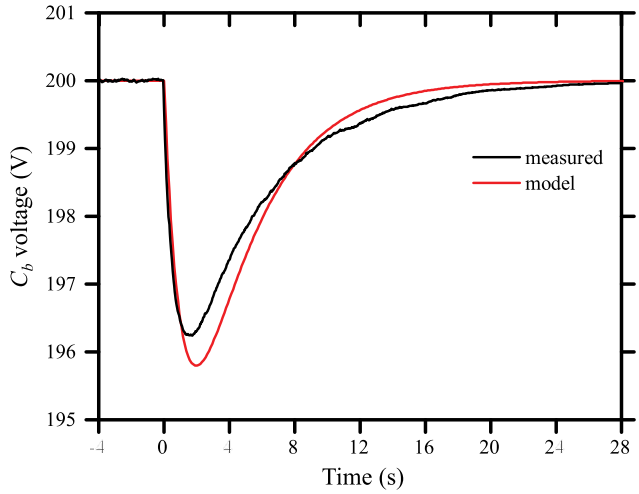

Fig. 14. Measured v_{cb} response to a negative unit step in $v_{\rm dc}$. Compared with transfer function negative step response from Section III-D.

Fig. 13 shows the flow diagram for the PSoC and its protection features. Upon startup, the input admittance $y_{\rm in}$ is first initialized to the nominal value. Then, a timer interrupt is used to trigger sampling and discrete PI control at 7.2 kHz. To prevent issues from integrator windup, the PSoC enters an *overvoltage warning* mode if v_{cb} exceeds 220 V. In this mode, the software PI controller functions with an increased integrator gain $8 \times \alpha_3$. Increasing this gain causes v_{cb} to be restored to nominal (200 V) with less overshoot. If this does not lower the overshoot enough, or if for some other reason v_{cb} exceeds 240 V, the PSoC enters a *boost shutdown* mode in which the boost stage duty cycle goes to zero. The lamp can still operate in this mode, with the output buck stage effectively connected directly to $v_{\rm dc}$ through the boost stage diode. However, control over the input impedance is lost. Another protection against windup is provided by resetting the input admittance integrator if input voltage decreases below a minimum threshold. Then, v_{cb} will not recharge, and when the input voltage is restored, the possibility of an overvoltage is reduced.

V. Test Setup and Measurements

In order to test the converter, a test setup is used that allows an arbitrary ac high voltage to be delivered as an input to the device while voltage, current, and luminous output measurements are recorded. A high-bandwidth light intensity sensor is contained in an enclosure placed over the test lamp. This ensures consistent illuminance measurements across various tests.

Fig. 14 shows and compares the energy buffer voltage v_{cb} response to a negative unit step in input voltage and compares it to a negative step response from the transfer function (31). The voltage on the boost capacitor v_{cb} determines how much energy remains in the energy buffer. A negative input voltage step causes the input power to decrease. The capacitor voltage drops as it supplements the load, and the low-bandwidth control loop restores the voltage over time. Good agreement in Fig. 14 validates the analytical design.

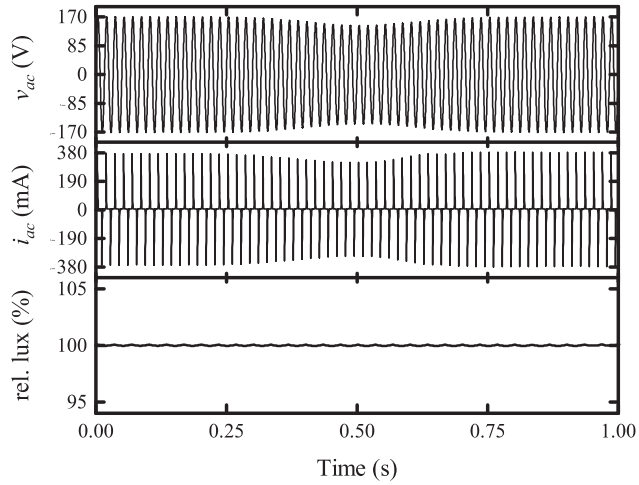

Fig. 15. AC voltage and current during a 15% input voltage dip lasting 0.5 s. Resembles a resistive load. Lamp output is consistent.

A. Input Current and Power

A voltage dip fluctuation can be simulated by modulating the ac waveform by a Gaussian function. Fig. 15 shows a 15% input voltage dip lasting approximately 0.5 s, along with the ac input current and luminous output. The current waveform resembles that of a resistive load since it follows a direct relationship to the input voltage. Simultaneously, the light sensor measures no significant light output fluctuations, signifying constant output performance.

In order to clarify the information portrayed by the ac waveforms, it is useful to calculate and plot rms or average quantities instead. Average ac power is computed by moving average, and dividing this power by $v_{\rm ac,\,rms}$ gives the in-phase current fundamental rms, denoted by $i_{d,\,\rm rms}$.

For a short 15% input voltage dip, the input current for four different lamps is compared in Fig. 16. The incandescent bulb is the best resemblance of an ideal resistive load. However, with no

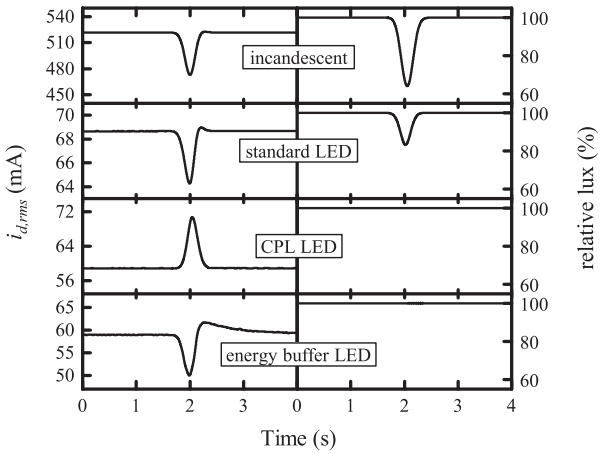

Fig. 16. AC in-phase input current for various devices during a 15% input voltage dip lasting 0.5 s. Expressed as the rms of the in-phase fundamental current. Only a CPL or energy buffered CPL produce consistent lamp output.

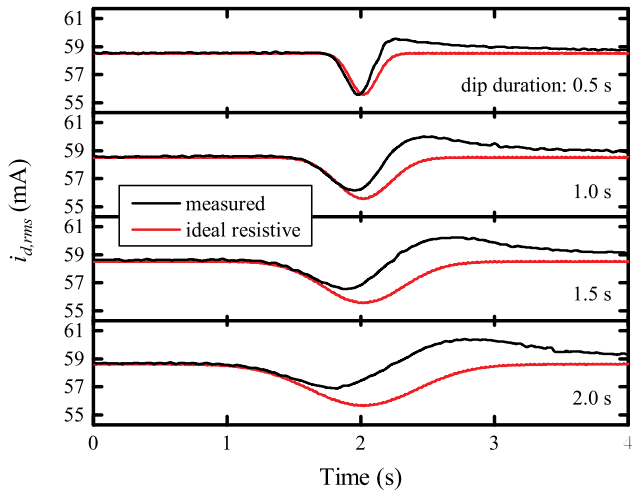

Fig. 17. AC in-phase input current during a 15% input voltage dip lasting various durations, compared to response of an ideal resistance. Expressed as the rms of the in-phase fundamental current. Presented converter cannot resemble a resistance indefinitely. For long input fluctuations, input begins resembling a CPL.

energy buffer, its light output is highly susceptible to the input voltage fluctuation. A standard LED bulb also exhibits resistive input impedance, but the lack of an energy buffer again results in a luminance drop. The lamp labeled "CPL LED" is the presented power converter with the boost stage shut down. In this way, the energy buffer is not active and the input resembles a CPL with current increasing during the voltage dip, demonstrating the negative incremental resistance of the CPL. However, the light output is consistent. Finally, the presented power converter with an energy buffer exhibits favorable characteristics for both measures; its input resembles a resistive load, and its light output is consistent and flicker free.

As the duration of a voltage dip increases, the energy buffer becomes unable to supplement the CPL for the entire duration. A comparison of the input current during voltage dips of varying durations is shown in Fig. 17. For the shortest voltage dip

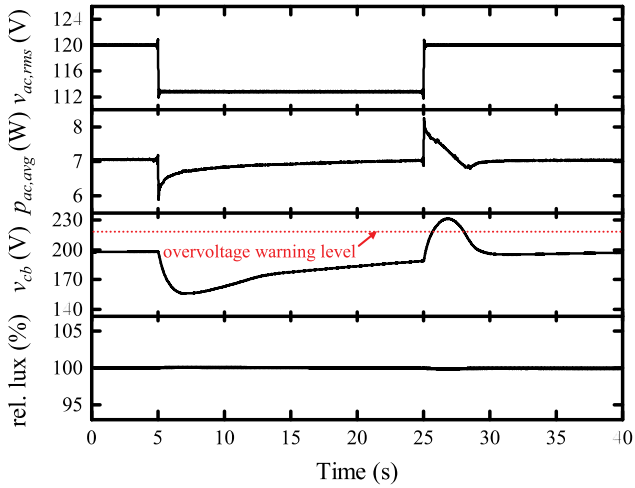

Fig. 18. Overvoltage warning scenario. An excessive C_b charge level is caused by integrator windup during a 6% input voltage drop. Digital PI controller functions at an integrator gain $8 \times K_{i3}$ when $v_{cb} > 220$ V. Critical charge levels are averted while lamp output is not affected.

duration of 0.5 s, the input current resembles that of a resistive load. Longer voltage dip durations do not resemble a resistive load well since the energy buffer becomes increasingly depleted.

B. Overvoltage Scenarios

An overvoltage scenario is shown in Fig. 18. The input voltage decreases by 6% for a 20 s duration. During this time, the energy storage element C_b is depleted dramatically and the input admittance is increased in order for increased input power to allow C_b to recharge. This is shown by the boost capacitor voltage v_{cb}. The input voltage is restored at $t = 25$ s, and with the converter settled on a higher input admittance, excess input power causes the boost capacitor to overcharge. If v_{cb} exceeds 220 V, the converters operates in an *overvoltage warning* mode in an attempt to counteract the effects of the windup. In the scenario in Fig. 18, this action prevents v_{cb} from exceeding critically high levels and restores the voltage to 200 V. The buck stage continues to provide constant power to the load, as is evident by consistent light output.

In a more drastic scenario, *an overvoltage warning* mode may not prevent the energy buffer from reaching a critically high level. If at any time v_{cb} exceeds a maximum allowable 240 V, the converter enters a *boost shutdown* mode. This shuts down the boost stage and any control over the input power and input impedance is lost. In both overvoltage scenarios, the buck stage remains powered through the boost stage diode, and light output is consistent with no noticeable fluctuations.

VI. Conclusion

This paper has presented a power converter with an energy buffer that drives a CPL lighting load while presenting a resistive input impedance to the utility. A switched-mode power supply is implemented with cascaded boost and buck converters. The output buck stage implements high-bandwidth feedback control

on the load to produce high quality, consistent lighting that rejects fluctuations in input voltage. The boost stage provides a flexible input admittance to the utility over short time scales and also the ability to balance the energy consumed by the system over longer time scales. This allows the converter to appear as a resistive load during transient input voltage changes, helping to mitigate stability concerns stemming from CPLs.

We are exploring and expanding this CPL stability approach to other loads that demand constant power, such as HVac components controlled by variable speed drives to regulate a setpoint. Our approach developed here extends directly to boost input stages that also provide active PFC. A cost analysis of this proposed converter, as it would be if its use were widespread, would be a valuable continuation in the research, as well as a comparison of the proposed decentralized stability approach with that of a more centralized solution.

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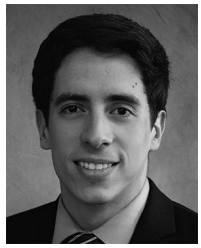

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