Improved Transient Response Control Strategy and Design Considerations for Switched-Capacitor (SC) Energy Buffer Architectures

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***Abstract*—Switched-capacitor (SC) techniques have been proposed for energy buffering applications between DC and AC grids. These techniques have been implemented using film or ceramic capacitors and have been shown to achieve high energy utilization and comparable effective energy density to electrolytic capacitors. Practical applications require control schemes capable of handling transients. This paper takes a comprehensive view of the SC energy buffer design space and examines tradeoffs regarding circuit topology, switching configuration, and control complexity. A two-step control methodology that mitigates undesirable transient responses is proposed.**

Keywords- switched-capacitor (SC), energy utilization, control algorithm, dc-ac inverter, ac-dc, power factor correction (PFC), transient response

I. INTRODUCTION

A power conversion interface between a DC and a single-phase AC system requires an energy buffer to store the instantaneous power difference between the constant power of the DC port and the time-varying power of the AC port. Traditionally, this energy buffer is implemented with large electrolytic capacitors. As the system reaches periodic steady state with unity power factor, the instantaneous power difference manifests itself as a voltage ripple on the energy buffering capacitor at double-line frequency. However, the single capacitor approach is known to achieve poor energy utilization [1].

Energy utilization is defined as the ratio of the energy used to buffer the instantaneous power difference to the maximum stored energy on the capacitor. Energy utilization for single capacitor energy buffers with respect to the peak-to-peak ripple ratio can be derived as:

$$E_{util} = \frac{2r}{1 + r + 0.5r^2}, \quad (1)$$

where r is the prescribed peak-to-peak ripple ratio. For instance, in a system with 10% peak-to-peak ripple ratio, the single capacitor energy buffer implementation has an energy utilization of less than 20%. In other words, the capacitor has to store more than 5 times the energy as actually needed.

Many alternative techniques have been proposed to manage the double-frequency energy flow [1-5]. In particular, the recently introduced switched-capacitor (SC) energy buffer architectures [6, 7] can achieve higher energy utilization and lower voltage ripple. Fig. 1 shows the general architecture of the proposed SC energy buffer. The SC energy buffer consists of two banks of capacitors shown as one possible example in Fig. 1: "backbone" capacitors and "supporting" capacitors. The configuration will be described as *y*-*z*, where *y* is the number of capacitors in the backbone bank and *z* is the number of capacitors in the supporting bank.

The backbone capacitor bank contains capacitors that withstand large voltage variations during the ripple cycle, where the voltage variations are typically much greater than the prescribed peak-to-peak ripple allowance. In order to bring the bus voltage ripple within bound, the supporting capacitor bank is switched so that the voltages of the supporting capacitors are either added to or subtracted from the voltage of the backbone capacitor bank. The switching pattern is defined such that the resulting bus voltage satisfies the ripple specification. The supporting capacitors have to withstand a much smaller voltage variation during the ripple cycle. Specifically, in this two-bank energy buffer architecture, the voltage variations on the supporting capacitors are limited to one-half the specified peak-to-peak bus ripple magnitude if the supporting capacitors and backbone capacitors are equally sized.

Using this technique with a peak-to-peak ripple ratio of 10%, energy utilization can be improved to >70% with one backbone capacitor and >80% with three backbone capacitors. Moreover, this technique enables the use of capacitors with smaller capacitance and lower voltage ratings, thereby making it possible to replace limited-life electrolytic capacitors with ceramic or film capacitors. Practical uses of this technique require control schemes that can produce acceptable transient responses to time-varying power levels. Section II examines different control schemes and exposes undesirable behavior under certain operating conditions. This paper proposes a two-step control scheme while taking a comprehensive view of the design space, exploring tradeoffs between circuit topology and control. Topology selection and switching configurations are discussed in Section III. Control strategy requirements and tradeoffs are examined in in Section IV. Finally, simulation results of the proposed control strategy in two different circuit topologies are presented in Section V.

II. CONTROL ALGORITHMS

Different control schemes have been proposed for the SC energy buffer shown in Fig. 1 [6, 7]. Two approaches are

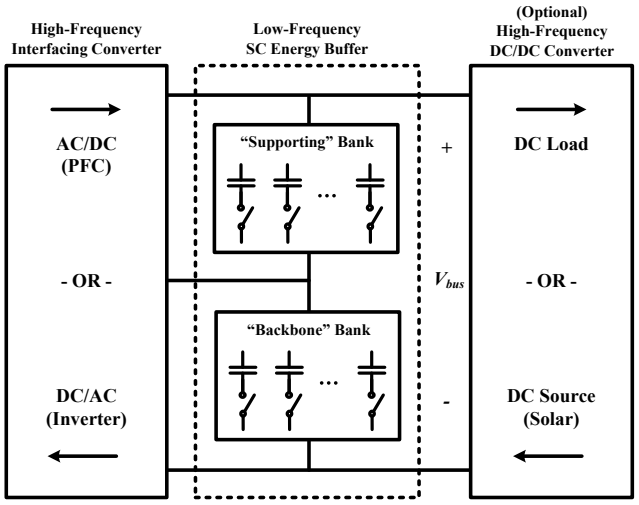


Figure 1. General architecture of the SC energy buffer.

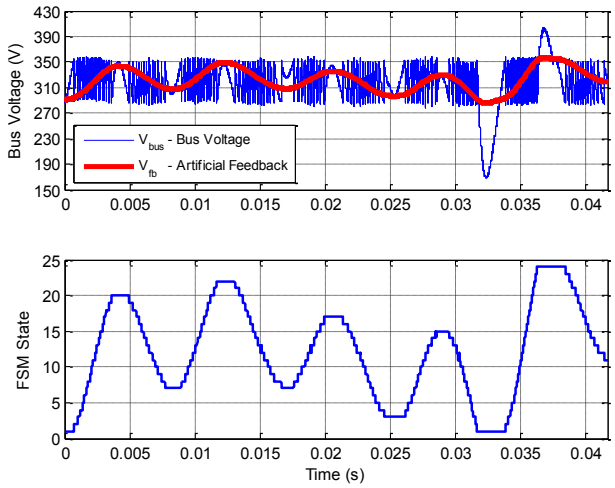


Figure 2. Transient bus voltage response of a 2-6 SC energy buffer in a PFC due to a 30% load power step. The energy buffer uses bipolar switching configuration and is controlled by the bus voltage monitoring, finite state machine controller in [6]. The state variable saturates at the terminal states, 1 and 24, during the power transient, causing unacceptable ripple shoot-through.

reviewed briefly here, neither of which is necessarily satisfactory during transient operation. These two approaches illustrate different control design philosophies with regard to the bus voltage ripple relative to the overall level of power being processed. In the first case, discussed below in the context of a PFC utility interface for providing power to a load, the controller offers a fixed peak-to-peak bus ripple, $\Delta V_{r,pp}$, for all but very low power levels during steady-state operation. In the second case, discussed in the context of a grid-tie inverter, the controller varies the steady-state bus ripple with the power level injected to the grid. In both cases, power delivery changes can result in large bus voltage transients.

A. Bus-Voltage Monitoring, Finite State Machine Control

We first illustrate a control problem in the case of a SC energy buffer inside a PFC utility interface. In this example, discussed in [7], the controller directly monitors the bus voltage and triggers finite-state-machine state transitions when the bus voltage is about to exceed pre-defined bounds. The switching pattern associated with each state is defined so that an increase in state number would boost the bus voltage up by $\Delta V_{r,pp}$ when the bus voltage dips below the lower trigger threshold, and a decrease in state number would drop the bus voltage down by $\Delta V_{r,pp}$ when the bus voltage rises above the upper trigger threshold.

Because the supporting capacitor voltages are not individually monitored, state transitions do not guarantee the desired boost or drop on the bus voltage, e.g., as shown in [7]. Also, the state machine is unaware of the power level and is not reset or "re-centered" between ripple cycles, so power transients may cause the state to saturate at either the state associated with the lowest or the highest apparent energy. During this state saturation, the SC energy buffer no longer has any available state to contain the ripple in the saturation direction. Finally, because the controller attempts to maintain the bus voltage within constant DC boundaries at all times, a transient response to a new steady-state power level can lead to extreme bus voltage transients as the controller will attempt to maintain the DC boundaries until it is driven into state saturation.

To investigate such undesirable behaviors, a SPICE simulation is performed using LTSpice from Linear Technology. A LT1249 active power factor controller is selected for the simulation because the model is readily available in the bundled component library. The simulated testbench circuit is derived from the typical application example in the datasheet [8] with the output filter capacitor replaced by the 2-6 SC energy buffer presented in [7]. In addition, the simulation model also incorporates the controller implemented with a 24-state finite state machine and an "artificial feedback voltage" reported in [7]. The design specifications include a nominal output voltage of 320V and a 20% peak-to-peak ripple ratio. The simulation results are shown in Fig. 2, where the bus voltage exhibits unacceptable over- and undershoots when the state machine state saturates at states 1 and 24 in response to 30% load power level transients. Note that the artificial feedback voltage does not faithfully reproduce the over- and undervoltage conditions. The extreme overshoots from the shortcomings of the controller are amplified by two additional factors. The capacitances of the capacitors in the energy buffer are greatly reduced under the assumption of proper ripple reduction. Moreover, the capacitors are linked in series, which further diminishes the effective capacitance seen on the bus.

B. Supporting Capacitor Monitoring, Timing Interval Control

A similar control problem can be illustrated considering Fig. 1 in its inverter configuration. In this case, discussed in [6], the individual supporting capacitor voltages are monitored while giving up the task of controlling the backbone capacitor voltage to the energy-balance controller of the inverter. The control logic pre-computes the charge and discharge intervals for each supporting capacitor relative on the phase of the ripple cycle and enables these intervals when the capacitor voltages are within their reference minima and maxima [6].

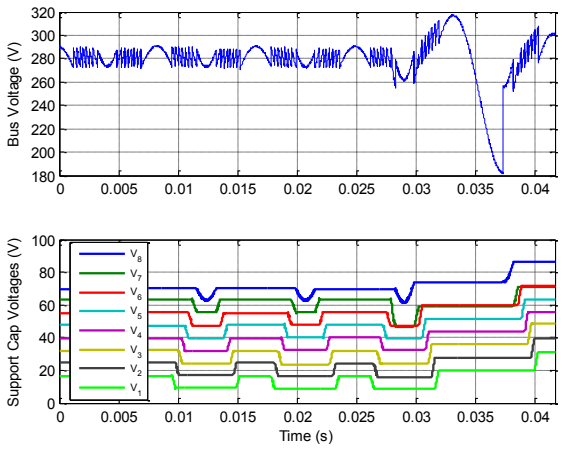


Figure 3. Transient bus voltage response of a 1-8 SC energy buffer in a solar inverter due to a 30% input power step. The energy buffer uses the unipolar switching configuration and is controlled by the supporting capacitor monitor, timing interval controller. The discharge is disabled in order to charge the supporting capacitors up to the new reference values, exposing the full-swing backbone capacitor ripple.

The reference voltages scale linearly with power level and the ripple is reduced by a fixed ratio. Therefore, the resulting bus voltage behavior is very similar to that of a single capacitor implementation – the backbone capacitor experiences the natural transient and settling behaviors from the energy-balance controller, and the supporting capacitors are used to keep the ripple voltage within the prescribed limits.

However, this controller makes inefficient use of the supporting capacitor bank – all capacitors in the supporting bank are used regardless of power level. As a result, the supporting capacitor voltage references must be adjusted significantly in response to power variations. Since the voltage on capacitors cannot change instantaneously, the supporting capacitors will need time to be charged or discharged to the new reference levels. This introduces a few cycles where the supporting capacitors experience large imbalance in their charge and discharge times. In the extreme case, the supporting capacitors may not be used in either the charge or the discharge cycle at all, thus exposing the bus to the full-swing ripple from the backbone capacitor with reduced capacitance during the corresponding half cycle.

A SPICE simulation is again used to demonstrate the potential problems with this control strategy. The simulated testbench circuit is implemented using the feedforward energy-balance controlled solar inverter demonstrated in [6] along with a 1-8 SC energy buffer. The nine supporting capacitors are monitored and managed by the controller with pre-computed switch timings discussed above, and the backbone capacitor is controlled by the feedforward energy-balance controller of the solar inverter. The design specifications include a nominal output voltage of 250V and a 10% peak-to-peak ripple at maximum power. As shown in Fig. 3, the bus voltage experiences an unacceptable undershoot when the supporting capacitor voltages references are dramatically increased in response to 30% power level transients. The second subplot in Fig. 3 shows the

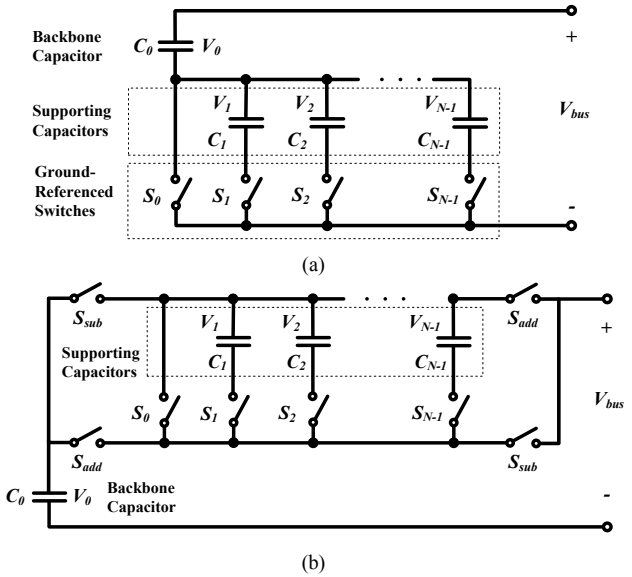


Figure 4. General 1-*z* architecture of SC energy buffer. (a) Implementation with ground-referenced switches only for unipolar switching configuration. (b) Implementation with four additional switches to achieve bipolar switching configuration.

nonparticipation of the supporting capacitors during their discharge half-cycles, resulting in the lack of buffering during the discharge half cycle.

III. SC Energy Buffer Design Considerations

There are many tradeoffs to be considered in designing an SC energy buffer. A basis for making these tradeoffs is developed in this section. In principle, energy utilization can be increased arbitrarily at the expense of switching frequency and buffer complexity. Desirable transient performance implies new control requirements that also impact SC buffer design. We consider these tradeoffs in the context of two general SC buffer architectures, unipolar and bipolar switching configurations shown in Fig. 4.

A first consideration in designing the energy buffer is energy utilization when the design goal is to reduce the overall amount of physical capacitance in the system. Equation (1) summarizes the energy utilization for a non-switching, single capacitance buffer. The energy utilization equation can be generalized for the SC case shown in Fig. 1 by taking the sum of ΔE, the change in energy stored, divided by the sum of $E_{\max}$, the maximum energy stored, of all the capacitors in the energy buffer . This is shown in (2).

$$E_{util} = \frac{\sum_{j=1}^{y} \Delta E_{backbone}(j) + \sum_{i=1}^{z} \Delta E_{support}(i)}{\sum_{j=1}^{y} E_{\max,backbone}(j) + \sum_{i=1}^{z} E_{\max,support}(i)} \qquad (2)$$

The variables in (2) depend on not only the nominal bus voltage, the specified ripple ratio and the selected capacitor size, but also the switching configuration. Thus, the two cases shown in Fig. 4 illustrate a tradeoff between topology and switching complexity versus capacitor utilization. Note that Fig. 4 illustrates the two cases with a single backbone

capacitor, i.e., $y = 1$ in each case, although more backbone capacitors could be employed with arbitrary y.

A. Capacitor Configurations

For illustration, the energy utilization of an SC energy buffer with bipolar switching configuration versus different numbers of backbone and supporting capacitors for three different ripple ratios is shown in Fig. 5. Two important conclusions can be drawn from these plots. First, for each ripple ratio and number of backbone capacitors used, there exists an optimal number of supporting capacitor which maximizes the energy utilization of the overall energy buffer. Secondly, the energy utilization can be improved with diminishing return by introducing more backbone capacitors.

However, the number of backbone capacitors cannot be increased indefinitely. The switching frequency of the SC energy buffer is directly proportional to the number of capacitors in the energy buffer. In particular, the switching frequency can be approximated as

$$f_{sw} \approx 2 f_{grid} \cdot p \cdot y \cdot (z+1), \tag{3}$$

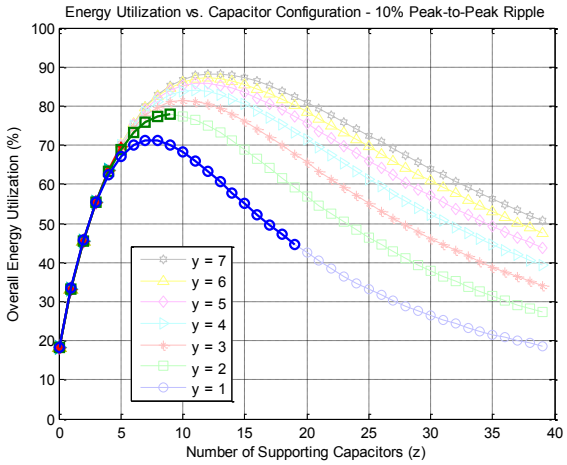
where $p = 2$ for unipolar switching schemes and $p = 4$ for bipolar switching schemes. Clearly, increasing the number of capacitors would unavoidably increase the incurred switching loss. Also, excessive number of capacitors would cause the SC buffer switching frequency to approach that of the PFC or inverter controllers, consequently causing undesirable interactions between the two control loops.

In order to guarantee time-scale separation between the low-frequency energy buffer control and high-frequency PFC or inverter control, the number of capacitors must be limited. When designing a switching converter, the switching frequency is expected to be high with respect to the natural frequency of the energy storage elements. This extends to the case of a SC energy buffer. While any specific case requires a control loop and stability analysis, a similar rule-of-thumb to keeping the natural time constant in the canonical models long compared to the switching period, e.g. 10 times the switching period, is to have the SC buffer switching at below 1/10 the frequency of the interfacing switching converter. As illustrated in Fig. 1, high-frequency switching converters can be found on either side of the SC energy buffer.

For example, assuming the switching frequency of the high-frequency loop is on the order of a hundred kilohertz, average switching frequency of the energy buffer control might be constrained to be less than approximately ten kilohertz. In other words, the relationship in (4) must hold.

$$p \cdot y \cdot (z+1) \le \frac{10kHz}{2 f_{grid}} \tag{4}$$

This establishes an upper bound on the number of capacitors that can be incorporated in these SC energy buffers. Referring back to Fig. 5, the unfeasible combinations of capacitor configurations are greyed out. As shown, the achievable improvement in energy utilization is limited, albeit still significant, as this becomes a constrained optimization problem. For peak-to-peak ripple ratios of 2%, 5%, and 10%, the optimal achievable energy utilizations are realized with only one or two backbone capacitors.



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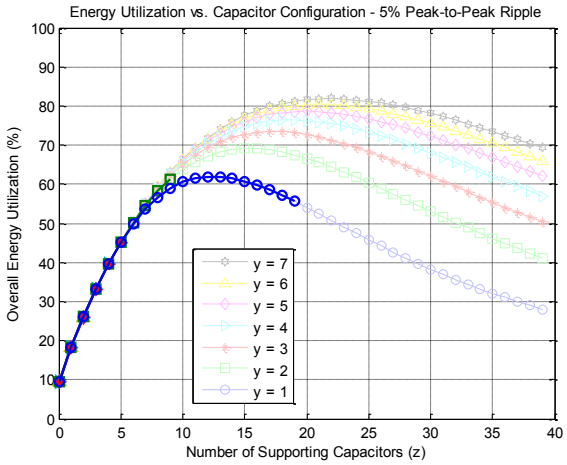

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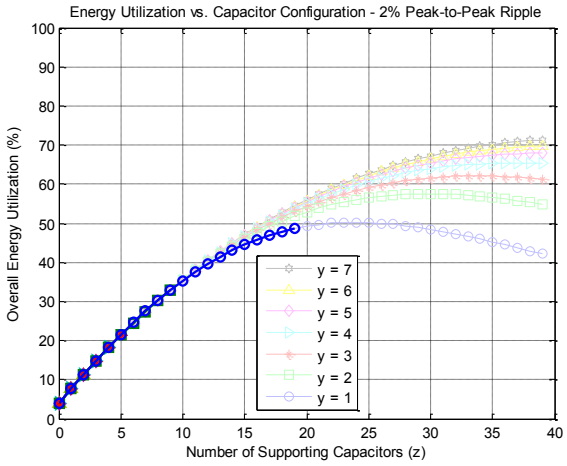


(c)

Figure 5. Overall energy utilization of the SC energy buffer as a function of the capacitor configuration. These numbers are computed for SC energy buffers with equally sized backbone and supporting capacitors using the bipolar switching configuration. Recall that y denotes the number of backbone capacitors and z denotes the number of supporting capacitors.

In a SC energy buffer, the bus voltage is no longer an accurate measure of the energy stored in the energy buffer. Therefore, when integrating with conventional power-factor correction controllers or energy-balance inverter controllers, the bus voltage cannot be directly used as the feedback voltage. Reference [7], for example, uses an artificial feedback voltage to ensure compatibility with existing hardware. However, such an artificial feedback voltage is not guaranteed to be sinusoidal and may not reliably detect under- and over-voltage conditions as shown previously.

By implementing the backbone capacitor bank with only one capacitor, a voltage feedback signal is available at the single backbone capacitor for interfacing with conventional power-factor correction controllers or energy-balance inverter controllers. Because there is a single path in the backbone capacitor bank through which the energy buffering current must flow, the single backbone capacitor voltage can be treated as an AC-scaled version of the single electrolytic capacitor voltage in traditional energy buffers.

Energy utilization is still high with a single backbone capacitor. Specifically, in the case of 10% peak-to-peak ripple ratio, using a single backbone capacitor reduces the achievable energy utilization from 77.9% to 71.2%, still a sizable improvement from 18.1%. In the cases of 5% and 2% peak-to-peak ripple ratios, the optimal energy utilizations remain unchanged. Also, this simplification enables the exclusive use of ground-referenced switches in unipolar switching configurations.

B. Switching Topology Tradeoffs

We therefore focus on the 1-*z* architecture shown in Fig. 4, where we define $N = z + 1$ as the total number of capacitors in the SC energy buffer. The backbone capacitor is denoted as C_0, and the supporting capacitors are denoted as C_1 through C_{N-1}. Two types of switching configurations can be explored: unipolar and bipolar. In unipolar switching, supporting capacitor voltages are added to the backbone capacitor voltage when it is too low, but are never subtracted. With equally sized capacitors, the resulting peak-to-peak bus voltage ripple with respect to the total number of capacitors is

$$\Delta V_{r,pp,unipolar} = \frac{2}{N+1} \cdot \left(\frac{P}{\omega_0 \cdot C \cdot V_C} \right), \tag{5}$$

where P is the power level, ω_0 is the angular frequency of the grid, C is the capacitance of all capacitors in the SC energy buffer, and V_C is the nominal voltage of the grid.

If the backbone capacitor voltage is regulated by energy balance control, i.e., to achieve constant mean squared voltage, using the unipolar switching configuration will result in a variable mean bus voltage. Specifically, the mean bus voltage will increase with increasing power level, but will always be above the regulated mean voltage of the backbone capacitor. For this reason, the unipolar switching configuration is unsuitable for PFC applications with constant output voltage requirements. However, it is compatible with solar inverters where the bus voltage must remain sufficiently high in order to maintain control of the grid. In addition, because the mean bus voltage is positively correlated to the power level, it ensures fast response time in hysteresis current controlled inverters when the output current amplitude is increased. Finally, the one-sided switching configuration also has the added benefit of being able to utilize ground-referenced switches only. By rearranging the supporting capacitor bank and the backbone capacitor as shown in Fig. 4a, the unipolar SC energy buffer avoids high-side gate drives.

In the bipolar switching configuration, four additional switches are added in order to invert the polarity of the supporting capacitor voltages during parts of the ripple cycle. This enables ripple reduction with a constant mean bus voltage. Supporting capacitor voltages are added to the backbone capacitor voltage when it is too low and are subtracted from the backbone capacitor voltage when it is too high. As such, the bipolar switching configuration is compatible with power-factor correction applications without an additional dc-dc converter at the output. Moreover, the bipolar switching configuration uses the supporting capacitors more efficiently; it achieves a peak-to-peak voltage ripple of

$$\Delta V_{r,pp,bipolar} = \frac{1}{N} \cdot \left(\frac{P}{\omega_0 \cdot C \cdot V_C} \right), \tag{6}$$

approximately twice as effective, in terms of ripple reduction capability versus number of capacitor added, as the unipolar switching configuration. The ripple adavantage requires four extra switches and high-side gate drives, which contribute to additional switching losses.

The steady-state maximum supporting capacitor voltages under maximum power rating for both switching configurations are outlined here to supplement energy utilization calculations and to facilitate capacitor selections.

$$V_{\max,unipolar}(i) = \frac{i+1}{N+1} \cdot \frac{P_{\max}}{\omega_0 \cdot C \cdot V_C} \tag{7}$$

$$V_{\max,bipolar}(i) = \frac{i+1}{2N} \cdot \frac{P_{\max}}{\omega_0 \cdot C \cdot V_C} \tag{8}$$

for $i = \{1, 2, \ldots, N-1\}$. For the backbone capacitor, the maximum capacitor voltage is the same for both switching configurations and can be calculated as

$$V_{\max}(0) = V_C + \frac{1}{2} \cdot \frac{P_{\max}}{\omega_0 \cdot C \cdot V_C}. \tag{9}$$

In the following section, control strategies for both switching configurations are presented.

IV. Two-Step Control Strategy

A controller capable of handling power level transients must not prescribe strict DC voltage boundaries constraints on the bus voltage. Instead it should allow the DC level of the bus voltage to undergo natural settling while maintaining the AC ripple magnitude within specification around the DC level. This enables the controller to evenly distribute the charge buffering to the supporting capacitors instead of leaving the terminal-state capacitors to absorb an unusual large amount of leftover charges. Also, the controller must effectively reset its state from ripple cycle to ripple cycle in order to guarantee the availability of reserve buffering states in the event of power transients. Finally, the controller must intelligently manage the supporting capacitors so they can remain effective in reducing

the ripple magnitude at all time. This translates to maintaining the reference voltage levels of the supporting capacitors relatively constant regardless of power level.

These requirements can be satisfied by adopting a two-step control strategy: capacitor participation optimization and switch timing determination. The controller first determines the optimal number of capacitors to use in buffering the bus voltage, and then compute the switch timings for the allocated supporting capacitors to maximally reduce the bus voltage ripple. In a 1-z SC energy buffer configuration, the single backbone capacitor voltage is used as the feedback node to either a PFC or an inverter controller. Thus, the SC energy buffer controller discussed here passes the regulation of the backbone capacitor voltage to an external interfacing controller.

Two design examples will be presented to better illustrate the operation and the effectiveness of the proposed control strategy. The specification for the design examples is a 500W inverter with a 250V nominal bus voltage and a 10% peak-to-peak ripple ratio. For maximum energy utilization, a 1-8 SC configuration is chosen for the unipolar switching scheme. For the bipolar switching scheme, a 1-4 SC configuration is chosen for comparable switching complexity and ripple reduction power.

A. Capacitor Participation Optimization

In order to optimize the supporting capacitor participation, the controller samples the current power level and calculates the minimum number of capacitors required to keep the voltage ripple within the specification. The sampling frequency is twice the line frequency for the unipolar switching configuration and four times the line frequency for the bipolar switching configuration. The sampling points with respect to the ripple cycle are illustrated in Fig. 6. Note that the minimum required number should have a lower bound at 1 because the backbone capacitor is always used, and can be derived by inverting the ripple magnitude (5) and (6) for the two different switching topologies. Equation (10) shows the solution for the unipolar switching configuration and (11) shows the solution for the bipolar switching configuration. Note that $P[n]$ is the sampled power level during the current ripple cycle.

$$N_{unipolar}[n] = \max\left(\text{ceil}\left(\frac{2P[n]}{\omega_0 \cdot C \cdot V_C \cdot \Delta V_{r,pp}} - 1 \right),\ 1 \right) \quad (10)$$

$$N_{bipolar}[n] = \max\left(\text{ceil}\left(\frac{P[n]}{\omega_0 \cdot C \cdot V_C \cdot \Delta V_{r,pp}} \right),\ 1 \right) \quad (11)$$

By only using the minimum required number of capacitors, the controller ensures that there is a sufficient number of capacitors in reserve, ready to kick in during a sudden power level increase. In addition, relatively constant energy storage in the supporting capacitors is maintained over a wide range of power levels. Consequently, the system is able to respond to large power transients by adjusting the number of capacitors used, rather than drastically changing the energy stored on all the supporting capacitors. Fig. 7 illustrates the supporting capacitor voltages and the expected ripple size across all possible power levels in the 1-8 unipolar SC energy buffer design example. The number of switching events is reduced as

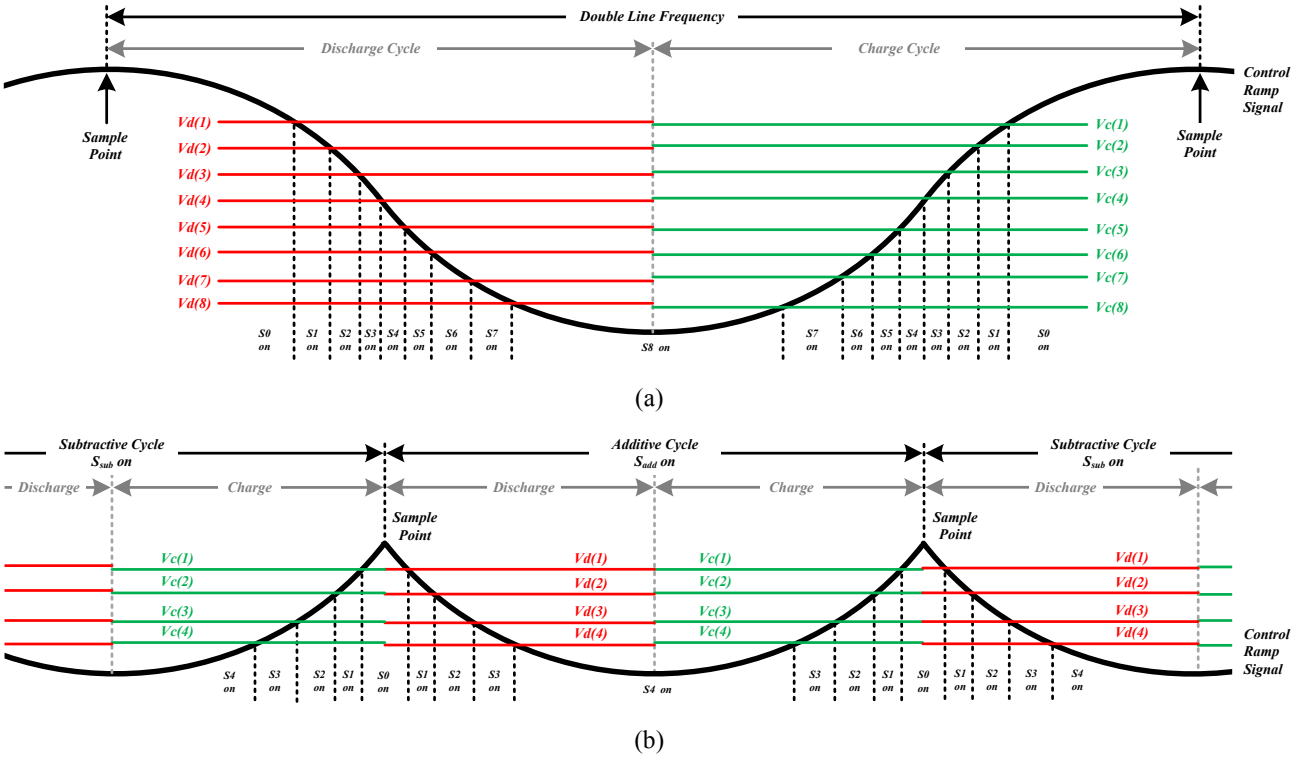
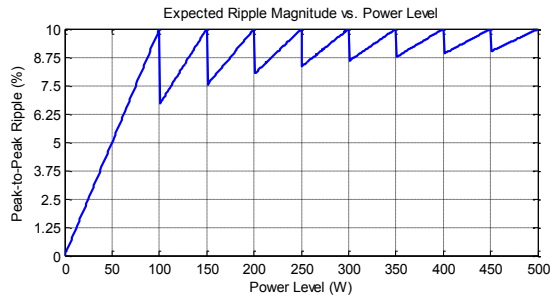


Figure 6. Sampling points and control variables, $v_c(i)$ and $v_d(i)$, in relation to the ripple cycle and the control ramps for (a) unipolar switching configuration and (b) bipolar switching configuration.



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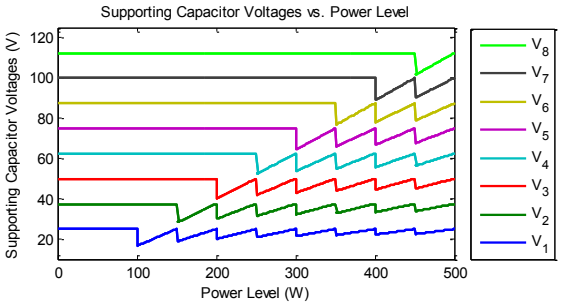


(b)

Figure 7. Expected ripple magnitude and the supporting capacitor voltages as a function of power level for the 1-8 unipolar design example.

the power level decreases, which improves the overall system efficiency.

B. Switch Timing Determination

Given the number of capacitors to use, the controller proceeds to compute the switch timings for the capacitors based on the current power level. That is, the charge and discharge cycle durations are adjusted for each supporting capacitor based on the current sample of its voltage and its respective reference values.

Since the charging and discharging of the capacitors by the double-line frequency energy flow are inherently nonlinear with respect to time, a nonlinear element is inserted into the control loop to enable the use of simple linear function in the rest of the controller. The nonlinear element takes form of a control ramp on which the switching event is triggered. For the unipolar switching configuration, the control ramp is a double-line frequency sine wave phase-locked to the grid. In addition, the unipolar control ramp is assumed to be normalized with unit peak-to-peak amplitude and ramps from 0V to 1V.

For the bipolar switching configuration, the ripple cycle can be further broken up into two sub-cycles. There is the additive sub-cycle where the supporting capacitor voltages are added to the bus voltage, and the subtractive sub-cycle where the supporting capacitor voltages are subtracted from the bus voltage. Thus, the same cycle duration computation needs to be performed twice as often as in the unipolar case. The control ramp function for the bipolar switching configuration then must be periodic at four times the line frequency. Specifically, the bipolar control ramp is a rectified and inverted version of the unipolar control ramp and ramps from 0V to 0.5V. The two control ramp signals in relation to their respective control voltages and sampling points are shown in Fig. 6.

Because the control ramps are assumed to be normalized, the control equations will also be defined in a power-independent fashion. All sampled values are normalized to the full-swing ripple magnitude on the backbone capacitor. The normalizing function is defined as

$$\bar{v}[n] = \frac{v[n]}{P[n]/(\omega_0 \cdot C \cdot V_C)}, \tag{12}$$

where $v[n]$ is the sampled supporting capacitor voltage.

Based on the normalized sampled supporting capacitor voltages, the allowable discharge and charge durations for each capacitor are calculated from (13) and (14),

$$\text{disch}(i) = \max\left(\min\left(\bar{v}_i[n] - \frac{i}{D_x[n]}, \frac{1}{D_x[n]}\right), \frac{k}{D_x[n]}\right) \tag{13}$$

$$\text{charg}(i) = \max\left(\min\left(-\bar{v}_i[n] + \frac{i+2}{D_x[n]}, \frac{1}{D_x[n]}\right), \frac{k}{D_x[n]}\right) \tag{14}$$

where $i = \{1, 2, \ldots, N-1\}$ denotes the supporting capacitor index, $1/D_x[n]$ is the normalized step in voltage between the supporting capacitors, and $k \in [0,1)$ determines the minimum duration. The variable x in $D_x[n]$ denotes the switching configuration. The discrete step size definitions differ in the two switching configurations and are shown in (15) and (16).

$$\frac{1}{D_{unipolar}[n]} = \frac{1}{N_{unipolar}[n]+1} \tag{15}$$

$$\frac{1}{D_{bipolar}[n]} = \frac{1}{2N_{bipolar}[n]} \tag{16}$$

The minimum duration defined by k determines the tradeoff between transient ripple size and settling time. If k is very close to zero, the controller may allow the capacitor voltages to reach their new reference values quicker by imposing a large imbalance between their charge and discharge cycles. However, larger imbalances between the charge and discharge cycles increase exposure of the bus voltage to the ripples of the backbone capacitor, resulting in larger transient ripple. If k is very close to one, the controller will maintain ripple buffer throughout more of the ripple cycle. But the limited imbalance between the charge and discharge cycles results in longer settling times. Note that by managing the capacitor participation based on power level, the reference voltages for the supporting capacitors are kept fairly constant. Therefore, k can be set very close to one for adequate buffering without the risk of unreasonably long settling times.

Having computed the allowable charge and discharge durations for each supporting capacitor, the actual control voltages can be calculated by a cumulative sum. More specifically, the individual charge and discharge control trigger levels are

$$v_d(i) = \sum_{m=i}^{N_x[n]-1} \text{disch}(m) \tag{17}$$

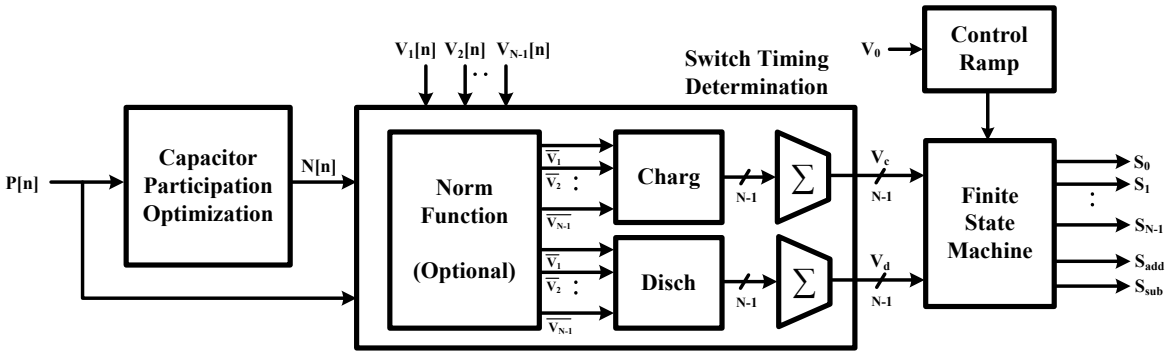


Figure 8. Proposed two-level SC energy buffer controller block diagram, where v_0 denotes the backbone capacitor voltage, $v_i[n]$ for $i = \{1, 2, \ldots, N-1\}$ denotes the sampled supporting capacitor voltage, v_c and v_d correspond to the charge and discharge control signals respectively.

$$v_c(i) = \sum_{m=i}^{N_x[n]-1} \text{charg}(m). \tag{18}$$

When $N_x[n]-1 < i$, the i^{th} control voltage is set to zero, which means that supporting capacitor i is not being used in the current ripple cycle. Furthermore, higher-indexed switches have precedence over lower-indexed switches. That is, if $v_c(1)$, $v_c(2)$, … , $v_c(M) > v_{ramp}$, switches 1, 2, … , $M-1$ are all disabled, and only switch M is turned on. The complete two-step controller block diagram is shown in Fig. 8.

C. Distortion and Phase Error

In the previous section, the control ramps are assumed to be perfectly sinusoidal, or rectified sinusoidal, with zero phase error. Practical phase-locked loops may not guarantee zero steady-state phase error. If a phase error persists between the control ramp and the actual ripple cycle, systematic errors would be introduced to the steady-state voltages of all supporting capacitors, which would result in an increased overall bus voltage ripple. Additionally, the grid voltage may not be perfectly sinusoidal and the ripple voltage may exhibit distortions. Distortion from the assumed sinusoidal profile would introduce unsystematic imbalances in the charge and discharge of the supporting capacitors, which again causes the overall bus voltage ripple to increase.

Therefore, the generated phase-locked signal cannot always be used. Instead, the control ramps can be derived from the backbone capacitor voltage. By passing the AC component of the backbone capacitor voltage through a clamped capacitor circuit, a unipolar control ramp signal from 0V to the peak-to-peak ripple magnitude can be extracted. Similarly, the bipolar control ramp can be created by inverse rectifying the AC component of the backbone capacitor voltage, then processing the resulting signal with a clamped capacitor circuit. This yields a bipolar ramp signal from 0V to the peak ripple amplitude. Alternatively, both control ramp signals can be produced digitally after sampling the backbone capacitor voltage.

Generating the ramp functions directly from the backbone capacitor voltage guarantees zero distortion and phase error between the control signals and the actual ripple cycle. Furthermore, normalization of the sampled signals may not be required because the normalization factor is the inverse of the peak-to-peak ripple amplitude on the backbone capacitor. In practice, implementing control logic with the large voltages may not be feasible. Therefore, resistive dividers can be employed as long as the divider ratio is consistent between the control ramp generation and the supporting capacitor sampling.

D. Pre-charge Circuit Requirement

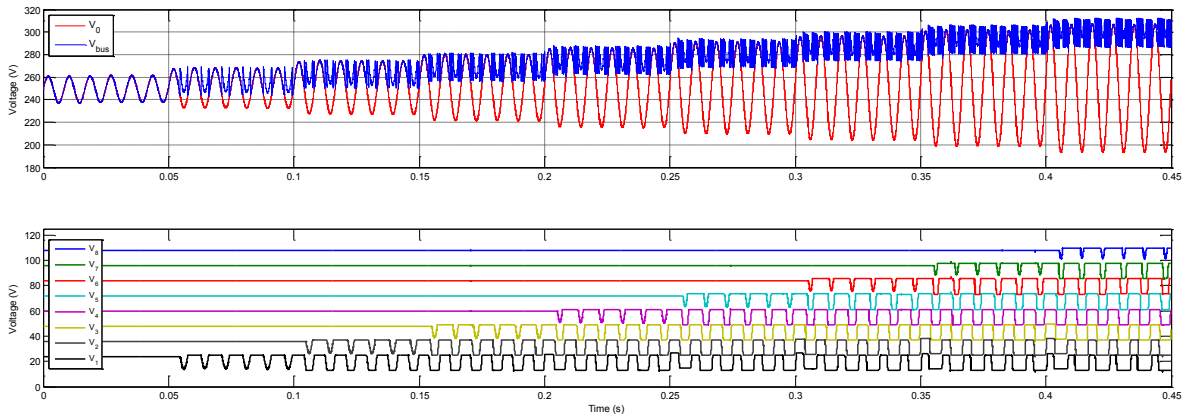
It is not necessary to have a pre-charge circuit used in [7] when using the control strategy described in the previous sections. By adjusting the switch timings, the controller automatically introduces imbalances between the allowable charge and discharge durations of the supporting capacitors so the capacitor voltages reach their reference.

This is a tradeoff. The pre-charge circuit can facilitate the process of charging the supporting capacitors to their reference levels at startup, which allows the system to reach steady-state operation faster. Secondly, the pre-charge circuit can assist in maintaining the charges on unused capacitors. The proposed controller only controls charge and discharge duration on the active supporting capacitors in the ripple cycle; it has no control over the nonparticipating capacitors in reserve. Thus, having a pre-charge circuit adds an extra layer of security to ensure that the capacitors in reserve remain ready in the event of a power level increase. Finally, by using a pre-charge circuit to set up all the capacitors to known states initially, the SC energy buffer can in principle be operated without a requirement to monitor the voltage on every supporting capacitor in the buffer.

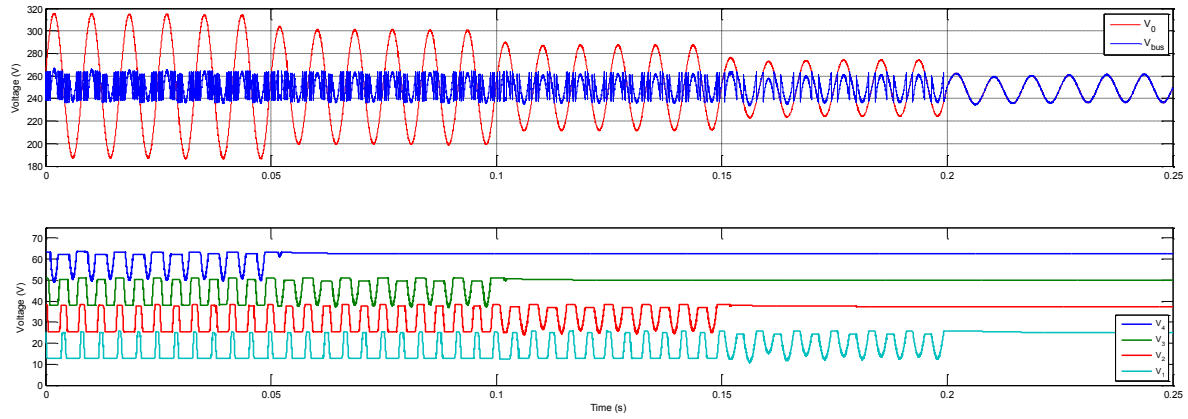
E. Over- and Undervoltage Protection

Aside from the overvoltage protection circuitry commonly found in PFC and inverter controllers, the SC energy buffer controller can incorporate an additional layer of protection to guard against large transients between sampling periods. Switching duration computations are performed at the beginning of each sampling period. If the transient between sampling periods is large enough, the computed and ideal switch timings may differ significantly, resulting in over- or under-buffering conditions.

"Over-buffering" occurs when the actual ripple magnitude is significantly smaller than the expectation of the controller. When such an event occurs, the boost and drop in the bus voltage from switching the supporting capacitors will be greater than what is actually needed. Similarly, "under-buffering" occurs when the actual ripple magnitude is



(a)



(b)

Figure 9. Steady-state bus voltage waveforms of the (a) 1-9 SC energy buffer with unipolar switching experiencing increasing power level and (b) 1-4 bipolar SC energy buffer with bipolar switching experiencing decreasing power level. In (a), the power level increases from 96W to 480W with +48W step size every 50ms. In (b), the power level decreases from 480W to 96W with a -96W step size every 50ms. Recall that v_0 denotes the backbone capacitor voltage, and v_i for $i = \{1, 2, \ldots, N-1\}$ denotes the supporting capacitor voltage.

significantly larger than the expectation of the controller. Consequently, the boost and drop in the bus voltage from switching the supporting capacitors will be smaller than the required values. Both over- and under-buffering conditions result in larger than expected ripple.

Such undesirable conditions can be avoided by introducing feedforward compensation, i.e., a forced resampling triggered on over- and undervoltage thresholds. Once the bus voltage exceeds the defined thresholds, the controller resamples the current power level and the supporting capacitor voltages to recompute the number of active capacitors required and recalculate the switch timings. In over-buffering conditions, the recomputed number of active capacitors would be decreased, whereas in under-buffering conditions, the recomputed number of active capacitors would be increased.

V. Simulation Results

The unipolar 1-8 SC energy buffer and the bipolar 1-4 SC energy buffer design examples have been successfully implemented and simulated in SPICE with a 500W inverter. The system is implemented with control ramps generated from the backbone capacitor voltage to avoid distortion and phase errors. In addition, the minimum duration constant k is set to 0.9 and a pre-charge circuit is configured to manage the voltages of supporting capacitors in reserve. The steady-state bus voltage ripple and the backbone capacitor feedback voltage are shown in Fig. 9. The simulated result matches the analytical solution quite well. The external inverter control manages the backbone voltage and holds it to 250V. The peak-to-peak ripple is set to 10% by inverting (5) and (6) and solving for the required capacitance.

The bus voltage in the unipolar switching energy buffer exhibits a power-dependent mean as discussed in Section III, and remains well above the grid voltage to retain control. As the power level increases, more supporting capacitors become involved in ripple buffering, as demonstrated by the capacitor activities in the subplot of Fig. 9a. Conversely, the bus voltage in the bipolar switching energy buffer has a constant mean over the all power levels as shown in Fig. 9b. With decreasing power level, the supporting capacitors sequentially become inactive, leaving only the backbone capacitor to buffer the small power ripple.

In a sampled system, the worst-case behavior occurs if a large transient occurs immediately after sampling has taken place. Thus, this is the case chosen for the transient response characterization. Positive and negative 30% steps in input power level are introduced to the inverter with the bipolar 1-4

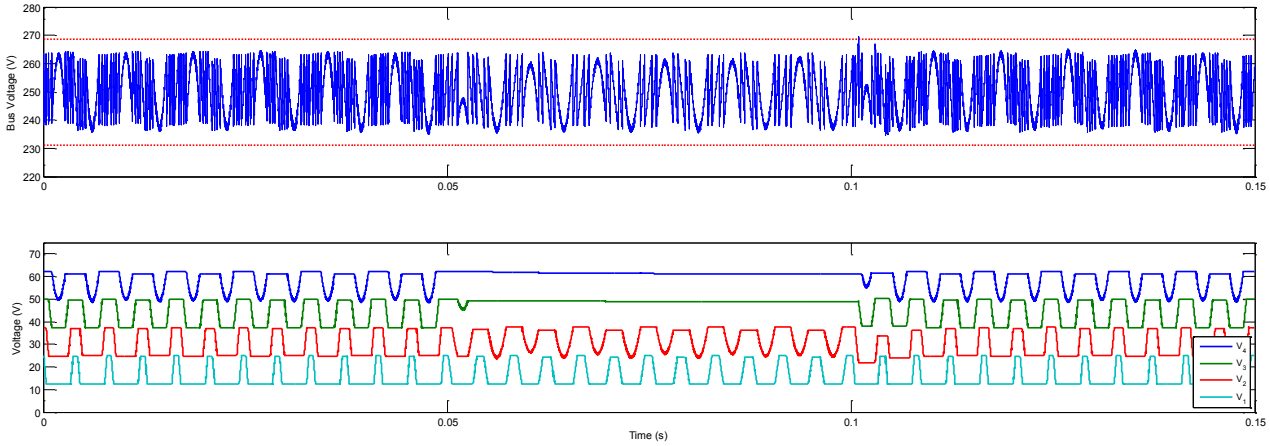


Figure 10. Transient bus voltage response of the example bipolar 1-4 SC energy buffer in a solar inverter due to 30% input power step. The power steps from 480W to 336W at 50ms and back to 480W at 100ms. The second supporting capacitor voltage is shown to deviate from its reference value shortly after 100ms, but the two-step controller brings it back to its reference level in less than 2 ripple cycles.

SC energy buffer. As shown in Fig. 10, the positive step in power causes an under-buffering condition until the bus voltage crosses the upper threshold. Note that the over and undervoltage thresholds are defined to be 1.5 times the ripple specification, i.e. 15% peak-to-peak from 250V, and shown in Fig. 10 as dotted lines. At this point, the controller immediately resamples and recomputes the switch timings to pull the bus voltage back within bounds. Even though the transient may cause some supporting capacitor voltages, v_2 in this particular example, to deviate from their reference values, the two-step controller is able to bring the system back to steady-state in just a few cycles, without any unacceptably large transient ripple.

VI. Conclusion

Switched-capacitor energy buffers have been shown to achieve much better energy utilization than their single electrolytic counterparts. However, overshooting and the possibility of losing control to the grid are major concerns. The proposed control strategy can potentially minimize the possibility of such undesirable behaviors by maintaining an appropriate number of supporting capacitors in reserve to guard against sudden transients in power level.

Two SC energy buffers – 1-8 with unipolar switching and 1-4 with bipolar switching – have been examined in a 500W inverter. The simulated models show excellent agreement with the calculated results. Furthermore, the system is able to maintain a minimum bus voltage of 250V and limit the peak-to-peak ripple to 10% under steady-state operation . It is also shown that the new control strategy can successfully maintain the ripple specification under significant power level transients.

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