Design of DC System Protection

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***Abstract*—A modified Z-source breaker topology is introduced to minimize the reflected fault current drawn from a source while retaining a common return ground path. A conventional Z-source breaker does not provide steady-state overload protection and can only guard against extremely large transient faults. The Z-source breaker can be designed for considerations affecting both rate of fault current rise and absolute fault current level, analogous in some respects to a "thermal-magnetic" breaker. The proposed manual tripping mechanism enables protection against both instantaneous current surges and longer-term over-current conditions. The fault operation intervals of the proposed Z-source breaker topologies are demonstrated in SPICE simulation.**

I. Introduction

Direct current power distribution is under examination for application in all or part of the power architecture of future naval vessels [1]. In particular, the medium voltage dc (MVDC) power system architecture has attracted interest as a means for dealing with dc power loads and providing uninterruptible power [2]. The lack of a natural voltage or current zero-crossing to extinguish an arc that can occur when opening a breaker presents a well-known challenge to protecting dc distribution systems. The recently introduced Z-source circuit breaker [3, 4] potentially mitigates this problem.

Previously proposed Z-source circuit breaker topologies are illustrated in Fig. 1. When a transient fault occurs, the Z-source breaker provides a fraction of the transient fault current through the Z-source capacitors and thereby forces a current zero-crossing in the SCR (silicon controlled rectifier). Once the current in the SCR reaches zero, the SCR naturally commutates off and the faulty load becomes isolated from the source.

However, practical uses of this technique are limited because the Z-source breaker does not provide steady-state overload protection and can only guard against large transient faults. Furthermore, the previously proposed Z-source breaker topology shown in Fig. 1a does not provide a common ground between the generation source and the load, and the topology shown in Fig. 1b reflects a large fault current to the generation source. This paper aims to address the aforementioned shortcomings by proposing a new Z-source breaker topology which minimizes the reflected fault current drawn from the generation source while retaining a common return ground path. Comprehensive analyses, including minimum detectable fault current magnitude and ramp rate, component sizing, and frequency response, of the previously proposed and new Z-source circuit topologies are presented in Section II. In addition, manual tripping mechanisms, which enable protection under both instantaneous large current surges and longer-term over-current conditions, are introduced and analyzed in Section III. Finally, detailed simulation results of the proposed Z-source circuit breaker with extended protection schemes are presented in Section IV.

II. Z-source Breaker Overview

The Z-source breaker consists of an SCR, a pair of L-C legs, and snubber diodes and resistors. Different topologies of the Z-source breaker arise from different L-C configurations while maintaining the same operating principle. When a fault occurs, the fault current is supplied from both the load capacitor and the high-frequency conduction path through the Z-source capacitors as illustrated in red in Fig. 1. Note that the high-frequency conduction path through the Z-source capacitors, or the "shoot-through" path, is anti-series to the SCR forward current, which forces commutations if the Z-source capacitor current reaches the level of the Z-source inductor current.

The Z-source topology shown in Fig. 1a uses a crossed L-C connection and will therefore by referred to as the "crossed" Z-source configuration. The crossed Z-source topology requires an inductor to be placed in the return path of the dc source, which can be seen as a disadvantage in systems where a common ground is preferred. The Z-source topology shown in Fig. 1b places the L-C pairs completely in-line with the

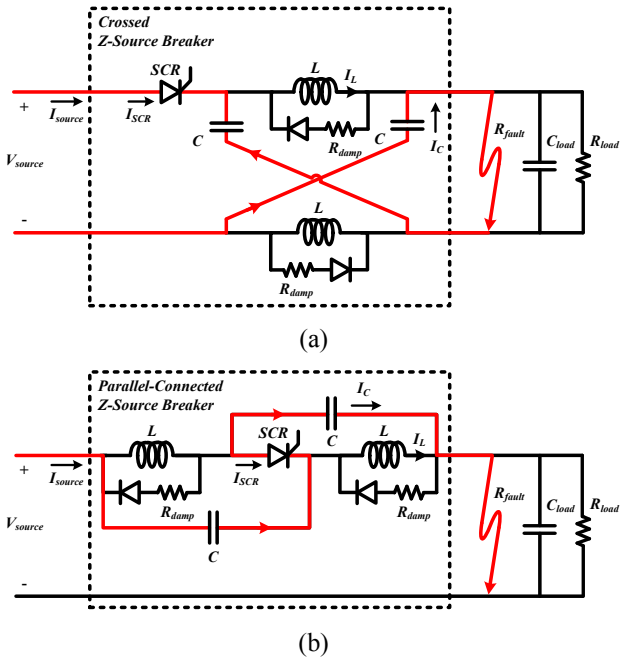


Figure 1. Previously proposed Z-source circuit breaker: (a) crossed Z-source topology and (b) parallel-connected Z-source topology.

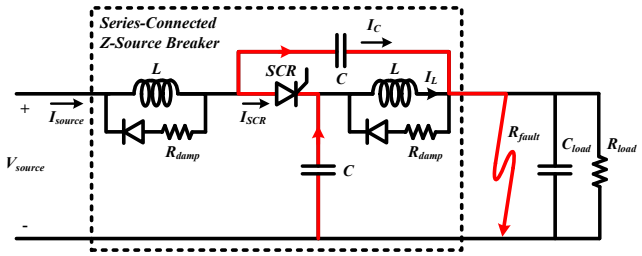


Figure 2. New series-connected Z-source circuit breaker topology.

power source to provide a common ground. This topology will be referred to as "parallel-connected" Z-source because the L-C legs are connected in parallel after the SCR commutates off. The parallel-connected Z-source topology allows for common ground connection between the source and all loads, but it reflects a large fault current at the source because the high-frequency conduction path through the Z-source capacitors is directly in-line with the source.

In order to preserve a common ground connection while reducing the amount of fault current reflected to the source, a new Z-source breaker topology is proposed and shown in Fig. 2. The source-connected capacitor in the parallel-connected topology is replaced by a shunt capacitor to ground. The new topology is termed **"series-connected"** because the L-C legs are connected in series once the SCR commutates off. The series-connected topology provides the fault current from an energy storage element instead of the source. Hence, the reflected current to the source during breaker operation is greatly reduced.

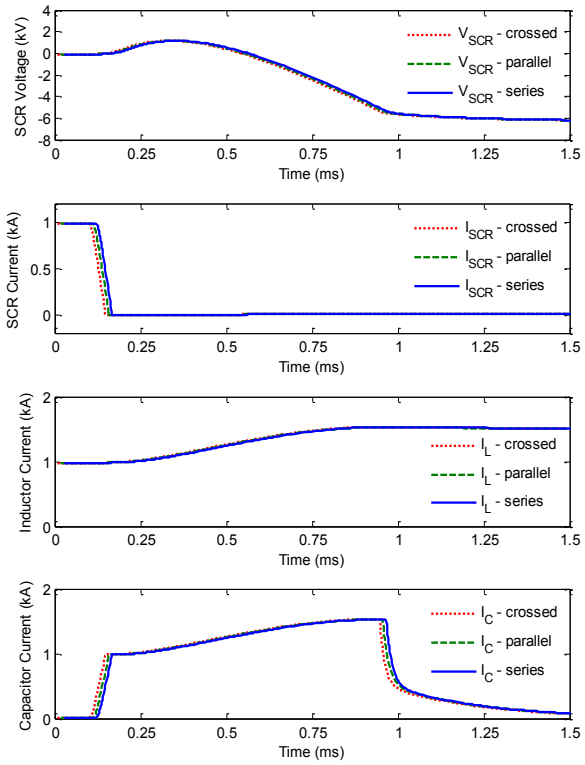
In the following sections, the transient fault response of the Z-source breaker is analyzed and a design methodology for component sizing is presented. While the majority of the analysis presented here is general and can be applied to all three Z-source configurations, some characteristics are topology-specific. Any distinguishing characteristic will be noted and compared among the three topologies.

A. Fault Clearing Waveforms

The full set of fault clearing waveforms for the three Z-source topologies is shown in Fig. 3. The waveform variables are as labeled in Figure 1 and 2. The simulated system has a source voltage of V_{source} = 6kV with a maximum load power of 6MW, i.e. a load resistance of R_{load} = 6Ω. The load capacitance is assumed to be C_{load} = 1mF, and the Z-source parameters are chosen to be C = 200μF and L = 2.4mH.

In the simulation, the system first operates under steady-state condition until a fault with conductance G_{fault} = $5\Omega^{-1}$ occurs near 100μs. It is assumed that the fault conductance ramps up linearly to the final value in Δt = 0.1ms, which translates to a fault conductance ramp rate of $50{,}000s^{-1}\Omega^{-1}$.

As shown in Fig. 3, the characteristic fault clearing waveforms – SCR voltage and current, Z-source inductor and capacitor currents – are shown to be identical across all three topologies. When the fault is introduced, the transient fault current will be supplied by both the Z-source capacitors and the load capacitor because the Z-source inductor current cannot change instantaneously. The Z-source capacitor current will increase until it reaches the Z-source inductor current. At this point, the SCR experiences a current zero-crossing and is allowed to commutate off naturally. Once the SCR turns off,



by 10μs and 20μs respectively for clarity.

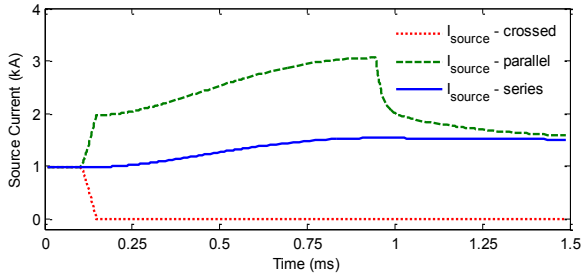


Figure 4. Comparison of the reflected fault current at the source among the three Z-source circuit breaker topologies.

the two L-C legs start a resonance where they supply the fault from their respective energy storage. This resonance will continue until the inductor voltage tries to become negative. At this point, the snubber diodes turn on to steer the current away from the capacitors, and the current will continue to flow in the snubber loop until the energy stored in the inductor decays to zero.

However, there are important differences in the amount of fault current reflected back to the source, as illustrated in Fig. 4. In the case of the crossed Z-source circuit breaker, the current drawn from the source equals the SCR current. Therefore, no fault current is reflected to the source as soon as the SCR commutates off.

In the parallel-connected Z-source breaker, the current drawn from the source during a fault interval equals the sum of the Z-source inductor and capacitor currents. Hence, in order to trip the Z-source breaker, the source must be able provide a transient current that is at least twice its maximally rated nominal steady-state current. This large transient current

requirement may be seen as a major disadvantage for this topology and may impose additional requirements on the input filter.

In the series-connected Z-source breaker, the high-frequency conduction path is intentionally directed away from the source by the use of a shunt capacitor. As a result, the current drawn from the source during a fault interval becomes the Z-source inductor current alone. This reduces the source transient current requirement by half compared to the parallel-connected topology.

B. Minimum Detectable Fault Magnitude

One important metric for characterizing a breaker circuit is the minimum detectable fault current, which is defined as the minimum amount of fault current required to trip the breaker. Since the Z-source breaker consists of frequency-dependent components, the minimum detectable fault magnitude must also be frequency dependent. However, for this analysis, the minimum detectable fault current across all frequency range is desired. Thus, an instantaneous load step is assumed for the following analysis.

For an instantaneous step transient in load current, i.e. with infinite fault conductance ramp rate, the current through the inductor leg during the fault transient can be assumed constant at the nominal load level while the Z-source capacitors and the load capacitor collectively supply the full fault current. The amount of the fault current supplied through the Z-source capacitor path can be calculated using the following capacitive divider ratio

$$i_C = \frac{C}{C + 2C_{load}} \cdot i_{fault} . \tag{1}$$

where C is the capacitance of the Z-source capacitor, C_{load} is the capacitance of the load capacitor, and i_{fault} is the fault current. Note that the in the crossed and parallel-connected Z-source topologies, the source inductance may have an effect on this ratio, whereas in the series-connected topology, the relationship is exact. Nevertheless, the impact of source inductance is small, and will be assumed to be negligible. Since the Z-source would not trip unless $i_C = i_L = I_{load}$, the minimum detectable fault current can be calculated as

$$i_{fault} > \left(\frac{C + 2C_{load}}{C} \right) \cdot I_{load} . \tag{2}$$

In other words, the fault conductance must be greater than the load conductance by the same factor, as illustrated in (3).

$$G_{fault} > \left(\frac{C + 2C_{load}}{C} \right) \cdot \frac{1}{R_{load}} . \tag{3}$$

For example, using the Z-source parameter values from the previous section, the breaker would not trip unless the fault current exceeds 11 times the nominal operating current. For slower transient faults, an even greater fault current is required because the inductor current ramps up along with the shoot-through capacitor current. Even in the limiting case where C is infinitely larger than C_{load}, the magnitude of the fault current must be at least equal to that of the nominal operating current. Therefore, the Z-source breaker offers no protection against, for example, a 20% overload condition.

The Z-source breaker offers limited longer-term over-current protection and is only effective in protecting against large transient faults. Thus, additional tripping mechanisms must be introduced for practical use of the Z-source breaker, as will be discussed in Section III.

C. Minimum Detectable Fault Ramp Rate

In addition to the minimum detectable fault current, the efficacy of the Z-source breaker is also limited by a minimum detectable fault ramp rate. The minimum detectable fault ramp rate is defined as the cutoff fault ramp rate below which the Z-source breaker would not trip regardless of how large the fault eventually becomes.

The inductance of the Z-source breaker plays a part in determining the minimum detectable fault ramp rate. However, even for a Z-source breaker with infinite inductance, there exists a fundamental limit on the minimum detectable fault ramp rate determined by the load resistance, the load capacitance, and the Z-source capacitance. In order to compute this limit, the analytical expressions for the output voltage and transient Z-source capacitor current will be derived while assuming an infinitely large Z-source inductor. The size of the inductor required to asymptotically achieve this minimum detectable fault ramp rate limit will then be derived in the next section.

In this analysis, the fault conductance is assumed to ramp linearly from zero to the final fault conductance linearly with a rate of

$$K = \frac{G_{fault}}{\Delta t} \tag{4}$$

where G_{fault} is the final fault conductance and Δt is the time interval for the ramp. The fault current can then be defined using the load voltage and the fault ramp rate as

$$i_{fault} = v_{out} \cdot K \cdot (t - t_0) \tag{5}$$

for $t_0 \le t \le t_0 + \Delta t$, where t_0 is the instant of time the fault occurs and v_{out} is the output load voltage. Without loss of generality, t_0 will be assumed to be zero, so (5) simplifies to

$$i_{fault} = v_{out} \cdot K \cdot t \tag{6}$$

for $0 \le t \le \Delta t$.

Assuming the source inductance is negligible and the Z-source inductor current and the load current remain constant, the amount of fault current supplied by the load capacitor can be calculated using a capacitor divider ratio between the load capacitor and the two Z-source capacitors. Therefore, a differential equation for the output voltage across the load capacitor can be written as

$$C_{load} \frac{dv_{out}}{dt} = -\left(\frac{2C_{load}}{C + 2C_{load}} \right) \cdot v_{out} \cdot K \cdot t . \tag{7}$$

Solving the above equation yields the following solution for the output load voltage

$$v_{out} = V_{source} \cdot \exp\left(-\frac{K \cdot t^2}{C + 2C_{load}} \right), \tag{8}$$

and the fault current then can be rewritten as

$$i_{fault} = V_{source} \cdot K \cdot t \cdot \exp\left(-\frac{K \cdot t^2}{C + 2C_{load}}\right). \quad (9)$$

Combining (1) and (9) yields the analytical expression for the Z-source capacitor current during the fault interval as shown in (10).

$$i_C = V_{source} \cdot K \cdot t \cdot \frac{C}{C + 2C_{load}} \cdot \exp\left(-\frac{K \cdot t^2}{C + 2C_{load}}\right). \quad (10)$$

Furthermore, the time at which the current is maximized can be solved as

$$t_{\max} = \sqrt{\frac{C + 2C_{load}}{2K}}, \quad (11)$$

and the maximum Z-source capacitor current during the fault interval is

$$i_{C,\max} = \sqrt{\frac{K}{2e \cdot (C + 2C_{load})}} \cdot C \cdot V_{source}. \quad (12)$$

In order for the Z-source breaker to trip, the Z-source capacitor current must reach the level of the nominal load current through the Z-source inductors during the fault interval. In other words, the maximum Z-source capacitor current must be equal to or greater than the nominal load current. Hence, the minimum detectable fault ramp rate K must be

$$K_{\min} = 2e \cdot \left(\frac{1}{R_{load} \cdot C}\right) \cdot \left(\frac{C + 2C_{load}}{C}\right) \cdot \left(\frac{1}{R_{load}}\right). \quad (13)$$

Equation (13) is intentionally written in an expanded form to illustrate the intuition behind this fundamental limit. The product of the last two terms from (13) is equivalent to the minimum detectable conductance from (3). So the minimum detectable fault ramp rate is determined by the minimum detectable fault conductance and the time constant set by the R-C product of the load resistance and the Z-source capacitance. Given the component values from the previous section, the minimum detectable fault ramp rate is approximately $8{,}300 s^{-1}\Omega^{-1}$.

When designing a Z-source circuit breaker, the minimum detectable fault current can be set by choosing the ratio of the load-to-Z-source capacitance. Then, by changing the capacitor sizes while holding their ratio constant, the minimum detectable fault ramp rate can be set. By increasing the Z-source capacitance, both the minimum detectable fault magnitude and ramp rate can be improved. However, the tradeoff is not only an increased capacitor volume, but also an increased inductance requirement to achieve this fundamental limit as will be shown in the following section.

D. Z-source Inductor Sizing

Having too little Z-source inductance would not allow the Z-source breaker to achieve the minimum detectable fault ramp rate, while having too much Z-source inductance adds unnecessary cost and volume to the design. In this section, the inductor current during the fault interval will be approximated and the inductance threshold where this current becomes negligible will be derived.

In order to avoid non-closed form solutions, i.e. error functions, the Taylor Expansions of (8) and (10) will be adopted for the following analysis.

$$v_{out} = V_{source} \cdot \left(1 - \frac{K \cdot t^2}{C + 2C_{load}} + \frac{K^2 \cdot t^4}{2(C + 2C_{load})^2}\right) + O\left(t^6\right) \quad (14)$$

$$i_C = \frac{V_{source} \cdot C}{C + 2C_{load}} \cdot \left(K \cdot t - \frac{K^2 \cdot t^3}{C + 2C_{load}}\right) + O\left(t^5\right) \quad (15)$$

By subtracting (14) from the source voltage, the voltage across the Z-source inductor can be derived, and the inductor current can be found to be

$$i_L = I_{load} + \frac{V_{source}}{6 \cdot L} \cdot \frac{K \cdot t^3}{C + 2C_{load}} - O\left(t^5\right). \quad (16)$$

Finally, combining (15) and (16) gives the current through the Z-source breaker SCR during the fault interval, as illustrated in (17).

$$\begin{aligned} i_{SCR} = I_{load} &- \frac{V_{source} \cdot C \cdot K}{C + 2C_{load}} \cdot t \\ &+ \frac{V_{source} \cdot K}{C + 2C_{load}} \cdot \left(\frac{1}{6L} + \frac{C \cdot K}{C + 2C_{load}}\right) \cdot t^3 - O\left(t^5\right) \end{aligned} \quad (17)$$

Equation (17) represents a conservative approximation in terms of the Z-source breaker operation because the capacitor current is underestimated and the inductor current is overestimated. In addition, the contribution of the inductor current relative to the capacitor current on the third order term is exposed. In order to achieve the minimum detectable fault ramp rate limit derived in the previous section, the inductor current must be negligible compared to the capacitor current. Thus, the following relationship must hold

$$L >> \frac{1}{6K} \cdot \left(\frac{C + 2C_{load}}{C}\right). \quad (18)$$

Plugging in $K_{\min}$ from (13) into (18) gives a minimum inductance required that would ensure the inductor current can be safely ignored for all detectable fault ramp rate K.

$$L >> \frac{1}{12e} \cdot R_{load}^2 \cdot C \quad (19)$$

Choosing an inductor approximately 10 times the limit derived in (19) gives the following expression for inductor sizing.

$$L_{\min} = \frac{1}{3} \cdot R_{load}^2 \cdot C \quad (20)$$

Equations (19) and (20) uncover an interesting relationship between the Z-source inductance and the load resistance. The inductance requirement can actually be relaxed as the nominal load increases, i.e. as the nominal load resistance decreases. Furthermore, it is shown that the required inductance is directly proportional to the Z-source capacitance.

Fig. 5 summarizes the relationship between the minimum detectable fault magnitude and the fault ramp rate. As expected, the minimum detectable fault magnitude increases as the fault ramp rate increases. The minimum detectable fault ramp rate is shown as the point when the required fault magnitude blows up. With the capacitor ratio fixed at 5, the

minimum detectable fault magnitude at high ramp rates is expected to be 11. The effect of the absolute capacitance on the minimum detectable fault ramp rate is shown by comparing the solid blue and solid red curves. The inductor sizing equation is verified by comparing the minimum detectable fault ramp rate using three different Z-source inductances. Very little improvement in minimum detectable fault ramp rate is achieved even when increasing the recommended inductor size from (20) by a hundredfold. Nevertheless, decreasing the recommended inductor size by a factor of ten causes a much more significant change in the minimum detectable fault ramp rate as illustrated in Fig. 5.

E. Constant Power and Resistive Loads

In the above formulation, the load current is assumed to be constant during the fault interval. However, in practical systems, a constant power load with high enough bandwidth would draw additional current as the output voltage drops. On the other hand, a resistive load would draw less current as the output voltage drops. To characterize the effect of this change in current on our analysis, the differential equation in (7) is modified to incorporate the additional current contribution.

$$C_{load}\frac{dv_{out}}{dt} = -\left(\frac{2C_{load}}{C+2C_{load}}\right)\cdot\left(v_{out}\cdot K\cdot t \pm \frac{V_{source}-v_{out}}{R_{load}}\right) \quad (21)$$

The plus-minus accounts for both constant power load and resistive load cases. In particular, the plus sign with additional current draw corresponds to the case with a constant power load with sufficiently high bandwidth, and the minus sign with less current corresponds to the case with a resistive load.

The solution to (21) is shown as a Taylor series, again to avoid working with non-closed form solutions and to illustrate the effect of having a finite load resistance:

$$\begin{aligned} v_{out} &= V_{source} \\ &- V_{source}\cdot\frac{K\cdot t^2}{C+2C_{load}}\cdot\left(1\pm\frac{2\cdot t}{3\cdot(C+2C_{load})\cdot R_{load}}\right) \\ &+ V_{source}\cdot\frac{K^2\cdot t^4}{2(C+2C_{load})^2}\cdot\left(1-\frac{2}{3K\cdot(C+2C_{load})\cdot R_{load}^2}\right) \\ &+ O\left(t^5\right) \end{aligned} \quad (22)$$

Comparing (22) and (14), the following two equations must hold so that the results derived under the constant current load assumption can be justified and applied in practical situations.

$$R_{load} >> \frac{2\cdot t}{3\cdot(C+2C_{load})} \quad (23)$$

$$R_{load} >> \sqrt{\frac{2}{3K\cdot(C+2C_{load})}} \quad (24)$$

For the time period of interest, i.e. the fault interval, (23) can be written in terms of the fault resistance and the fault ramp rate

$$R_{load} >> \frac{2}{3\cdot(C+2C_{load})\cdot K\cdot R_{fault}}. \quad (25)$$

Using the minimum detectable fault ramp rate and the minimum detectable fault magnitude, (25) can be simplified to

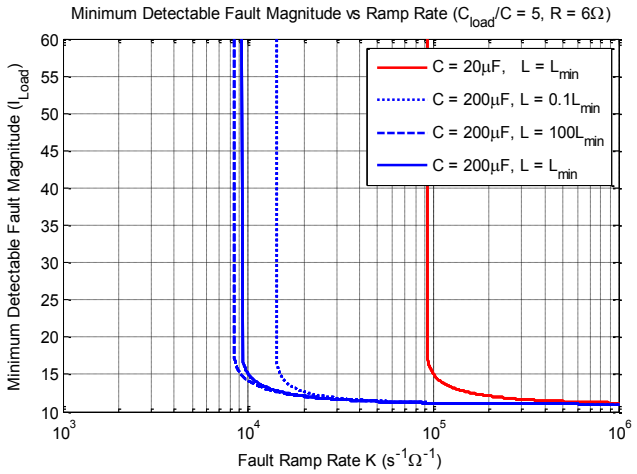


Figure 5. Minimum detectable fault magnitude vs fault ramp rate with fixed load to Z-source capacitor ratio of 5 and a load resistance of 6Ω.

$$R_{load} >> R_{load}\cdot\left(\frac{C}{(C+2C_{load})}\cdot\frac{1}{3e}\right), \quad (26)$$

which is guaranteed to hold regardless of the actual nominal load resistance. Using the component value from the previous section, the current contribution from the change in load current is only about 1.1% of the total fault current.

A similar condition can be derived from (24) by using the minimum detectable fault ramp rate, as illustrated in (27).

$$R_{load} >> R_{load}\cdot\left(\frac{C}{(C+2C_{load})}\cdot\frac{1}{\sqrt{3e}}\right) \quad (27)$$

Again, the inequality in (27) will always hold as the constant term is guaranteed to be less than one. If the Z-source capacitance is on the same order or less than the load capacitance, the current contribution from the load is constrained to about 10% of the total fault current. Using the component values before, the constant is evaluated to be 3.2%, which is again negligible.

F. Z-source Voltage Transfer Function

In this section, the filtering capabilities of the unfaulted Z-source circuit will be evaluated – the frequency response of each circuit not only indicates behavior as an input filter, either alone, or in conjunction with an explicit filter, but also highlights issues in input stability that may arise when dc-dc converters appear as a load. In contrast to the preceding sections where the analyses applied to all three topologies, the ac transfer functions are topology-dependent and will vary greatly among the three Z-source circuit topologies.

See [5] for a discussion of input filter design and the related stability for power converters. The following input-output voltage transfer functions are derived assuming a resistive load for illustration purposes. For other loads, the designer can quickly arrive at the appropriate transfer function by replacing R_{load} with a general Z_{load}.

$$H_{crossed}(s) = \frac{-s^2+(1/LC)}{s^2+(2/R_{load}C)\cdot s+(1/LC)} \quad (28)$$

$$H_{parallel}(s) = \frac{s^2 + (1/LC)}{s^2 + (2/R_{load}C)\cdot s + (1/LC)} \quad (29)$$

$$H_{series}(s) = \frac{(1/LC)}{s^2 + (2/R_{load}C)\cdot s + (1/LC)} \quad (30)$$

As shown in the above equations, all Z-source circuit topologies have unity gain with zero phase at low frequencies. This can be understood by observing the inductor conduction path while ignoring the presence of capacitors. However, the high-frequency behaviors are different due to the dissimilar capacitor configurations.

For the crossed Z-source topology, the crossed capacitor connections create a unity gain with 180° phase at high frequencies. For the parallel-connected Z-source topology, the capacitors form a high-frequency conduction path that results in unity gain with zero phase at high frequencies. As such, neither of these two topologies provides any filtering capability at high frequencies, so additional input filter will be required. In particular, the crossed Z-source circuit transfer function resembles that of a resonator and actually amplifies perturbations near the resonance frequency. On the other hand, the parallel-connected Z-source circuit forms a notch filter at the resonant frequency. The Bode plots for the two transfer functions are shown in Fig. 6a and 6b.

The series-connected Z-source circuit has a low-pass characteristic due to the shunt capacitor placement. Specifically, the transfer function is a second order low-pass filter with a quality factor of

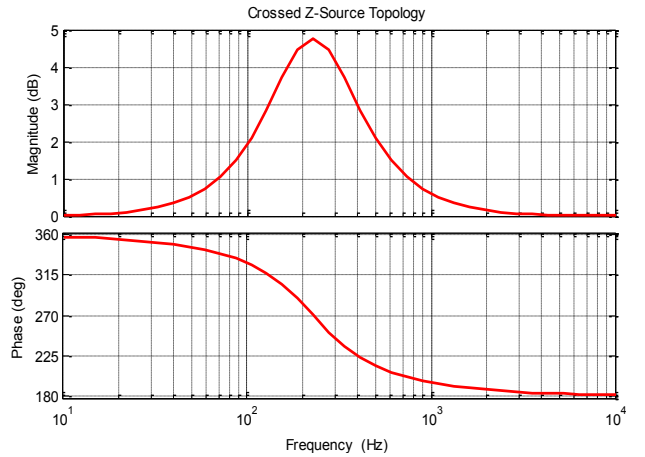
$$Q = \frac{R}{2}\sqrt{\frac{C}{L}}\,. \quad (31)$$

Using the recommended inductor sizing from the previous section, this corresponds to a quality factor of $\sqrt{3}/2$, which is slightly underdamped. The Bode plot is shown in Fig. 6c. For maximally flat frequency response, the recommended inductor size can be increased by 1.5 times. For critically damped frequency response, the recommended inductor size can be increased by 3 times.

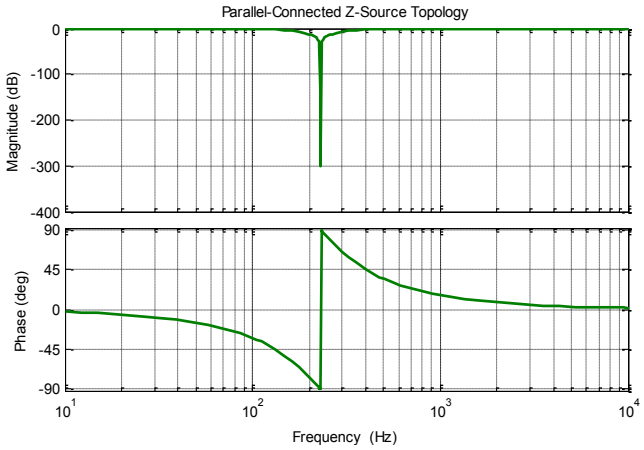
As discussed above, because the series-connected Z-source circuit topology offers inherent low-pass characteristic, it is possible to incorporate the input filter as part of the breaker. Along with other attributes such as a common ground connection and a low reflected fault current at the source, the new series-connected Z-source circuit topology is considered the most favorable among the three available topologies. As a result, the various enhancements proposed in the following section will be demonstrated on the series-connected Z-source breaker topology. Table I summarizes the key differences among the three Z-source circuit breaker topologies.

TABLE I. Z-SOURCE BREAKER TOPOLOGY COMPARISON

Features	Z-source Topology		
	Crossed	***Parallel***	***Series***
Common Ground	No	Yes	Yes
Fault Current at Source	I_{SCR}	$I_L + I_C$	I_L
Z-source Transfer Function	Resonator	Notch Filter	Low-Pass
Input Filter Integration	No	No	Yes



(a)



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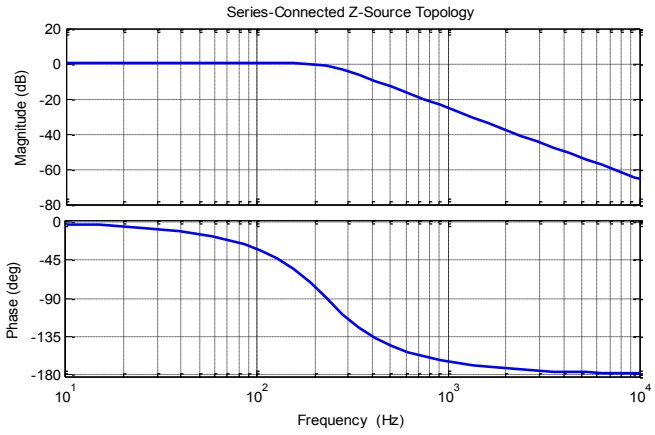

(c)

Figure 6. Input-output voltage transfer function of the Z-source circuit breaker assuming resistive load. Component values are R = 6Ω C = 200μF, and L = 2.4mH.

III. EXTENDED PROTECTION SCHEMES

Clearly, the Z-source circuit breaker can only protect against faults that exceed both the minimum detectable fault magnitude and the minimum detectable fault ramp rate thresholds. These faults are the most critical type and it is an

inherent advantage of the Z-source breaker that they can be handled automatically, in principle, without external detection. However, this only covers a subset of faults that can occur in practical systems. Additional detection and triggering schemes must be introduced to the Z-source circuit breaker to protect power systems from faults that satisfy only one or none of these two criteria.

A. Manual Tripping of Z-source Breaker

It is possible to trip the Z-source breaker manually via an artificially induced fault current. A sufficiently large and fast artificial fault current can force current commutation of the Z-source SCR. This can be accomplished by introducing additional controlled or semi-controlled devices into the breaker topology. The main artificial fault inducing mechanism must also be able to turn off safely after the SCR commutation occurs, i.e. the artificial short must not form a direct dc path from source to ground after turning on.

Two embodiments are illustrated in Fig. 7 where the additional components for manual tripping are shown in blue. In Fig. 7a, the artificial fault, with magnitude set by current limiting resistor R_{limit}, is induced at the same point where a natural fault would typically occur. This will be referred to as an external artificial fault. Moreover, it would be counter-productive if the induced fault is divided between the load and Z-source capacitors – the artificial fault current must again be 11 times the nominal load current using the component values in the previous section. Consequently, a blocking diode D_{block} is inserted into the design.

With the blocking diode present, the required artificial fault current becomes independent of the capacitor ratio and is reduced to twice the nominal load current. This can be understood by considering an artificial current larger than the nominal load current. By KCL, the artificial fault can sink current from three places: Z-source inductor, blocking diode, and Z-source capacitor. If the artificial fault current is larger than the nominal load current, it would have steered away the full Z-source inductor current, leaving no current through the blocking diode. The remaining current of the artificial fault must then come from the Z-source capacitor conduction path. The Z-source breaker would trip if the remainder current is at least as large as the nominal load current, thus arriving at the artificial fault current requirement of twice the nominal load current.

The artificial fault inducing element U_{AF} can be either a power transistor or an auxiliary SCR. In this arrangement, the fault inducing element does not form a direct dc path to ground once the Z-source SCR commutates off. So the current through in the artificial fault path will naturally decay to zero, allowing the transistor implementation to be turned off safely and the auxiliary SCR implementation to turn off naturally once the current drops below the SCR holding current.

In efficiency constrained designs, the additional diode conduction loss from the blocking diode during normal operation may be seen as a disadvantage. A different embodiment of the manual tripping circuit is proposed and shown in Fig. 7b to induce an internal artificial fault current. In this configuration, the portion of the induced fault current through the Z-source SCR, anti-series with the nominal load current can be found to be

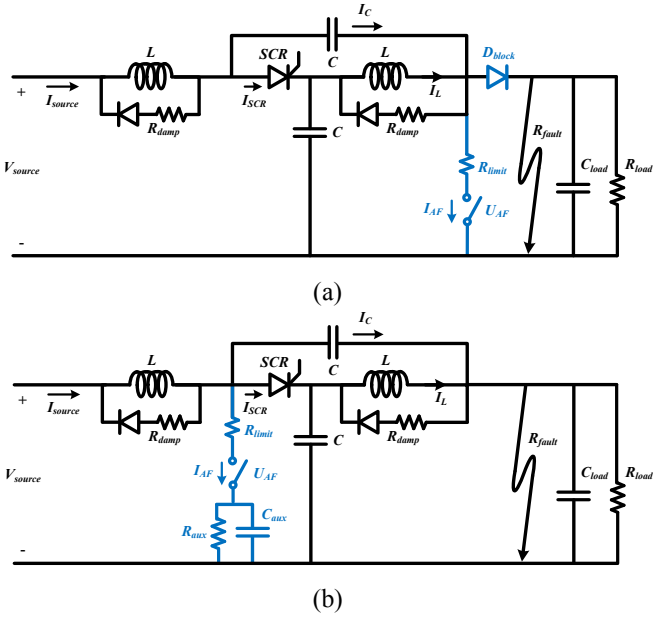

Figure 7. Two ways of manually tripping the Z-source breaker. (a) inducing an external artificial fault near the output and (b) inducing an internal artificial fault within the Z-source breaker.

$$\left(\frac{C+C_{load}}{C+2C_{load}}\right)\cdot I_{AF}\,. \tag{32}$$

The capacitive divider in (32) has a minimum of one half and a maximum of one. Hence, having an artificial fault of twice the nominal load current would guarantee that the Z-source breaker can be properly tripped to isolate the source.

The artificial fault inducing element U_{AF} can again be either a power transistor or an auxiliary SCR. The auxiliary resistor and capacitor are introduced to prevent the fault inducing element from forming a direct dc path to ground with the Z-source inductor. When an auxiliary SCR is chosen as the fault inducing element, the auxiliary resistor is chosen so that the current V_{source}/R_{aux} is less than the holding current of the auxiliary SCR. The auxiliary capacitor is then used to set the duration of the induced fault interval.

During normal operation, the auxiliary SCR is turned off and the auxiliary capacitor is completely discharged by the parallel auxiliary resistor. When a fault is detected, the auxiliary SCR is turned on to draw a surge of current to force commutation of the Z-source SCR. This current drawn by the auxiliary SCR will gradually decrease as the auxiliary capacitor is charged up. Once the current level drops below the SCR holding current, the auxiliary SCR naturally turns off and the auxiliary capacitor starts to discharge through the auxiliary resistor again, resetting the trip mechanism.

Similarly, a power transistor can be used as the fault inducing element. The power transistor is turned on for a fixed amount of time to force the Z-source SCR commutation. In this case, the capacitor is chosen to set decay constant to ensure that the current through the power transistor is sufficiently small by the end of the fixed artificial fault interval, allowing the transistor to be turned off safely.

While both embodiments shown in Fig. 7 require an artificial fault current of only twice the nominal load current,

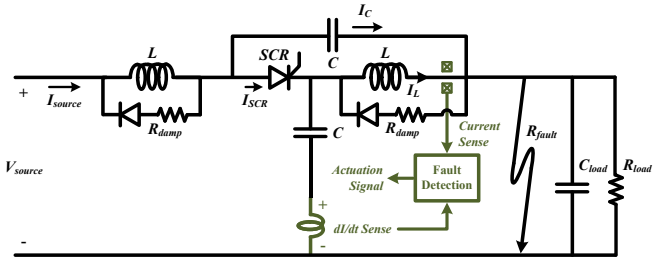

Figure 8. Fault detection sense nodes in a Z-source circuit breaker.

i.e. the current limiting resistor should be half the nominal load resistance, a greater artificial fault current may be needed in practice. For example, any delay in the fault detection and actuation control loop translates into time for the Z-source inductor current to increase from its nominal load level, raising the amount of current required to trip the breaker.

B. *Dual-Mode Fault Detection*

With means of manually tripping the Z-source breaker, additional fault detection schemes can be incorporated to protect against the types of faults that the Z-source breaker cannot deal with autonomously. Analogous in some respects to a "thermal-magnetic" breaker [6], faults in the power system can be detected using two methods: *dI/dt* and absolute magnitude *I*.

Fig. 8 illustrates the points of detection within a Z-source breaker. Instantaneous current surges can be detected via *dI/dt* by measuring the voltage across a small inductor or a transformer winding placed in series with the high-frequency conduction path. The small inductor must have an orders of magnitude lower inductance than the Z-source inductor in order to minimize its effect on normal Z-source breaker operations. The voltage across the small inductor in relation to the linearly ramped fault current can be approximated as

$$v_{sense} = -L_{sense} \cdot V_{source} \cdot K \cdot \frac{C}{C + 2C_{load}} . \qquad (33)$$

Even though the sense voltage is negative from a sense inductor, a transformer-based sensing scheme can easily flip the polarity while providing gain or attenuation as needed. Assuming the load is regulated and given the control bandwidth of the power regulator, the maximum current change rate induced by the controller is known. Any faster changing current transient should be classified as a fault, and the detection threshold can be calculated using (33).

Longer-term over-current conditions can be detected by monitoring the current through the Z-source inductor. This can be accomplished in various manners, two of which will be discussed here. First a high-side current sense resistor circuit can be placed in series with the Z-source inductor. This allows for accurate current reading at the cost of additional power loss and lack of galvanic isolation. Second, in power systems where efficiency is constrained or galvanic isolation is desired, a Hall Effect current sensor may be used in place of the current sense resistor.

IV. Extended Z-source Breaker Simulation

Two simulations are presented in this section to verify the operation of each manual tripping mode. The simulated

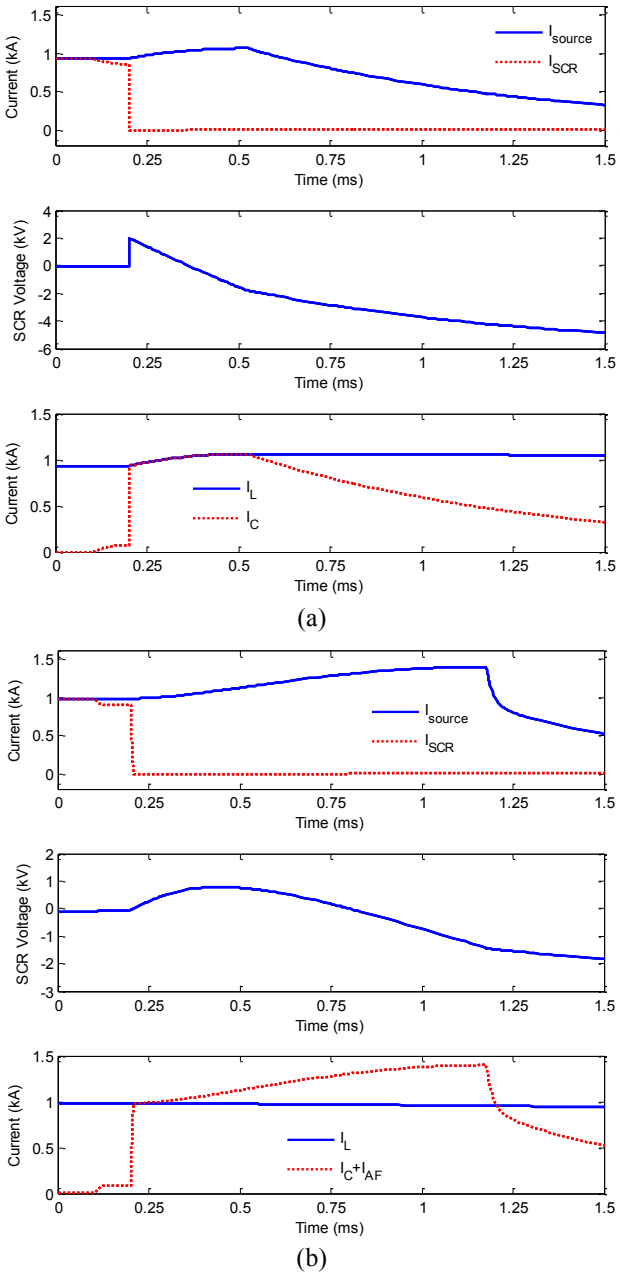

Figure 9. Fault clearing waveforms using manual tripping methods: (a) external artificial fault current and (b) internal artificial fault current.

system has a source voltage of V_{source} = 6kV with a maximum load power of 6MW, i.e. a load resistance of R_{load} = 6Ω. The load capacitance is assumed to be C_{load} = 1mF, and the series-connected Z-source topology is adopted with design values of C = 200μF and L = 2.4mH. The simulated waveforms are shown in Fig. 9 and the waveform variables are as labeled in Fig. 7.

In the simulation presented in Fig. 9a, the external artificial fault inducing mechanism from Fig. 7a is used with a limiting resistor of 2Ω. A value less than half the nominal load resistance is used to provide some margin in case the Z-source inductor current was given time to deviate from the nominal load level. The system experiences a transient fault of

R_{fault} = 6Ω at 100µs, which is not sufficient to trip the Z-source breaker automatically; only a small dip in the SCR current is observed. However, by inducing an external artificial fault, the breaker can be tripped successfully to isolate and protect the source as shown in Fig. 9a. Manual tripping occurs near 200µs to emulate a 100µs delay in the fault detection and actuation control loop.

Similarly, the internal artificial fault inducing mechanism from Fig. 7b is used in the simulated fault clearing waveforms shown in Fig. 9b. A limiting resistor of 2Ω is again used in this system. The auxiliary capacitor is set to be 200µF to set the fault interval time constant to 0.4ms and the auxiliary resistor is set to 6kΩ to limit the turn off current to be 1A. The system again experiences a transient fault of R_{fault} = 6Ω at 100µs, and the internal artificial fault is induced at 200µs. The sum of I_C and I_{AF} can exceed I_L in this configuration because additional current is drawn from the source as illustrated in Fig. 9b.

A final simulation illustrates the effect of the sense inductor and verifies the approximation in (33). The same Z-source component values are used, and the system experiences a transient fault of $G_{fault} = 5\Omega^{-1}$ with a fault conductance ramp rate of $50{,}000s^{-1}\Omega^{-1}$. Note that this fault is detectable and will trip the Z-source breaker automatically.

The simulated results shown in Fig. 10 compare the fault clearing waveforms with and without an additional sense inductor of 2.4µH placed in the high-frequency conduction path as illustrated in Fig. 8. The sense inductor is chosen to be 3 orders of magnitude less than the Z-source inductor. As shown in Fig. 10, the fault clearing waveforms are nearly identical during the fault interval. Finally, the sense inductor voltage is shown to exceed the calculated value of -65V from (33) due to higher order effects. Thus, the approximation presented in (33) is conservative and the detection system will not make false negative type errors.

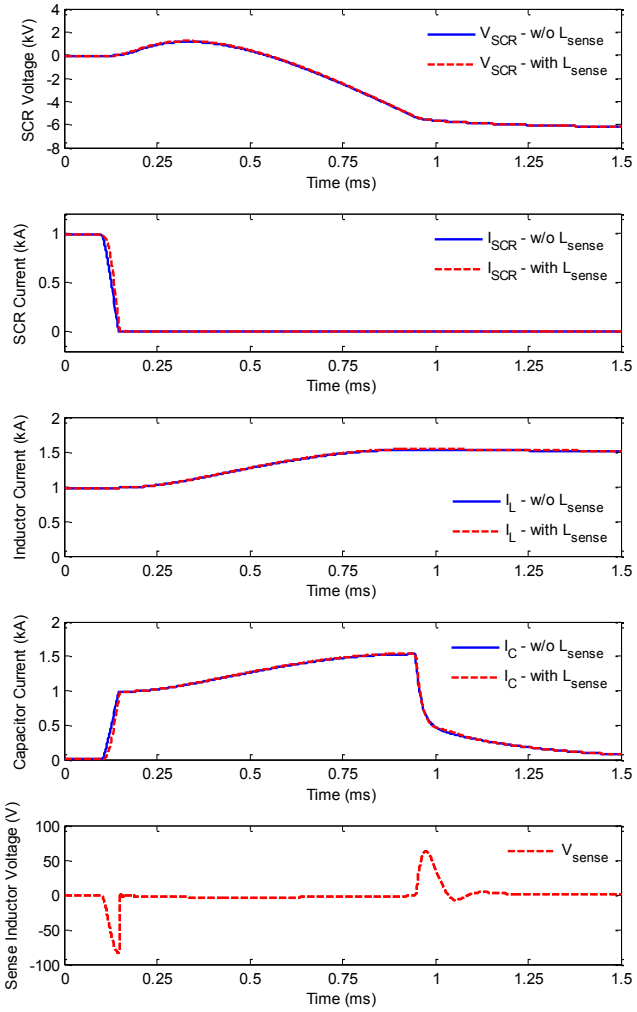

Figure 10. Fault clearing waveforms demonstrating negligible effects from the current sense inductor on the normal operation of the Z-source breaker.

V. Conclusion

The Z-source circuit breaker topology has promise in protecting against faults in dc power distribution systems by creating a natural current zero-crossing. This breaker could be used to protect all sorts of dc distribution, including renewable arrays, e.g., solar installations. This paper presents a comprehensive analysis and design methodology of the Z-source circuit breaker and proposes a new series-connected topology to maintain a common ground connection while mitigating the problem of reflected fault current at the source. Manual tripping mechanisms along with fault monitoring methods are introduced to enable "dual-mode" protection against both instantaneous large surges in current and longer-term over-current conditions.

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