Teaching Modeling, Control, and Simulation in a Modular Kit for Power Electronics

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***Abstract*—We introduce an educational kit to teach modeling, control, and simulation through power electronics. This hands-on kit consists of a power converter and controller, and is built using discrete electronic devices. Our proposed strategy in this paper is to use the kit to help guide students in system modeling by dividing the process into different levels of model abstraction: system-level, control-level, behavioral-level, and device-level. This strategy is illustrated through design examples utilizing circuit blocks from the kit.**

I. Introduction

System modeling and design is fundamental in engineering, especially power electronics. We have developed an educational kit that serves as an experimental platform to help teach modeling, control, and simulation in power electronics within a robust system design strategy. Much of today's engineering education focuses on ensuring that students understand numerous technical concepts, and perhaps apply these concepts in course projects or laboratories to build systems that perform some function. However, little or no attention is generally given to the iterations the students perform in the system design process. As a result, many new engineering graduates enter industry lacking a proper system design methodology. For example, it is common for electrical engineering undergraduates to learn about basic circuit design techniques and topologies, and implement some circuits with discrete components. However, the fact that a proper modeling and system design approach is often not emphasized as a teaching objective leads students to various undesirable engineering practices, such as repeatedly "tweaking" component values and iterating on simulations, attempting to simulate the entire system all at once, which in large projects is intractable. This paper's approach to modeling and design in the context of a teaching kit aims to promote better system design.

Along with teaching modeling and simulation, the educational kit, which is inspired by the UC3842 power electronic controller shown in Figure 1, provides an invaluable hands-on experience. The actual building within the platform and the modularity of the circuit blocks gives significant insight on interconnections, board parasitics, current flow, grounding and layout, device variations and nonidealities, among others. These aspects will not be elaborated further in this paper, as the focus will be on the proper incorporation of modeling and simulation in the design of large complicated systems.

It is without a doubt that simulation has taken a major role in modern system design not only in circuit design and power electronics, but also in most, if not all, other engineering disciplines. The advancements in computing power have made computer simulation a very powerful tool; its speed and ease can make it a pedagogical crutch to learning, and of great value to industry [1]. At the same time, systems continue to grow in complexity, and especially at the forefront of technology, system complexity tends to outpace the power of simulation. Moreover, simulations are based on mathematical models of different physical processes, which themselves contain many assumptions and limitations. Students should therefore keep in mind that simulation by itself is not enough, and can arguably waste significant time if it is not incorporated within a proper system design methodology.

It is crucial that instructors help students understand the role of simulation in the design process by keeping it as a teaching goal. Students should know, for instance, that hand calculations serve as a first order model of the system, whether this is achieved by performing linearizations about fixed operating points through small-signal analysis, or by idealized functions, such as in translinear circuits. Computer simulations provide extra levels of model complexity, depending on the device models used, which leads to the inherent tradeoff between simulation time and model accuracy. With that in mind, students would be mindful that running the whole controller as in Figure 1, for example, through a time-domain transient simulation is not wise. Simulation, with all its power in computation and algorithms, requires a degree of sophistication in system-level thinking and problem partitioning.

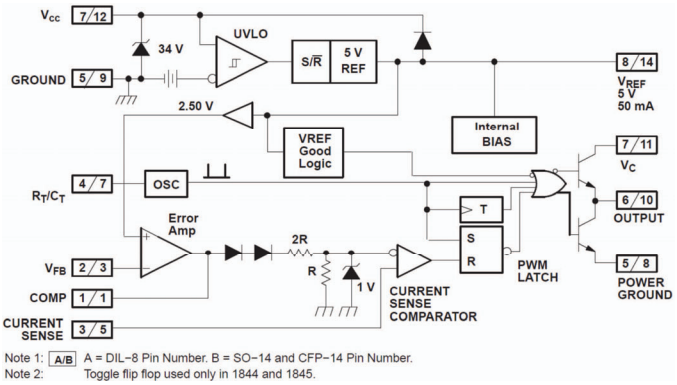

Fig. 1. The venerable Unitrode UC3842 provides the inspiration. The UC3842 has been used as a controller building block for many classically controlled power converters [1], [2].

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The strategy that we propose in this paper is to use the kit to help guide the students in system design, modeling, and simulation by dividing the process into different levels of model abstraction: system-level, control-level, behavioral-level, and device-level. The final objective of the syllabus is to have a fully functional power electronic controller that is built using only discrete electronic devices: transistors, capacitors, and resistors. Without a proper design process, this is unattainable because of a naive preoccupation of a simultaneity of design details. With the proposed design strategy, students analyze the power electronic controller kit at each model level and identify the parts of interest and their functionality at that model level. This emphasizes the need for a *top-down* approach when defining and organizing the whole system and its requirements, as well as a *bottom-up* approach when analyzing technological capabilities (i.e. what is possible) and specific functionality.

The use of hands-on kits and platforms on which educational experiments are conducted has been continually evolving over the recent years [3], [4], [5], [6], [7], [8]. Examples vary from a buck converter to drive an electric motor of a solar model car [5], to a reconfigurable educational platform for fast experimentation with different power converter topologies [4], to an educational system for controlling power electronics systems with digital signal controllers (DSCs) [9], among others. Hands-on projects reinforce the concepts given in lecture, and provide more insight on various design issues that may not be obvious in theory. There is generally a great demand in the industry for the skills acquired from these educational platforms [3], [5].

The fact that power electronics is a multidisciplinary field makes the power electronic controller kit a platform for teaching not only classical concepts in power electronics, but also integrated circuit (IC) design [1], as well as classical control theory.

The paper is divided into five sections. Section II provides a description of the kit and the circuit blocks. Section III lays out the proposed system design methodology, and section IV provides three design examples on how this methodology can be educational. A conclusion is given in section V.

II. Kit Description

It can be seen from Figure 1 that the UC3842 current-mode controller consists of several subcircuits that perform different functions. These different functions, along with additional ones, were realized in different circuit boards in the kit, each carrying out a specific function. Figure 2 shows an overall view of the power controller kit. A wooden case houses the motherboard on which the controller blocks are mounted. The motherboard has female pin connectors to which the circuit blocks plug. Pin sockets are used for all components not only to minimize soldering, but also to provide design flexibility and ease in replacing components. Figure 3 shows a sketch of the different circuit blocks in the kit.

The modularity in the kit design is easily noticed. Each module can be isolated and tested independently. Individual modules can be easily replaced if they are damaged, or if the board is updated. In addition, the fact that pin sockets are used for component placement makes the modules reusable, thereby significantly reducing the operating costs in the long run.

Fig. 2. An overall view of the power electronic controller kit. The wooden box houses the motherboard, on which the various controller circuit blocks are mounted. The box also has a place for storing the kit components.

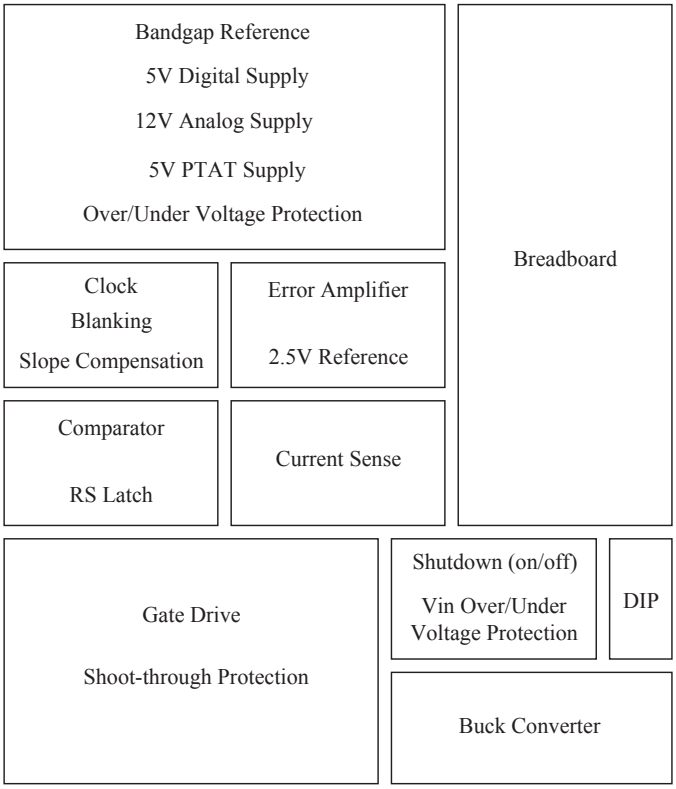

Fig. 3. Power electronic controller modules [1]. This clearly shows how the controller functionality is organized into different circuit blocks, each performing a specific function. The modularity in the kit design is clearly noticed.

All the designs are created using common discrete electronic devices, which are readily available and inexpensive. These include the well-known and characterized 2N3904 and 2N3906 NPN and PNP bipolar junction transistors (BJTs), respectively, and 2N7000 N-MOSFETs, among others. This gives substantial insight on deeper transistor-level circuit operation, making the kit a great tool for teaching IC design [1]. Test points to which instrumentation and oscilloscope probes may be clipped are available on most of the nodes, thus providing access to and insight on almost every part of the controller circuit. The

grounds and other connections of the different modules are also fully configurable, allowing many possibilities for testing. Furthermore, the kit contains a breadboard for optional external circuitry to interface with the controller circuit blocks.

The controller is used to operate a buck converter, as shown in Figure 3, and consists of the following modules:

- ***Bandgap and voltage references***: this block provides the different voltage levels necessary for the operation of the other controller circuit blocks. It provides a 5V supply for the digital blocks, a 12V supply for the analog blocks, and a 5V proportional to absolute temperature (PTAT) supply to generate PTAT current sources in other circuit blocks.
- ***Clock, leading-edge blanking, and slope compensation***: this block generates the clock pulses necessary for commanding the gate drive circuit and for setting the switching frequency of the power converter switches. It also provides leading-edge blanking to prevent false turn off of the high-side switch of the converter due to an initial current impulse [2], and generates the ramp voltage needed for slope compensation, which is crucial in current-mode control with duty cycles over 50% [10].
- ***Current sense amplifier***: this block provides a measure of the high-side switch current by amplifying the voltage across a sense resistor. Thus, it also provides the controller with a measure of the instantaneous inductor current while the high-side switch is on.
- ***Error amplifier***: this block implements the controller transfer function, and dictates the maximum inductor current value allowed before the high-side switch turns off, i.e. it provides inductor current command to the power stage. For example, this module can implement a proportional-integral (PI) controller, or perhaps some other controller, depending on the compensation network configuration used.
- ***Comparator and RS latch***: this block is responsible for deciding which state the converter must be in, i.e. whether the high-side or low-side switch should be on. The comparator toggles as soon as the measured inductor current reaches the maximum current dictated by the controller, thus turning the high-side switch off. The RS latch holds the state of the converter until the next clock pulse, at which the converter state changes back, turning the high-side switch back on.
- ***Gate drive circuitry***: this block receives the current state of the converter from the comparator and latch board, and provides the gate voltages required to turn the power switches on or off. The block also includes shoot-through protection circuitry to prevent the two switches from turning on at the same time. Moreover, the gate drive board checks whether the shutdown signal is asserted by the shutdown board, in which case the gate driver turns off both power switches.
- ***Shutdown and protection circuitry***: this block ensures that the input of the power converter is within the allowable limits. If the input voltage is too low or high, the shutdown signal is asserted, and the gate drive turns off both power switches. The shutdown board also includes the option of asserting the shutdown signal through a mechanical switch.
- ***Buck converter***: this block contains the power stage with the power switches and filtering needed to meet given output current and voltage ripple specifications. This block is where signals such as the inductor current and output voltage are fetched from.

Although the focus of this paper is on teaching modeling, control, and simulation through the power controller kit, it is important to highlight the importance of the hands-on aspect of the kit. The learning outcomes acquired from applying theoretical concepts in power electronics and control theory to actual circuits, and experiencing the system design process starting with back-of-the-envelope calculations and ending in a fully functioning system cannot be paralleled by those that result from most other teaching methods. The whole process engraves various skills in the hands and minds of the students, which otherwise would not have been possible without the hands-on aspect. It develops intuition and a feel of why and how different parts of the system behave the way they do, and this proves to be invaluable in the engineering industry. This is one of the main reasons why teaching engineering system design methodology within the context of power electronic control can be of great benefit.

III. Model Abstraction Levels

The system modeling strategy that we propose is to divide the process into different levels of model abstraction: system-level, control-level, behavioral-level, and device-level. This essentially structures the way students think about and analyze the given system. If properly applied, these model abstraction levels should prevent students from "getting stuck" in dealing with details of the design that are impertinent at the early stages of the system design process.

A. System-Level Model

The first level of model abstraction that students should understand is the system-level model. At this point, students have a high-level overview of the whole system. Students at this model level are encouraged to ask themselves fundamental questions such as, "What does the system consist of?" Or, "What does this system do?"

When the kit is presented at the system-level, students identify the buck power stage and the controller as the two subsystems that comprise the entire system. At this point, students should understand the basic functionality of each system, and how its role fits in the operation of the entire system.

For the power stage subsystem, students can be exposed to the topology of the converter. In addition, depending on the requirements, students can set their own specifications or understand the specifications provided to them. For example, the kit's buck converter is supposed to work with a 10-20V input voltage, and must deliver a steady output voltage of 5V. Students are free to set reasonable requirements for the output current and voltage ripples, as well as the switching

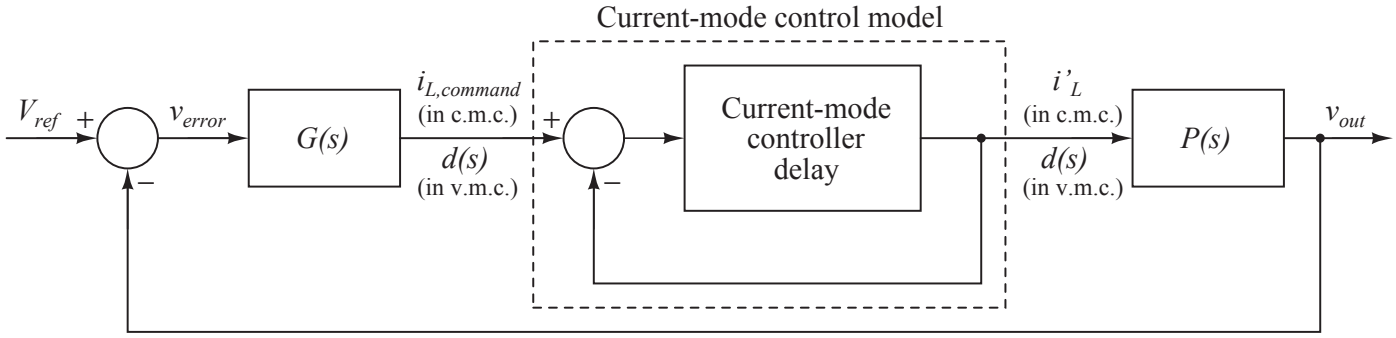

Fig. 5. Control-level model of the power controller kit. $G(s)$ corresponds to the controller which commands the maximum inductor current in c.m.c. or duty ratio in v.m.c.

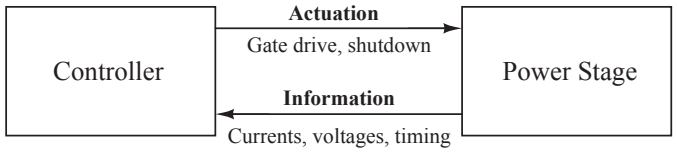

Fig. 4. System-level description of the power controller kit. The subsystems are identified, and the information flow between them is understood.

frequency of the converter switches. However, it is important to note that at this stage, students should not be concerned about *how* these specifications are met, or any further implementation details. The emphasis in the system-level model is on understanding the fundamentals of the system, identifying its main subsystems, and understanding its specifications and main functionality.

As for the controller subsystem, students can observe that it is a peak current-mode controller, and should understand that it controls the generation of pulse width modulation (PWM) signals, thereby controlling how often the converter switches turn on and off. Students can use this as an opportunity to think about the options available for controlling the converter, i.e. current-mode or voltage-mode control, but without yet being concerned about the peculiarities of the dynamics.

It is important to also understand how the roles of the individual subsystems are related to each other and how they all fit into the operation of the whole converter. The controller subsystem cannot function properly without obtaining information on inductor current, output voltage, and switch turn on/off timings from the power stage. Similarly, the power stage will not deliver power to the output without the PWM signals and the gate driver in the controller subsystem. This is an example of why a combination of a *top-down* and a *bottom-up* approach to system design is necessary. Figure 4 illustrates the system-level model.

B. Control-Level Model

After gaining understanding of what the system is and what it should do, students move on to the next model level, namely the control-level. At this level, students analyze each subsystem identified in the system-level model from a controls perspective. This is done by identifying the subsystem's main constituents (plant and controllers) and their interconnections in the form of block diagrams, each having inputs, a transfer function, and outputs [11]. Students identify the control structure and the relevant state variables. This could be an opportunity for students to not only learn about averaged power converter models and their transfer functions, but also explore differences in the dynamics of voltage-mode control (v.m.c.) and current-mode control (c.m.c.) [10], [12].

For example, students should be able to identify the kit's buck power stage as the plant to be controlled, and must understand the difference in the relevant states in v.m.c. and c.m.c., and the effect this has on the buck power stage transfer function:

$$P(s) = \begin{cases} v_o(s)/i'_L(s) & \text{in c.m.c.} \\ v_o(s)/d(s) & \text{in v.m.c.} \end{cases}$$

Students see at this point how current-mode control simplifies the buck transfer function to first-order, as opposed to second-order in the case of v.m.c. Students should be to come up with a control-level model similar to the one shown in Figure 5.

After identifying the plant and controller blocks, as well as the relevant state variables, and after deriving the relevant transfer functions, students should analyze the assess the different options for the design of the controller. One of the most critical teaching objectives at this model level is understanding design for stability and performance. Students understand that there is a trade off between the two, and proper design should be a compromise between stability and performance, depending on the system requirements [11]. Bode plots are introduced as tools to help visualize system response characteristics in frequency domain, and the step response is introduced as a means to observe the time domain system response to a step in the input.

Students are encouraged to study the effect of parameter variation on the various response characteristics of the system. Phase margin should be identified as a metric for relative stability, and students should be able to easily read it off the Bode phase response plot. Moreover, students should also note the effect of parameter variations on the performance metrics, such as over-shoot, settling time, and steady-state error. Based on these metrics, students should be able to come up with controller parameters that fit the design's stability and

performance requirements. Figure 6 shows an example of how variation in certain parameters can affect the phase margin (PM), causing significant ringing.

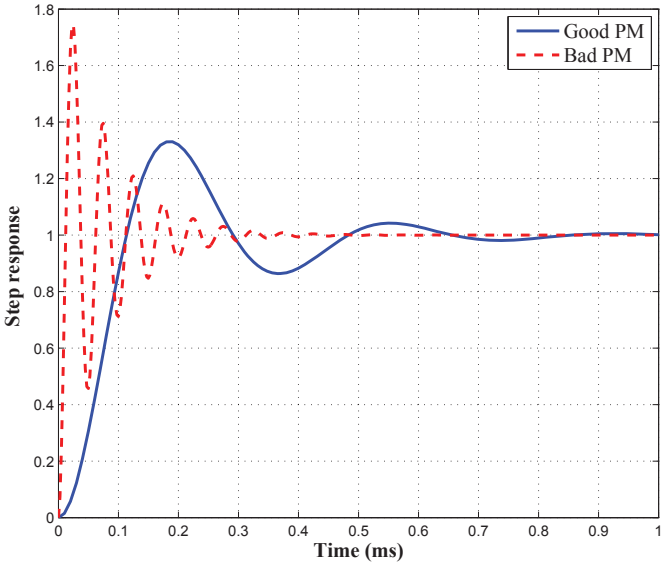

Fig. 6. An example of a closed-loop transfer function plot of a controller design with good phase margin, and one with poor phase margin.

A possible controller to use for the kit is a PI controller, with an additional pole to attenuate higher frequency components and thus provide lead compensation in addition to the PI controller. Bode plots of the loop transmission of the model in Figure 5 are shown in Figure 7. The controller, which corresponds to $G(s)$ shown in Figure 5, commands inductor current. In this model, the controller commands the peak inductor current allowed, beyond which the high-side switch of the buck power stage is turned off. The variation in the inductor current, denoted by i'_L in Figure 5 is estimated by measuring the current of the high-side switch.

Note that other circuit blocks, such as the voltage regulator and the bandgap reference, also utilize local feedback. Similar analysis can also be performed so that proper stability and performance is ensured.

C. Behavioral-Level Model

After the analysis of the control aspect of the system through the control-level model is completed, the next step is to devise circuit implementations of the subsystems. At this level, students translate the blocks whose dynamics have been analyzed into circuit blocks that are readily available in SPICE libraries (e.g. LTSpice), such as operational amplifiers, comparators, idealized switches, clock generators, and digital logic. The detailed transistor-level implementation of these blocks are irrelevant in this model level. The objective at this stage is to design circuits whose dynamics match the expected behavior that was analyzed at the control-level model.

A possible behavioral-level model of the power controller kit is shown in Figure 8. This model uses operational amplifiers, a comparator, and some digital logic, as a first pass behavioral design to implement the controller.

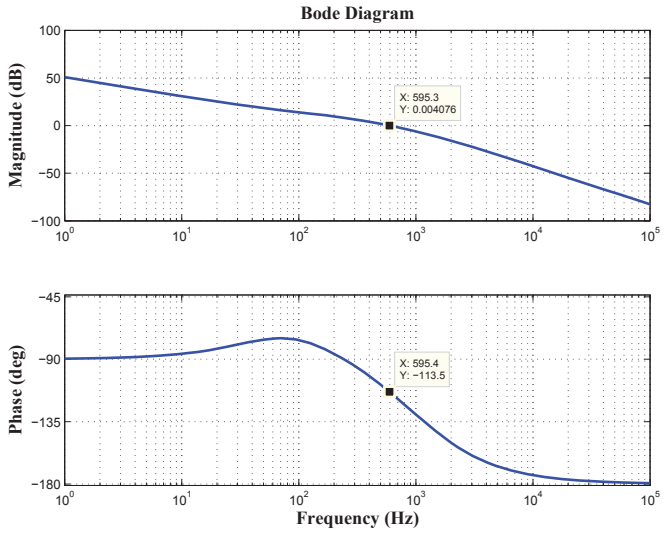

Fig. 7. Bode magnitude and phase plots of the control loop transmission. The phase margin can be easily read off the Bode phase plot as the difference between the phase at unity gain and -180°. In this case, there is 66.5° of phase margin.

The functionality of the controller can be demonstrated using SPICE simulations. Students are encouraged to perform both time-domain and frequency-domain simulations on the various portions of the behavioral model using transient and ac analysis. Important teaching objectives can be established during simulations at the behavioral-level model. Students need to design test circuits in order to be able to run a successful simulation with meaningful results.

Students should note, for example, that if there are circuit blocks that are implemented in open-loop configuration, then closing the loop around that block for testing purposes is necessary. Otherwise, students may end up with erroneous frequency response characteristics and wrong gain values due to the saturation of the amplifier. In addition to this, it is crucial that students devise test circuits that have proper conditions for providing a well defined dc operating point. This is important not only in dc bias point simulations, but also in ac small-signal analysis, where a fixed dc operating point is needed.

A possible test circuit for the error amplifier block, which

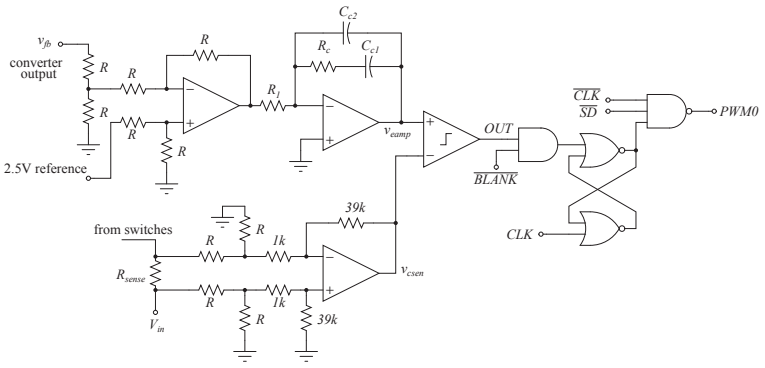

Fig. 8. Behavioral model of the controller kit. The control functionality is implemented using idealized blocks as a first pass behavioral design.

is part of the behavioral-level diagram in Figure 8, is shown in Figure 9. The fact that there is a pole at the origin means that the gain is undefined at dc, and thus the dc operating point is ill-conditioned. A large feedback resistor can be added to keep a finite dc gain. However, the offset voltage of the operational amplifier can saturate the amplifier if it is not accounted for. One solution is to place a large capacitor in series with R_1, as shown. One can also correct the offset by adding a voltage source at one of the operational amplifier inputs, and tweaking its value. At the behavioral-level model, students should be able to characterize the various circuit blocks using simulations.

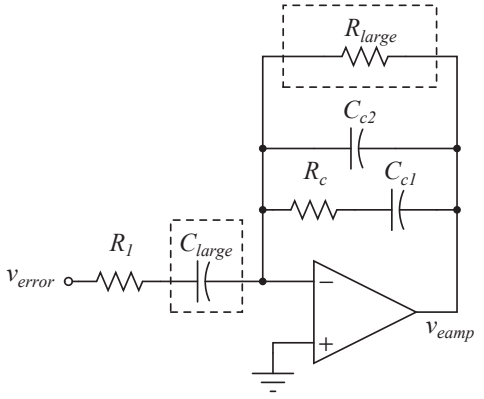

Fig. 9. A possible test circuit for the error amplifier implementation in Figure 8. The components shown in the dashed boxes ensure a stable dc operating point.

D. Device-Level Model

The last model abstraction level is the device-level. As mentioned earlier, one of the outcomes of having the hands-on kit is that students can learn circuit design through the different and diverse circuit blocks available. At this model level, all the circuit blocks such as operational amplifiers, comparators, clocks, and other blocks are implemented using transistors and passive components. No integrated circuits or any built-in blocks were used in the design of the power controller kit's circuit blocks. Students use devices that are readily available, such as 2N3904 and 2N3906 NPN and PNP BJTs, respectively, as well as 2N7000 N-MOSFETs and ZVP3306A P-MOSFETs.

After the device-level circuits are designed, it is important to verify that the functionality of the transistor-level circuits match that of the circuit blocks analyzed in the behavioral-level modeling stage. Once again, students should perform transient and ac analyses, and compare the time-domain and frequency-domain simulation results between those at the behavioral-level and device-level.

As part of the learning process, it is also equally important to compare the simulation results against the expected ones from hand calculations. Back-of-the-envelope calculations provide reasonable intuition on how and which components influence certain metrics and specifications, but students have to be aware of the approximations and linearizations that are assumed. Simulations provide nonlinear and more complex device modeling, but should agree, to a first order, with what students expect from their hand calculations.

One of the most important skills circuit designers possess is their knowledge of device parasitics and how they can impact the design. The device-level modeling stage can be an opportunity for instructors to shed light on this topic, and illustrate examples of how certain parasitics can severely affect the circuit behavior. These parasitics, in fact, become only apparent at the device-level model. For example, a behavioral-level model of the buck power stage would use ideal switches, and these switches do not capture the actual power device parasitics, such as gate capacitance as well as rise and fall times.

Students should always keep the previous model levels in the back of their minds. Due to the iterative nature of design, students are expected to continually go back and forth between the different model levels. Moreover, it is also important to keep in mind that all models, at all model levels, have their limitations; the more accurate the model is, the more time it takes for it to produce the results. There is an inherent tradeoff between model fidelity and simulation time that students should keep in mind.

IV. Design Examples

The following section contains examples that not only present interesting teaching goals which can be achieved through some of the kit's circuit blocks, such as the voltage regulator, but also point out some of the issues that students may encounter while applying the proposed design methodology. For example, it is important to note that it is not necessary that every circuit appears in all model levels. Utility circuits such as the bandgap and voltage references circuit block form a significant block that is needed for the operation of almost all other blocks, but in terms of dynamics, does not pertinently show up at the control-level model of the power controller. In addition to this, it is emphasized that sometimes certain differences between experimental and SPICE-simulated results can and will occur. Students need to be able to account for and explain the reasons why the experiment differs from their model, whether it is due to differences in device parameters, PCB layout issues, or some other reason. The clock circuit serves as an example of how and why this can happen.

A. Voltage Regulator

The voltage regulator circuit is a simple and illustrative way to use operational amplifiers. It involves one of the most basic control strategies that can be taught to students, namely dominant pole compensation [11]. This can be an opportunity for instructors to use this block to teach and experiment with various control methods. Furthermore, from a circuit design perspective, the voltage regulator introduces prevalent circuit blocks, including current sources and differential pairs. Concepts of feedback, compensation, and loading can be introduced and analyzed using this circuit block.

In addition to this, more advanced concepts such as the analysis and modeling of the regulator when a step in the load is applied can also be illustrated here. Instead of using the regulator response to a step in the bandgap voltage as the performance metric, the regulator's response to a load step is used. Students can learn how this can be modeled as a constant current perturbation for the system to remain linear and time

invariant. This can be illustrated in a control-level model, as shown in Figure 10.

Next, a behavioral-level as well as a device-level model can be created. Figure 11 shows these models (load resistor R_L is excluded to avoid confusion). These models can all be simulated and have their results compared with each other. The result of the device-level load step simulation is shown in Figure 12.

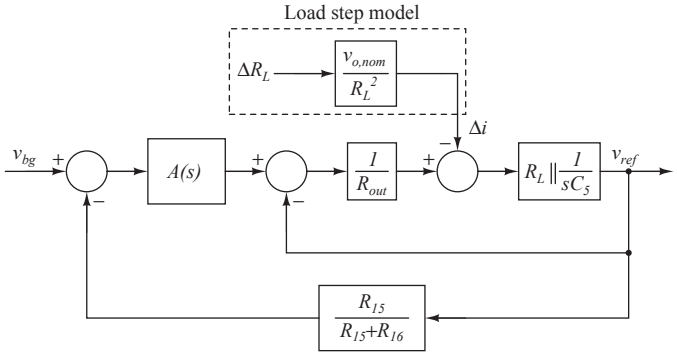

Fig. 10. Control-level model of the voltage regulator circuit, with load step modeled as a current perturbation. R_L is the output load. ΔR_L is placed instantaneously in series with R_L to create a step in the load. R_{out} is the output impedance of the operational amplifier.

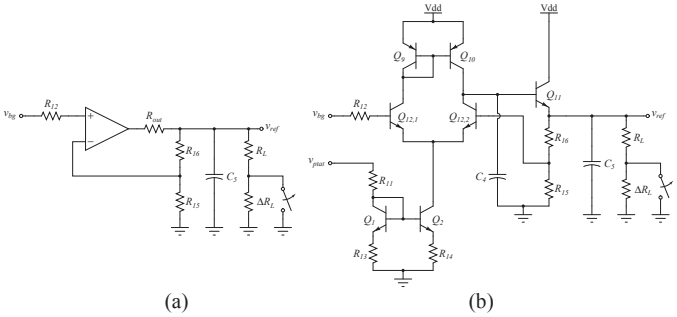

Fig. 11. (a) Behavioral-level model of the voltage regulator, and (b) its corresponding device-level model.

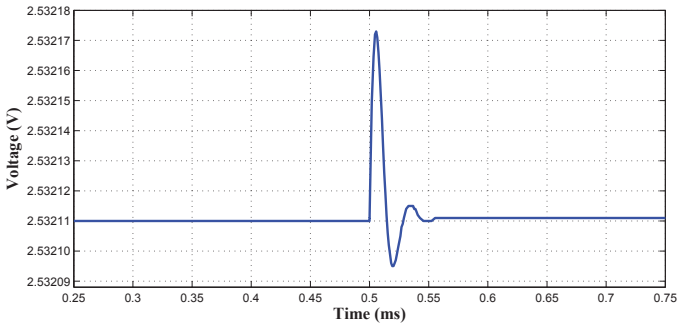

Fig. 12. Simulation of the voltage regulator response to a step in its load.

B. Bandgap Reference

Another interesting example is the bandgap reference circuit. As mentioned earlier, the bandgap circuit does not result directly from the control-level model, and can be used as a circuit block to convey this aspect to students. This circuit block suffers from a start-up issue, i.e. the circuit has a stable operating point at 0V. This aspect might be exposed at the device-level model, but definitely not at the behavioral-level model. In fact, this aspect portrays one of those less obvious issues encountered in circuit design, which may not even be detected from simulations. This stresses the fact that building the actual circuit after modeling it is an invaluable exercise.

Figure 13 [13] illustrates the concept behind the bandgap voltage, and can serve as a system-level model of the circuit block. It reflects the drift in the base-to-emitter voltage of a BJT with temperature, and how the thermal voltage V_t can be used to compensate for the drift. This leads to the generic implementation, i.e. the behavioral-level model, in Figure 14.

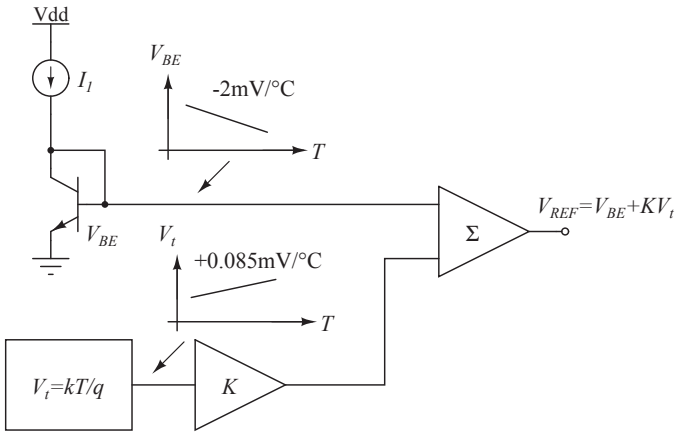

Fig. 13. Illustation of bandgap voltage creation [13].

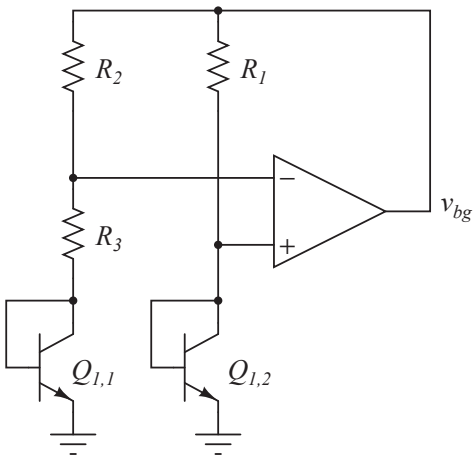

Fig. 14. Behavioral level model of the bandgap voltage circuit block.

It can be observed that there is no indication of any start-up issue with this model. The device-level circuit is shown in Figure 15. At this level, start-up circuitry can be incorporated to prevent the circuit from settling at the 0V trivial state. From this model, students should point out that the current through $Q_{1,1}$ is PTAT, and can thus utilize it, with the use of current mirrors, to create a PTAT voltage source to be used in other circuit blocks of the power controller. This is shown in the left half of Figure 15. An interesting teaching point here is performing a temperature sweep simulation, and observing the

variation of the bandgap and the PTAT voltages. The result is shown in Figure 16, which matches our expectations.

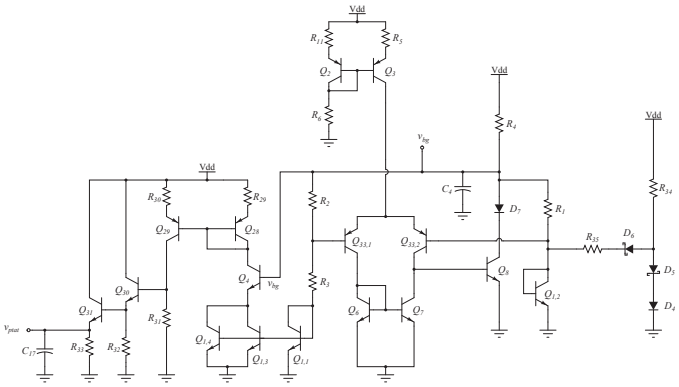

Fig. 15. Device-level bandgap voltage circuit block. Students can mirror the PTAT current through $Q_{1,1}$ to create a PTAT voltage source.

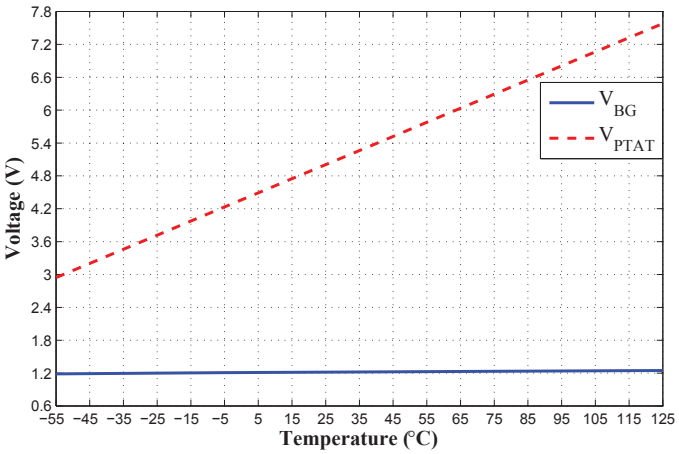

Fig. 16. Temperature sweep simulation showing the variation of PTAT and the bandgap voltages with temperature.

C. Clock

The third design example that illustrates the teaching benefits of the power controller kit is the clock circuit block. An important teaching objective here is to provide a hands-on experience on how variations in certain device parameters can severely impact the response characteristics. Robust design that is independent of the device nonidealities and variations in the manufacturing process is thus promoted and encouraged. The clock circuit also illustrates how the design process follows a spiral trajectory, whereby students iterate through the different model levels until the design objectives are met. It is an example of how simulation by itself does not guarantee identical operation in practice. However, when proper hand calculations are made, and when the design process is followed correctly, debugging becomes easier, and the number of iterations is low. Moreover, explaining the differences between simulation and experiment becomes much easier.

Figure 17 shows a behavioral-level model of the clock used in this kit. It consists of a single-input Schmitt trigger, which toggles at fixed high and low threshold voltages. When the Schmitt trigger output is low, the bottom current source I_{dis} is

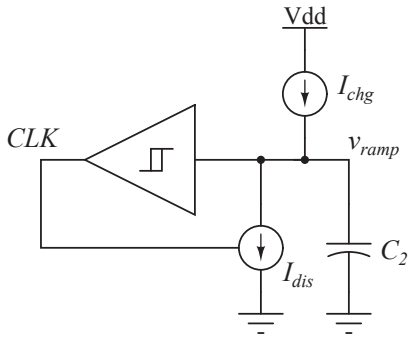

Fig. 17. Clock behavioral-level model. The clock pulse is the output of the Schmitt trigger, CLK. I_{chg} and I_{dis} control the pulse duration and the clock switching frequency.

off, and I_{chg} charges up C_2 at a rate equal to $m_r = I_{chg}/C_2$. When CLK is high, the bottom current source is on, and the capacitor voltage discharges at a rate $m_f = (I_{dis} - I_{chg})/C_2$, i.e. the slope of the voltage is $-m_f$. From this information, the times t_r and t_f taken for the capacitor voltage to rise from V_{th1} to V_{th2} or fall from V_{th2} to V_{th1}, respectively, can be calculated as follows:

$$t_r = \frac{V_{th2} - V_{th1}}{m_r} = \frac{C_2(V_{th2} - V_{th1})}{I_{chg}} \quad (1)$$

$$t_f = \frac{V_{th1} - V_{th2}}{-m_f} = \frac{C_2(V_{th1} - V_{th2})}{I_{chg} - I_{dis}} \quad (2)$$

Therefore, it can be seen that I_{chg} and I_{dis} are the design handles that set both the duration of the clock pulse as well as the clock frequency, f_{sw}, which is given by:

$$\frac{1}{f_{sw}} = \frac{C_2(V_{th2} - V_{th1})}{I_{chg}} + \frac{C_2(V_{th1} - V_{th2})}{I_{chg} - I_{dis}} \quad (3)$$

Figure 18 shows the device-level clock circuit. Notice how Q_1 and Q_2 perform the function of a single-input Schmitt trigger, with the resistors R_1 and R_2 configured in positive feedback to set the thresholds V_{th1} and V_{th2}.

Consider the case when, for example, the top current source in Figure 18 is configured to provide a current $I_{chg} \approx 95\mu$A, and the bottom current source is configured such that $I_{dis} \approx 620\mu$A. The simulation result of the clock circuit is shown in Figure 19, and the experimental result is shown in Figure 20. Notice how the clock frequencies are different; the simulation gives a 97.4kHz clock pulse, while the experiment results in a 60kHz clock pulse.

The reason behind the discrepancy between the simulation and the experiment lies in the actual device-level implementation of the Schmitt trigger. Specifically, the turn-off times of transistors Q_1 and Q_2 have a significant effect on the frequency of the clock. A small error in modeling this parameter in SPICE for both Q_1 and Q_2 can result in a large change in the rise time of the ramp signal, and in turn result in a large change in the clock frequency. This comes from the fact that the falling edge of the ramp has a much steeper slope than that of the rising edge. This is needed because the clock pulse occurs during the falling edge of the ramp; the narrower the clock pulse, the higher is the maximum converter duty ratio

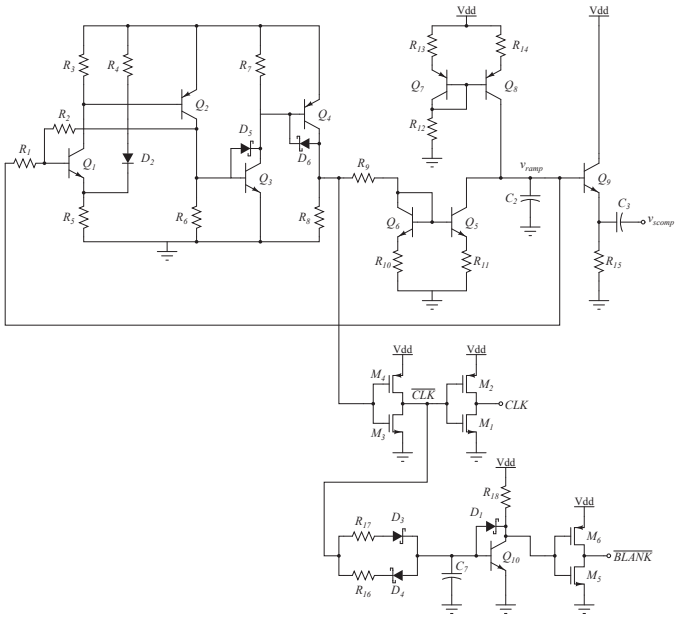

Fig. 18. Device-level model of the clock. This circuit block generates a clock pulse, a ramp, as well as a blank signal, all of which are needed in the complete controller implementation.

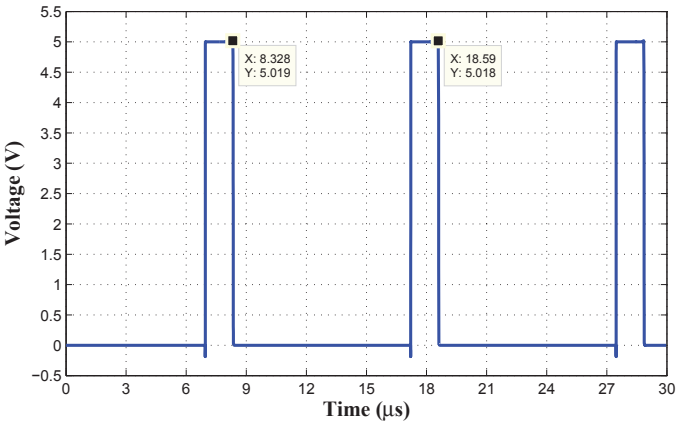

Fig. 19. Result from a SPICE simulation of the clock circuit. The clock period is about 10.3μs, which corresponds to a clock frequency of 97.4kHz.

the controller can sustain. Figure 21 illustrates the effect. It can be readily shown from the sketch that the errors in rise and fall times are related by the ratio of the slopes, as follows:

$$\Delta t_r = \left(\frac{m_f}{m_r}\right) \Delta t_f \tag{4}$$

Thus, the fact that we need $m_f \gg m_r$, i.e. $(m_f/m_r) \gg 1$, means that Δt_r is very sensitive to changes in Δt_f.

V. Conclusion

An educational power electronic controller kit was presented as an experimental platform for teaching modeling, control, and simulation in power electronics. A description of the kit's circuit blocks and their functionality was given. A methodology for proper system design that aims to eliminate poor engineering practices, such as running the whole controller through a time-domain device-level simulation, was

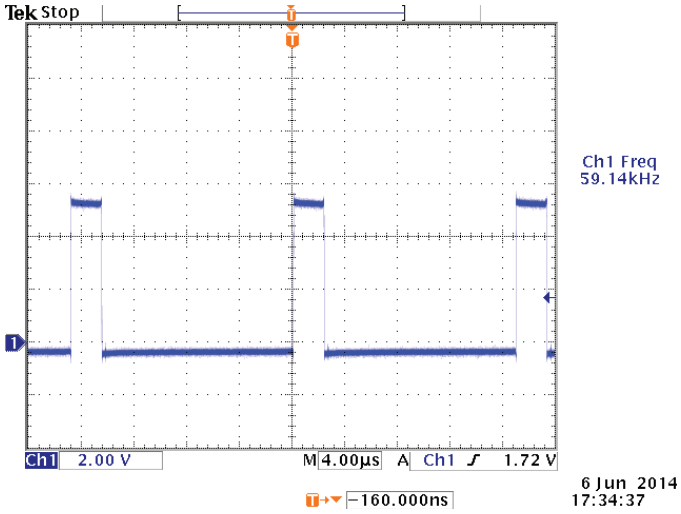

Fig. 20. Clock experimental result. The scope shows a clock frequency close to 60kHz, as opposed to the 97.4kHz observed in the simulation.

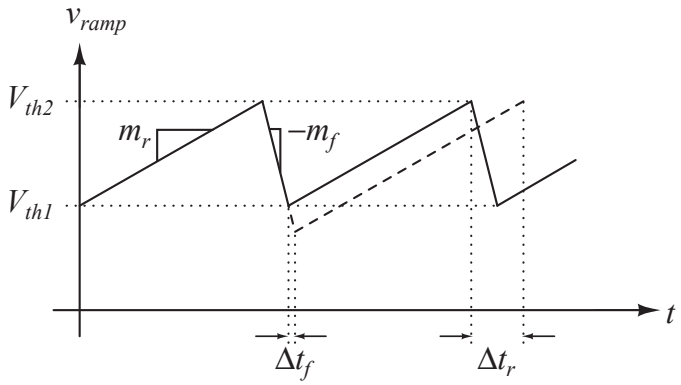

Fig. 21. Clock model error illustration. When $m_f \gg m_r$, a small change Δt_f in the ramp fall time causes a much larger effect on the ramp rise time Δt_r.

illustrated. Going through the different model levels not only results in a full rigorous understanding of each subsystem and circuit block of the power converter and controller, but also significantly reduces the chances of students facing problems when building each circuit block. The different model levels also prevent prolonged hours of extensive simulation iterations and tweaking of component values. Various teaching objectives were proposed and explained at the different model levels. Three design examples, taken directly from the kit's circuit blocks, were also presented, and a number of important aspects of system design were pointed out and elaborated on. This system design methodology is applicable not only in the field of circuit design and power electronics, but can also be extended to all fields of engineering involving system design.

Acknowledgment

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