Differential Diffusion Charge Redistribution for Photovoltaic Cell-Level Power Balancing

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Abstract— **Mismatch loss remains an important issue to address in PV systems, and many power electronic solutions have been proposed to recover these losses. However, conventional power electronics for solar power optimization often have to make tradeoffs among conversion efficiency, optimization granularity, and overall system cost. This paper presents a cell-level power balancing scheme that breaks the existing design paradigm. The proposed architecture simultaneously achieves maximum power point tracking without any external passive components at the cell-level, and maintains differential power processing with zero insertion loss. This is accomplished by leveraging the recently proposed diffusion charge redistribution technique, taking advantage of the readily available diffusion capacitance of solar cells to perform power balancing rather than relying on adding costly energy storage components. Furthermore, a dual current inverter interface is introduced to avoid processing common-mode generated power in order to minimize overall conversion loss. Significant boost in overall system efficiency is achieved under both matched and partial shading conditions. Simulation results are included to demonstrate the feasibility and benefit of this approach.**

Keywords-switched capacitor networks, distributed power converters, maximum power point tracking, differential power processing, PV energy optimization.

I. INTRODUCTION

Adoption of solar photovoltaic (PV) energy has been growing rapidly due to declining manufacturing costs and improving solar cell efficiency. However, in order for PV energy to reach grid-parity, inefficiencies in the existing power electronics architecture must be addressed to further improve energy capture and reduce cost.

It is well known that the conventional series-connections of photovoltaic (PV) power modules result in the weakest-link problem and cause disproportionate energy loss [11,13]. A few underperforming cells can cause significant loss in energy capture in a large string because series-connected cells must carry the same current, and are therefore constrained by the lowest-performing cell. Mismatches caused by partial shading, dirt accumulation, manufacturing tolerances, and different aging characteristics can severely limit the overall power extraction from a string and the negatively impact the long-term project economics [2-13].

Parallel bypass diodes at the sub-string level can lessen the problem by bypassing the underperforming sub-strings altogether. Nevertheless, while this approach may potentially extract more power overall, it is suboptimal because any available power from the underperforming sub-string is completely forfeited. In addition, the resulting output power characteristic curve is non-convex, which further complicates the maximum power point tracking (MPPT) algorithm [3,5].

A number of module-level power electronic (MLPE) architectures, such as cascaded dc-dc converters and micro-inverters, and their sub-module counterparts have been proposed to perform distributed maximum power point tracking [8-10]. The main disadvantage of cascaded architectures is the necessity to process the full power from each PV element, resulting in high insertion loss. The differential power processing schemes address the insertion loss problem by placing converters in parallel to only process the mismatch power [3-7]. However, all these approaches are subject to the high costs of intermediate energy storage components, such as discrete inductors and capacitors. Hence, their applications have been limited to the module and sub-module string levels, and cannot solve mismatch problems at the cell level.

Recent work has shown that the intrinsic diffusion capacitance of the solar cells can be used to performing power balancing effectively [1]. By using the diffusion charge redistribution (DCR) technique with a scalable ladder structure of solar cells, maximum power point tracking can scale down to the finest cell-level granularity. This approach balances the tradeoff between differential power processing and the cost of external passive components. In particular, by opting to process roughly half of the common-mode generated power, the requirement of intermediate energy storage can be completely eliminated.

This paper builds on the existing concept of diffusion charge redistribution and rethinks the string-level power electronics architecture to enable complete differential power processing for maximum power point tracking at the cell-level without the use of per-cell energy storage components. The background and shortcomings for the previously proposed diffusion charge redistribution technique will be discussed in Section II. The string-level power electronics enhancement, in
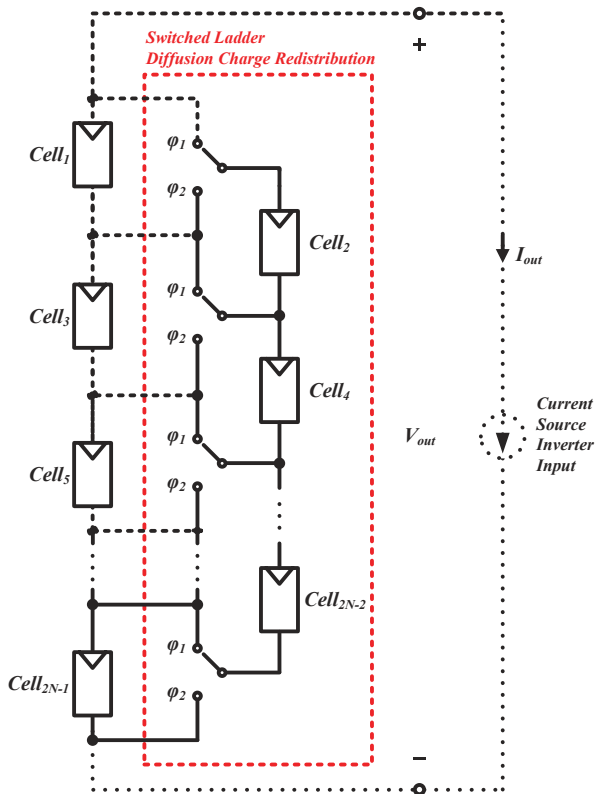
Figure 1.   Previously proposed ladder-connected DCR architecture [1].

particular a dual current inverter setup, will be presented and analyzed in Section III. Additional benefits in system reliability and control simplification, along with simulation results, will also be discussed.

II.   SINGLE-OUTPUT SWITCHED-LADDER DCR

A fully scalable, cell-level power balancing architecture using DCR was first proposed in [1] and illustrated in Fig. 1. It leverages the intrinsic capacitance of the solar cells to act as intermediate energy storage instead of adding discrete capacitors or inductors. The topology consists of a conventional string of N cells connected to the output load and a switched-ladder string of $N − 1$ cells in parallel. This hybrid approach simultaneously enables constructing long series strings to create a sufficiently high voltage for interfacing with grid-tie inverters, and making the cells appear in pseudo-parallel to eliminate the weakest-link problem in real-world operating conditions. Forcing the cells to have approximately equal voltages via the switching ladder structure, the entire switched string behaves as an effective "super-cell".

In this single-output DCR topology, power is extracted at the output of the conventional string, or the load-connected string shown on the left in Fig. 1. Therefore, the power produced from the switched-ladder string must be processed through the switching structure, regardless of the amount of mismatch present in the system. This constitutes an insertion loss, which is the additional conversion loss compared to a series string under perfectly matched condition. The insertion loss, though shown to be manageable, sets design constraints

on the switch sizing and especially the switching frequency based on the available intrinsic solar cell capacitance [1].

Conventional switched-capacitor converters have been well-studied, and their losses can be classified into two asymptotic limits: the slow-switching limit (SSL) and fast-switching limit (FSL) losses [12]. The existing analysis has been generalized to characterize the proposed multiple-input single-output distributed power generation system [1] to derive the respective FSL and SSL loss components for the ladder-connected DCR topology.

In particular, the FSL and SSL components of the percentage insertion loss can be derived [1] as shown in (1) and (2),

$$IL_{FSL} = \frac{4}{2N-1} \cdot \frac{N-1}{N} \cdot \frac{I_{mp}}{V_{mp}} \cdot R_{eff} \qquad (1)$$

$$IL_{SSL} = \frac{1}{12} \cdot \frac{N-1}{N} \cdot \frac{1}{f_{sw}} \cdot \frac{1}{V_{mp}} \cdot \frac{I_{mp}}{C_d} 0 \qquad (2)$$

where R_{eff} is the effective resistance of the switch on-resistance in series with any parasitic interconnect resistance, f_{sw} is the switching frequency, V_{mp} and I_{mp} are the maximum power voltage and current of the solar cells respectively, and C_d is the available diffusion capacitance of a single cell. From (1), it can be seen that the main design variables that determine the FSL insertion loss are the effective resistance and the length of the string. In fact, the FSL insertion loss can almost always be made negligible for a sufficiently long string. From (2), the SSL insertion loss is largely dictated by the fundamental material properties of the solar cells, such as the maximum power voltage, the maximum power current, and the diffusion capacitance. For a sufficiently large N, the only degree of freedom in this design space is the switching frequency.

The following example from [1] will be used to illustrate the estimated achievable insertion loss figures. Given solar cells with a maximum power voltage of 0.5 V, a maximum power current of 2 A, and an available diffusion capacitance of 9 μF, configured in a DCR string with N of 20 using MOSFET switches with an effective resistance of 15 mΩ, the FSL insertion loss can be shown to be negligible at 0.58%. However, in order to achieve a reasonable SSL insertion loss, a fast switching frequency must be used. At a switching frequency of 1 MHz, the SSL insertion loss is calculated to be 3.5%. While these losses are manageable, having insertion loss on the common-mode generated power may not be attractive for panel manufacturers and system integrators when long-term project economics are factored in. Therefore, in the next section, methods for enabling differential processing will be discussed and presented.

III.   DIFFERENTIAL DIFFUSION CHARGE REDISTRIBUTION

One key concept for improving the photovoltaic energy conversion efficiency is the idea of differential power processing (DPP). By only processing the generally small mismatch in power among PV elements, the incurred power conversion loss from performing maximum power point tracking (MPPT) can be reduced significantly. Specifically,
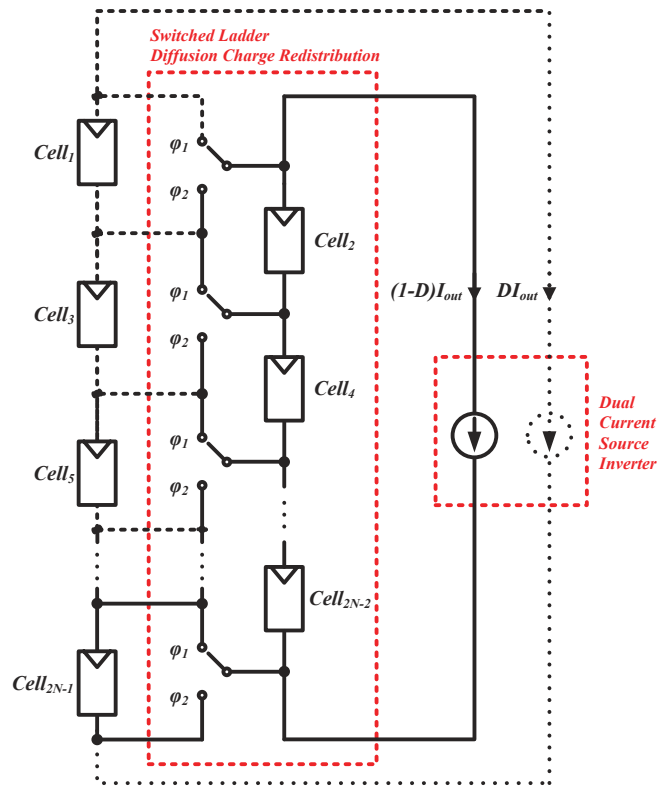
Figure 2. Conceptual diagram of the proposed differential DCR (dDCR) architecture with dual current source inverter output.
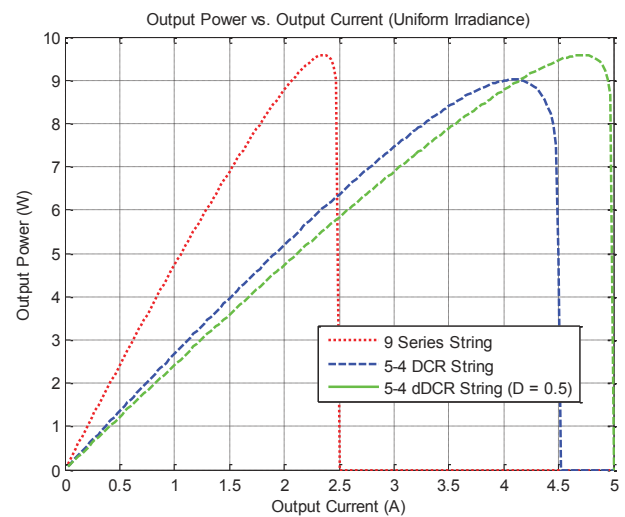

Figure 3. SPICE simulation comparing the output power versus total output current under uniform irradiance among three topologies: 9 series string, 5-4 DCR, and 5-4 dDCR architectures.

when the PV elements are operating under matched conditions, their energy production should be extracted directly by the output load, such as a grid-tie inverter, without any intermediate processing.

Differential power processing have been implemented at different levels of integration using a variety of architectures and topologies [3-7]. However, these approaches typically consist of a single modular functional block capable of achieving DPP and MPPT simultaneously, hence requiring these blocks with either parallel current steering inductors or voltage balancing capacitors at the desired level of MPPT granularity.

The recently proposed DCR technique has been shown to effectively perform cell-level power balancing without needing local intermediate energy storage components on a per-cell basis. In order to enable DPP for DCR while retaining its main advantage of requiring no per-cell energy storage components, this paper proposes a DPP-enabling circuit enhancement that is deliberately decoupled from the MPPT functional blocks. Instead, the proposed architecture is applied to the string-level power electronics. In particular, the string-level modification should allow direct energy extraction from both the load-connected and the switched-ladder strings.

The conceptual diagram of differential DCR (dDCR) architecture is illustrated in Fig. 2. The dual current source input interface can be implemented using two isolated string inverters, or via a current divider interface preceding a central inverter. In this topology, cell-level power balancing and maximum power point tracking are achieved by charge

redistribution on the solar cells' diffusion capacitance. The dual current source interface provides means for direct energy extraction from both the load-connected and the switched-ladder strings, thereby enabling differential power processing.

A. Differential Power Processing

When all the cells operate under perfectly matching condition, they must have the same maximum power voltage V_{mp} and maximum power current I_{mp}. To extract the maximum power from the strings, the dual current sources must extract I_{mp} from each and every cell, which can be accomplished by each demanding I_{mp} from their respective string. This corresponds to an even current divide ratio of $D = 0.5$. Under this condition, the solar cells would each exhibit the maximum power voltage V_{mp} so that no charge transfer will occur during the switching events of the ladder. Hence, there is no power processing and no insertion loss associated with adopting diffusion charge redistribution compared to a series string.

It can also be observed that when the maximum power current is being extracted from the switched-ladder string of solar cells, their active elements are effectively nulled from the perspective of the load-connected string of cells. Therefore, the ladder-connected cells appear as a passive string of capacitors to the load-connected string of cells. By symmetry, the same observation can be made of the load-connected cells from the perspective of the ladder-connected cells. Under matched condition, this means that no power from the ladder-connected string is processed by the load-connected string, and vice versa.

To validate the differential power processing capability in the proposed topology, a SPICE simulation is performed comparing the following three configurations: a 9-series string, a 5-4 DCR string, and a 5-4 dDCR string. In this simulation, the cells are assumed to be matched with uniform irradiance, and each generate a short-circuit current of $I_{SC} = 2.5$ A. In addition, an even current divide ratio of $D = 0.5$ is used in the dDCR string as discussed previously.

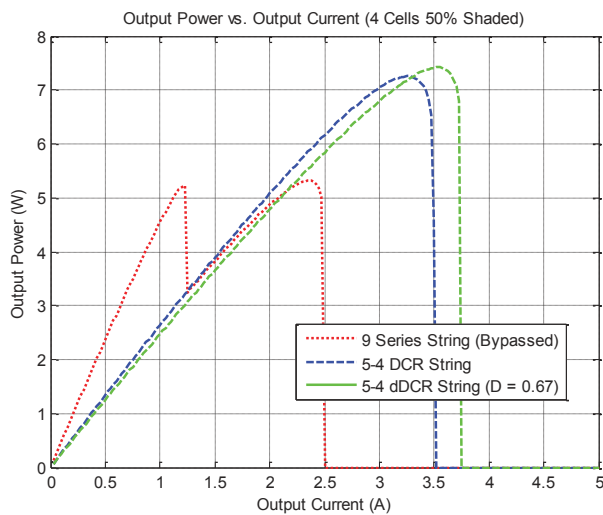Output Power vs. Output Current (4 Cells 50% Shaded)

Figure 4.   SPICE simulation comparing the output power versus total output current with four cells shaded among three topologies: 9-series string with per-cell bypass diodes, 5-4 DCR, and 5-4 dDCR architectures. In the DCR and dDCR configurations, the four shaded cells are chosen to be the ladder-connected cells.

Fig. 3 compares the output power of the three different configurations. The x-axis on the plot corresponds the total current extracted, which is the sum of the load-connected and ladder-connected string currents in the case of the dDCR string. In contrast to the single-output DCR string, the dDCR string exhibits no insertion loss and extracts the same peak power as the series string. This result verifies the differential power processing capability of the proposed architecture.

B.   *Current Divide Ratio Tuning*

For minimum insertion loss under perfectly matching conditions, the dual current sources should demand equal currents, in particular the maximum power current, from their respective strings. However, given asymmetric shading conditions, the current divide ratio of the two output sources can be used as an extra degree of freedom to minimize the amount of processed power. This is illustrated in Fig. 2 by the current divide ratio D, where the current commanded by an inverter is split into $D \cdot I_{out}$ through the load-connected string and $(1-D) \cdot I_{out}$ through the switched-ladder string. This provides additional means for optimization that was not available in the original single-output DCR configuration.

Consider the following example to demonstrate the utility of this added tuning capability: assume a dDCR system with all of the ladder-connected cells shaded by 50%. Because solar cells are current generation devices, it is clear that in order to maximize the extracted power from each cell while minimizing the amount of processed power, the commanded current from the load-connected string should roughly be twice that from the ladder-connected string. In other words, with a current divide ratio of $D = 0.67$, the amount of processed power is close to zero, whereas in the case of the single-output DCR with $D = 1$, approximately a quarter of the generated power has to be processed. Hence, the dDCR topology with the added tuning

ability is expected to extract a higher peak power compared to the original DCR configuration.

A SPICE simulation comparing a 9-series string with per-cell bypass diodes, a 5-4 DCR string, and a 5-4 dDCR string is again used to illustrate the utility of the current divide ratio tuning. In this simulation, four cells are affected by partial shading, and partial shading conditions are simulated by decreasing the short-circuit current by 50% in the affected cells. In the 5-4 DCR and dDCR architectures, the four shaded cells are chosen to be the ladder-connected cells according to the discussed example. Fig. 4 illustrates the extractable power under this partial shading condition. It can be observed that the DCR and dDCR configurations are able to deliver significantly more power under mismatch by performing power balancing at the cell-level. In addition, the benefit of having the current divide ratio tuning capability is demonstrated. By setting the current divide ratio to minimize the amount of processed power, more usable power can be extracted from the system.

In the general case with arbitrary shading patterns, finding the optimal current divide ratio may not be as simple as described in the previous example. The output power optimization must be performed over the entire space spanned by the following two variables: the total output current I_{out} and the current divide ratio D. The convexity of such a multivariable optimization problem will be examined in the following section.

C.   *Power Optimization Convexity*

It was demonstrated in [1] that the output power versus output current characteristic for the original DCR configuration is a convex upwards function, i.e., there is no more than one maximum, regardless of partial shading conditions. This is perhaps one of the most appealing benefits of adopting the DCR configuration. Without the possibility of being stuck at a local maximum power point, the string-level maximum power optimization algorithm can be greatly simplified.

The intuition behind the output power convexity with respect to output current of the single-output DCR topology can be derived from the switching configuration. The ladder switching topology effectively transforms the series string connections of the solar cells into pseudo-parallel ones. Parallel combination of solar cells is essentially equivalent to constructing a single large solar cell, and the pseudo-parallel combination of solar cells then creates a single "super-cell" with rescaled voltage and current characteristics. Regardless of scaling, if a string behaves as and exhibits characteristics of a single cell, then the output power versus output current curve must be convex.

In the case of the two-variable optimization problem, the same intuitive argument does not apply directly as the optimization now is trying not only to maximize the power extraction from the solar cells, but also to minimize the amount of power processed by diffusion charge redistribution. The rigorous mathematical model of extracted power with loss models incorporated is left to future work. In this paper, simulation over key corner cases of partial shading conditions as well as randomly generated shading patterns are presented.
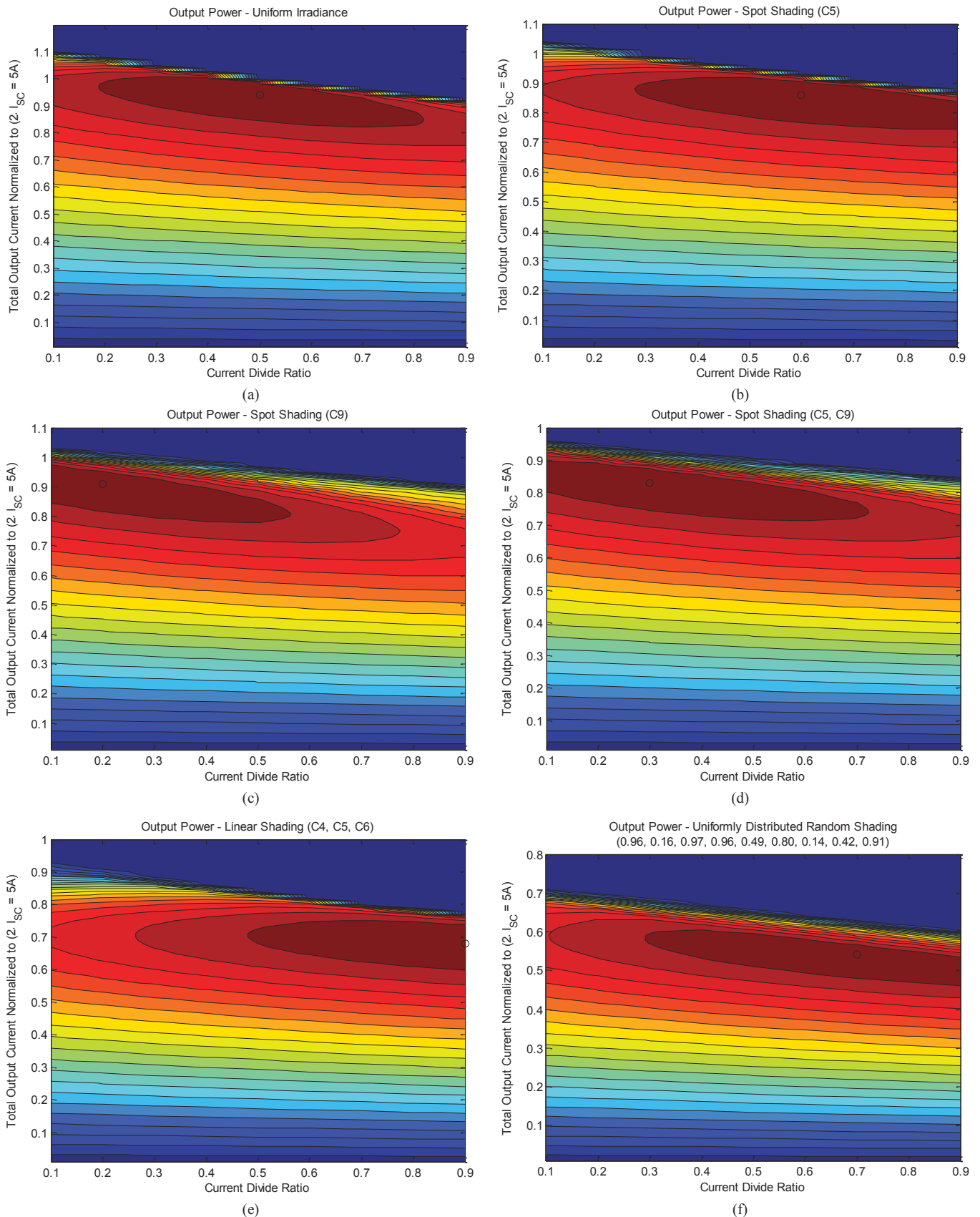
Figure 5. SPICE simulated output contours over total output current and current divide ratio. (a) uniform irradiance, (b) center spot shading, (c) termination spot shading, (d) combination spot shading, (e) horizontal linear shading, and (f) uniformly distributed random shading. In the specified shading cases, the affected cells are shaded by reducing their short-circuit current by 50%. In the randomly generated shading case, scaling of their I_{SC} are as specified.

Fig. 5 illustrates the simulated output power contours over the space spanned by the total output current I_{out} and the current divide ratio D under various shading conditions. In these SPICE simulations, a 5-4 dDCR string is configured with load-connected cells numbered with odd indices and ladder-connected cells numbered with even indices, ascending from top to bottom as shown in Fig. 2.

The output power contour when the system is operating in uniform irradiance condition is shown in Fig. 5a, and a current divide ratio of $D = 0.5$ is indeed where the peak power extraction occurs. Cases where the system experiences a symmetric center spot shading, an asymmetric termination spot shading, as well as a combination of these spots are illustrated in Fig. 5b, 5c, and 5d respectively. Finally, results for horizontal linear shading and randomly generated shading conditions are shown in Fig. 5e and 5f. Even though many more shading conditions are simulated by the author, these representative cases are chosen to demonstrate the general behavior of the power contours. In all simulated cases, the output power contour has always remained convex with only a single maximum power point over the entire space.

Since the output power contour is observed to be generally convex over a wide range of shading conditions, there is little to no risk of the optimization being stuck in a local maximum power point. Hence, the MPPT algorithm complexity for this multivariable optimization problem at the string level can be reduced, and well-known methods such as gradient descent or conjugate gradient methods can be adopted.

D. Local Control and Frequency Scaling

In traditional DPP topologies, where a single functional block capable of simultaneously achieving DPP and MPPT is employed and distributed at the desired level of optimization granularity, local MPPT control must control the duty ratio of individual converters such that each PV elements operates at its local maximum power point [5,6]. Although any of the existing and established MPPT algorithms can be adopted [14], having local control requires additional measurement and sensing hardware for each PV element.

In contrast, power balancing and optimization is inherent in the DCR switching topology such that charge redistribution occurs naturally. In this case, only switch synchronization hardware is required among adjacent converters. There is no need for full-fledged MPPT converters nor localized control to optimize the power for each PV element.

It was shown in [1] that in order to achieve low overall insertion loss, a switching frequency in the range of hundreds of kilohertz was required given the available diffusion capacitance to maximum power current ratio. This constraint arises from the fact that the original DCR configuration must process the generated power from roughly half of the solar cells at all times. In the case of dDCR, the amount of processed power can be reduced significantly. Therefore, it is possible to decrease the switching frequency while maintaining a certain level of overall conversion efficiency.

For example, given a solar array installation and its expected amount of mismatch, a slower switching frequency
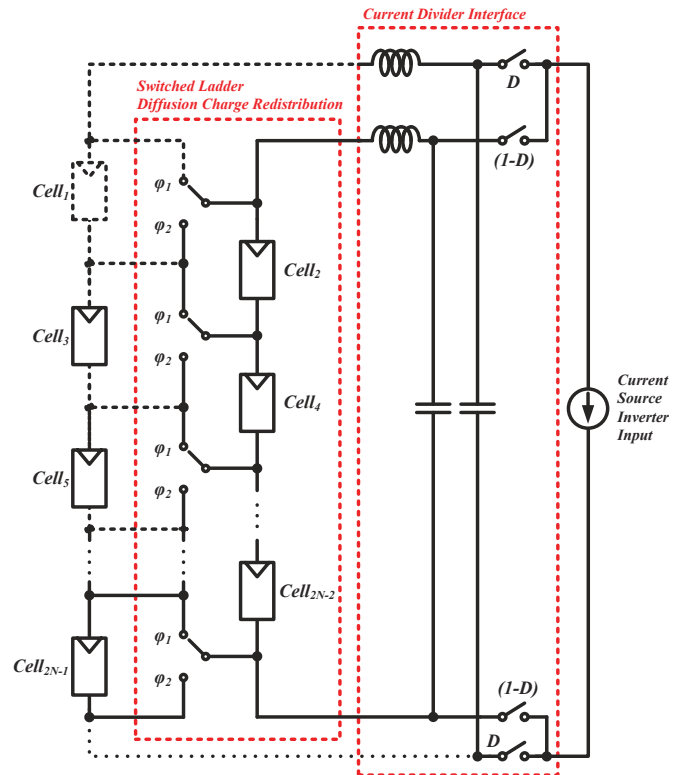

Figure 6. An example implementation of the output current divider interface preceding a centralized inverter.

can be determined and fixed at installation time to meet the desirable efficiency target of the project developer. A more advanced implementation may even enable adaptive frequency scaling during real-time operation.

E. Circuit Implementation

The dual current interface can be implemented with two isolated string inverters as mentioned in the previous section. In this configuration, the two inverters can perform MPPT individually as the entire optimization space is shown to be generally convex. Moreover, redundancy and fault tolerance can be gained as added benefits. If one of the inverters fails, it does not necessarily result in total system failure and shutdown. The remaining inverter can continue to operate the system as a single-output DCR system with increased insertion loss, given that appropriate power rating headroom is factored into the system design.

In systems where centralized inverters are used, a current divider interface preceding the inverter can be used. An example implementation of a current divider is shown in Fig. 6. In order for this topology to be adopted in practice, the conversion loss from current dividing must be lower than the insertion loss the single-output DCR topology would otherwise incur. In this illustration, two inductors are inserted to enable adiabatic charging and discharging of the capacitive energy buffers. In other words, the capacitors are charged by near-constant current sources from the inductors and discharged by a constant current from the inverter. Hence, the capacitive

charging and discharging losses can be drastically lowered, and it is possible to design this current divider to be extremely energy efficient.

IV. CONCLUSION AND FUTURE WORK

This paper presents a cell-level power balancing scheme that builds on the concepts of diffusion charge redistribution and differential power processing. The proposed topology separates the DPP enabling circuitry from the MPPT functional blocks to not only performs maximum power point tracking with cell-level granularity without using any external passive components, but also achieves zero insertion loss with minimal added hardware at the string or centralized inverter level.

The functionality and benefits of the proposed architecture are illustrated and validated in SPICE simulations. The added current divide ratio tuning capability has shown to be useful in minimizing the amount of processed power. Furthermore, the optimization over the space spanned by the output current and the current divide ratio is shown to be generally convex over a variety of partial shading conditions. Additional advantages include reduced switching loss from lower or dynamically scaled frequency of DCR, as well as higher reliability from inverter redundancy.

The dual current source inverter interface can also be extended to other existing maximum power point tracking topologies to enable differential power processing. For example, in PV installations with cascaded dc-dc converters, string connections may be added to the output of the PV modules in addition to the string connections at the output of the dc-dc converters. Together with the dual current source inverter interface, this enables both direct power extraction from the PV string and processed power extraction from the output of the cascaded dc-dc converters, and thereby achieves differential power processing with minimal extra hardware.

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