Constant Power Load Modeling for a Programmable Impedance Control Strategy

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***Abstract*—Expanded use of power electronics opens the possibility that input characteristics presented to the conventional utility as well as ac and dc microgrids could be controlled in ways that help support utility operation. Power factor correcting interfaces are one wide-spread example, used around the world to meet regulatory requirements for both power factor and also harmonic content injected to the utility. More support for ensuring healthy utility operation might be demanded from these power electronic interfaces. For example, the potentially destabilizing effects of constant power loads (CPLs) could be remediated on time scales useful for supporting utility operation. This article presents an equivalent circuit model for limited-bandwidth CPLs that quantifies the intrinsic damping properties of regulated converters. A control architecture based on this equivalent circuit model is then analyzed. The control scheme limits the impact of CPL operation by emulating the internal damping of CPLs through programmable input behavior. An intermediate, internal energy buffer is used to support CPL operation while enabling the programmable or selectable input impedance on designed time scales. The effectiveness of this strategy on system stability is shown using a stability analysis and experimental results.**

***Index Terms*—Active filters, energy storage, negative resistance devices, programmable filters, stability.**

I. Introduction

ELECTRONIC loads generally consume energy according to load requirements rather than utility capabilities. The input impedance presented by a load to the grid, dc or ac, will, therefore, vary with the type of load. For instance, constant power loads (CPLs) present a negative incremental input resistance. This characteristic of CPLs can cause instability in dc [1]–[4] and ac [5] systems. By commanding increased current when dc-link voltage decreases, CPLs favor load needs over utility capabilities.

A potential additional benefit of loads with power electronics is that they can be designed to tightly and flexibly control their input behavior. This article introduces a control architecture that can provide a flexible input impedance to the utility while simultaneously meeting load power demands by flexibly drawing power from an internal energy buffer. The buffer also provides an uninterruptible power supply on short time scales, and can be flexibly sized to trade cost for capability in supporting the utility. The approach introduced in this article opens the door to loads that not only satisfy customer demands but that also support utility operation.

For systems loaded by CPLs, stability criteria have been developed. These criteria typically rely on small-signal models that assume that CPLs are ideal negative resistors [6], [7]. This modeling approach is valid within the control bandwidth, but does not account for damping effects beyond this frequency. As will be shown in this article, this can lead to overly restrictive stability criteria. A more realistic limited-bandwidth model presented in this article provides more lenient stability criteria by revealing intrinsic damping properties of regulated converters, and forms a basis on how to use programmable input behavior as a stability method. Fig. 1 shows how the limited-bandwidth CPL model presented in this article expands on the ideal CPL model by adding a virtual damping component to include the intrinsic behavior stemming from limited control bandwidth.

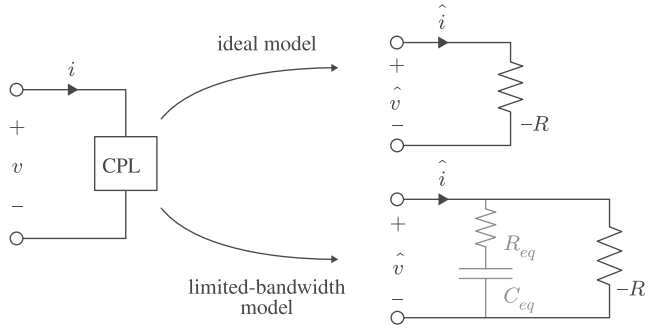

Fig. 1. In small-signal analysis, an ideal CPL can be represented as a negative resistor. A more expansive model that accounts for limited control bandwidth is shown that resembles the ideal model but includes an equivalent virtual damping component.

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Several methods have been developed for stabilizing systems with CPLs. Passive damping can stabilize dc-link voltage [8]–[10], but can require the addition of large filter elements that can be impractical in many applications. Active damping methods have also been developed [11], [12]. They often include nonlinear elements that increase complexity, or compromise load performance due to increased power ripple during input disturbances. Other stabilization methods have been proposed specifically for use in cascaded converter configurations rather than for point-of-load CPL converters [13]–[15]. Control oriented active stabilization techniques have also been developed [16]–[19], but also exhibit nonlinear complexities or increased power ripple. Another approach is presented in [20], which focuses on presenting a resistive input impedance, but creates high power ripple. Similar to the approach used in this article, virtual impedance methods have been proposed [21]–[24]. However, in this article, the virtual impedance is linear and introduces only limited power ripple by resembling a limited-bandwidth CPL. The approach presented in this article permits direct shaping of the input impedance while minimizing power ripple and supporting load operation.

Active stabilization methods that preserve load regulation have also been developed. In [25] and [26], a source converter rejects input voltage oscillations by incorporating high-pass filtering of the input voltage in its control. In other examples, stabilization of a CPL loaded dc microgrid is achieved by employing cost function based control [27], and by incorporating a source-side virtual series resistance [28]. In [29], active stabilization takes the form of a front end that presents a controlled resistance to the source and is controlled by managing the relationship between stored energy and input impedance. The goal of these approaches is to stabilize CPL loaded systems without adding large passive components, and without compromising load regulation. This article presents a new method to accomplish this that uses an equivalent circuit model approach that is based on the natural behavior of CPLs operating at reduced bandwidth. This natural behavior reveals an intrinsic damping component that can improve dc-link stability without the need for large passive damping components. In a structure similar to that of power-factor correction preconverters, the control strategy proposed in this article separates input and output behavior. However, the intent is not on wave shaping, and rather, the converter input stage is designed to present any impedance to the utility. In this case, the input stage is designed to resemble the natural behavior of a limited-bandwidth CPL for its virtual damping properties.

This article first presents an equivalent circuit model for limited-bandwidth CPLs that quantifies inherent damping properties of regulated converters. The following section then analyzes a converter and control strategy based on this equivalent circuit model. The scheme maintains load regulation while a programmable input impedance allows the converter to emulate a limited-bandwidth CPL. For the constant power application presented here, an intermediate energy buffer prevents input power ripple from affecting load power. Results from experimental testing are then presented. They demonstrate how the programmable input can stabilize a dc system by presenting a decreased CPL bandwidth, thereby increasing the intrinsic damping. It is shown that with an energy buffer implemented, load power remains regulated at high bandwidth.

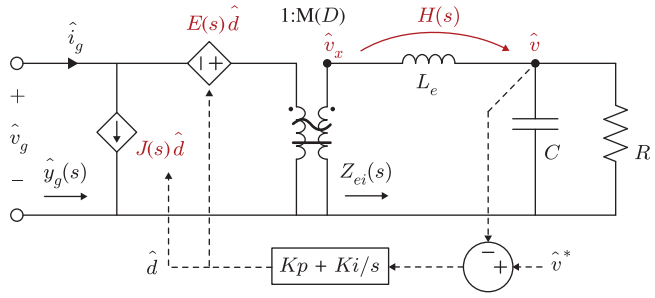

Fig. 2. Canonical circuit model for common converters operating in CCM with regulated output voltage (adapted from [32, p. 253]).

TABLE I
CCM CANONICAL MODEL PARAMETERS (AS IN [32, P. 253])

Converter	$M(D)$	L_e	$E(s)$	$J(s)$
Buck	D	L	$\frac{V}{D^2}$	$\frac{V}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V\left(1-\frac{sL}{D'^2R}\right)$	$\frac{V}{D'^2R}$
Buck-boost	$\frac{-D}{D'}$	$\frac{L}{D'^2}$	$\frac{-V}{D^2}\left(1-\frac{sDL}{D'^2R}\right)$	$\frac{-V}{D'^2R}$

II. LIMITED-BANDWIDTH CPL MODEL

A realistic CPL model accounts for limited control bandwidth. The well-known Middlebrook [8] introduced the valuable modeling step of including the full effects of feedback control in CPL behavior when designing a passive input filter. Other analyses favor a simpler modeling approach to ease analytical requirements at the expense of accuracy. This section develops a simple yet detailed equivalent circuit model for the input impedance characteristics of CPLs based on dc state and controller bandwidth. The model is useful for stability analyses and for understanding the value and deployment of the proposed input impedance controller developed in the following sections.

Common converters (buck, boost, and buck–boost) operating in CCM can be modeled using a canonical circuit model [30], [31] that is summarized in [32, p. 253]. A small-signal adaptation of this model is shown in Fig. 2. "Hatted" variables represent small-signal quantities. A PI controller for maintaining regulated output voltage, with proportional and integral gains K_p and K_i, is included in the model as an example. Of course, other compensators could be included without changing the spirit of the modeling effort in this section. The output filter loaded by R is represented by the transfer function $H(s) = \hat{v}/\hat{v}_x$. The dependent sources, transformer $M(D)$, and equivalent inductor L_e vary depending on the converter type as listed in Table I, where V and D are the operating point output voltage and duty cycle, respectively.

This canonical model serves as a starting point for deriving a simplified equivalent circuit model that summarizes the small-signal input admittance $\hat{y}_g(s)$. This model development begins by noting the governing equations for the output voltage, duty

TABLE II
CPL ADMITTANCE CHARACTERISTICS VALUES

Converter	Y_{LF}	Y_{MF}	ω_{CPL}
Buck	$\frac{-D^2}{R}$	$\frac{D^2}{R}\left(\frac{D-K_pV}{D+K_pV}\right)$	$\frac{K_iV}{D+K_pV}$
Boost	$\frac{-1}{D'^2R}$	$\frac{1}{D'^2R}\left(\frac{D'-K_pV}{D'+K_pV}\right)$	$\frac{K_iV}{D'+K_pV}$
Buck-boost	$\frac{-D^2}{D'^2R}$	$\frac{D^2}{D'^2R}\left(\frac{DD'-K_p(-V)}{DD'+K_p(-V)}\right)$	$\frac{K_i(-V)}{DD'+K_p(-V)}$

cycle, and input current

$$\begin{cases} \hat{v}_x = M\left(\hat{v}_g + E\,\hat{d}\right) \\ \hat{v} \;\; = H\hat{v}_x \\ \hat{d} \;\; = \left(K_p + \frac{Ki}{s}\right)(\hat{v}^* - \hat{v}) \\ \hat{i}_g = J\,\hat{d} + \frac{M^2}{Z_{ei}}\left(\hat{v}_g + E\,\hat{d}\right) \end{cases} \tag{1}$$

and then solving the system for $\frac{\hat{i}_g}{\hat{v}_g}$, which gives

$$\hat{y}_g(s) = \frac{\hat{i}_g(s)}{\hat{v}_g(s)} = \frac{M^2 s - JMRK_p s - JMRK_i}{R(s + EMK_p s + EMK_i)}. \tag{2}$$

This expression can be simplified by considering the low-frequency approximations of the transfer function $H(s)$ and impedance $Z_{ei}(s)$, which are given by

$$\begin{aligned} \lim_{s\to 0} H(s) &= 1 \\ \lim_{s\to 0} Z_{ei}(s) &= R \end{aligned} \tag{3}$$

as well as the low-frequency approximations of dependent sources $E(s)\hat{d}$ and $J(s)\hat{d}$, which vary depending on converter type according to Table I. After substituting these approximations into (2), the expression can be rearranged to clearly express input admittance in terms of low-frequency gain Y_{LF}, mid-frequency gain Y_{MF}, and bandwidth ω_{CPL}. In doing so, the input admittance takes the form

$$\hat{y}_g(s) = Y_{\text{MF}}\frac{s + \omega_{\text{CPL}}\frac{Y_{\text{LF}}}{Y_{\text{MF}}}}{s + \omega_{\text{CPL}}} \tag{4}$$

where

$$Y_{\text{LF}} = \frac{-J}{E} \tag{5}$$

$$Y_{\text{MF}} = \frac{1}{R}\left(\frac{M^2 - JMRK_p}{1 + EMK_p}\right) \tag{6}$$

$$\omega_{\text{CPL}} = \frac{EMK_i}{1 + EMK_p}. \tag{7}$$

To express these characteristics for specific converters, parameters from Table I can, then, be substituted into (5)–(7) to express the admittance characteristics for each type of converter. These values are shown in Table II.

The admittance characteristics describe converter behavior at frequencies below and above the control bandwidth ω_{CPL}, which is dependent on K_i and K_p. At frequencies below ω_{CPL}, the admittance is Y_{LF}. Note that Y_{LF} is negative and equal to the load

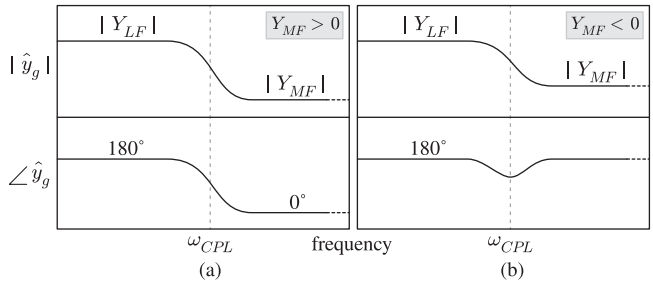

Fig. 3. Bode plot of small-signal input admittance of limited-bandwidth CPL with bandwidth ω_{CPL}. (a) $Y_{\text{MF}} > 0$. (b) $Y_{\text{MF}} < 0$.

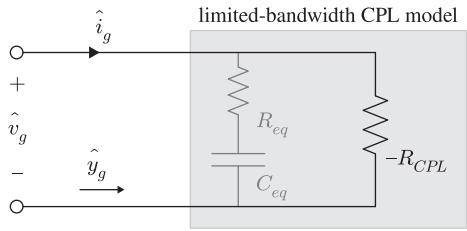

Fig. 4. Small-signal equivalent circuit model for limited-bandwidth CPLs.

R reflected across the transformer, and that it is not dependent on controller gains. This is consistent with the low-frequency behavior of CPLs: a negative resistance. At frequencies above ω_{CPL} but below the bandwidths of $H(s)$ and $Z_{ei}(s)$, the admittance is Y_{MF}. Depending on K_p, it can be positive or negative. A Bode plot of $\hat{y}_g$ is shown in Fig. 3 to show the relationship between Y_{LF}, Y_{MF}, and ω_{CPL}.

With the simplified input admittance (4), a suitable equivalent circuit model can be determined for the limited-bandwidth CPL. The circuit admittance should be Y_{LF} at frequencies below ω_{CPL}, and Y_{MF} at frequencies above ω_{CPL}. While many circuits can satisfy these conditions, the intuitive circuit shown in Fig. 4 will be used in this article.

Determining the component values R_{eq}, C_{eq}, and R_{CPL} is a matter of relating the circuit admittance below and above the circuit bandwidth to the corresponding characteristics Y_{LF}, Y_{MF}, and ω_{CPL}. This leads to the system

$$\begin{cases} -R_{\text{CPL}} &= 1/Y_{\text{LF}} \\ R_{eq}||(-R_{\text{CPL}}) &= 1/Y_{\text{MF}} \\ R_{eq}C_{eq} &= 1/\omega_{\text{CPL}} \end{cases} \tag{8}$$

and solving in terms of component values completes the equivalent circuit model

$$\begin{aligned} R_{\text{CPL}} &= \frac{-1}{Y_{\text{LF}}} \\ R_{eq} &= \frac{1}{Y_{\text{MF}} - Y_{\text{LF}}} \\ C_{eq} &= \frac{Y_{\text{MF}} - Y_{\text{LF}}}{\omega_{\text{CPL}}}. \end{aligned} \tag{9}$$

An ideal CPL model captures only the lowest frequency behavior, representing the input impedance as a negative resistor

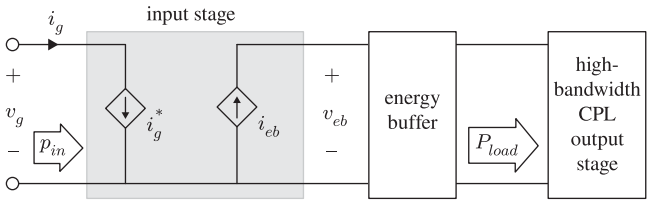

Fig. 5. Variable-bandwidth CPL with energy buffer overview.

$-R_{\text{CPL}}$. The model portrayed in (4) and Fig. 4 shows that limited-bandwidth CPLs resemble the ideal negative resistor model in the low frequency limit, but enhanced model fidelity adds virtual damping components R_{eq} and C_{eq} that are intrinsic to the converter and depend on bandwidth and converter properties.

This enhanced circuit model can be used to more realistically model CPLs in stability assessments, including CPLs implemented with no intentional virtual or passive damping or other instability mitigation. The model also suggests that an active controller tuned with the model behavior in mind could offer a variable-bandwidth input characteristic by considering the virtual variable damping leg as dependent on a selected bandwidth. A controller implemented with this capability could react to utility variations by lowering the apparent bandwidth at its input, thereby increasing the virtual damping and appearing resistive over a wider frequency range. The following section explores approaches for offering variable input impedance while simultaneously supporting load needs with an energy buffer incorporated into the power electronic controller.

III. Variable Bandwidth CPL Control

As shown in the previous section, the input behavior of CPLs depends on the control method and controller gains selected. Choosing reduced gains creates an increased virtual damping component that can improve dc-link stability. However, this reduces the quality of load regulation since input and output behavior are not independently controlled. In this section, a cascaded converter control scheme is presented that allows independent control of the input and output while managing long-term power imbalances.

With independent control of input and output behavior, the apparent bandwidth ω_{CPL} can be lowered without affecting output performance. In the presented cascaded converter, the input stage commands an input current i_g^* to virtually present the impedance (4) of a variable-bandwidth CPL. An output stage serves to provide constant power to the load at much higher bandwidth than the apparent input bandwidth by regulating load current or voltage. An energy buffer between the stages manages the resulting power ripple. A circuit overview is shown in Fig. 5, and a control scheme that implements the system is shown in Fig. 6.

A. Control Scheme and Energy Buffer Balance Control

In this section, the input voltage to energy buffer voltage transfer function, as well as the input admittance are derived. These relationships help select controller parameters for the energy buffer balancing controller G_{c3}. C_{eb} is assumed to be large enough that changes in v_{eb} are small enough for small-signal analysis to remain valid. C_{eb} is then sized in the following section according to expected input fluctuations and selected input bandwidth ω_{CPL}. The LTI analysis in this section is valid within a fixed ω_{CPL}. However, the results can be applied for all desired values of ω_{CPL} to ensure G_{c3} and C_{eb} are designed properly for variable-bandwidth CPL operation.

A reference input current i_g^* emulates the behavior of a load with the desired admittance (4) with selectable bandwidth ω_{CPL}. While Y_{MF} is also selectable, for simplicity in this analysis it is constrained such that $Y_{\text{MF}} = -Y_{\text{LF}}$. From (9), damping leg components R_{eq} and C_{eq} are then

$$R_{eq} = R_{\text{CPL}}/2$$
$$C_{eq} = 2/(R_{\text{CPL}}\,\omega_{\text{CPL}}). \tag{10}$$

High-bandwidth current control at the input stage by controller G_{c1} causes input current to follow i_g^*. High-bandwidth current control at the output stage by controller G_{c2} leads to regulated load current, and therefore, constant output power to a resistive load. To ensure balanced input and output power and to maintain the energy buffer charged to a nominal level in the long term, a balancing control loop G_{c3} supplements the reference input current i_g^* with a small current i_{bal}. Controller G_{c3} acts at low bandwidth so as to not interfere with the input impedance characteristics otherwise created by commanding reference i_g^* directly.

Analysis of the energy buffer is simplified by assuming ideal tracking of the reference commanded by current controller G_{c1}. The current i_g into the input stage is assumed to be $i_g^* + i_{\text{bal}}$. The analysis is also simplified by assuming ideal tracking of the reference commanded by G_{c2}, causing the output stage to resemble an ideal CPL, which is modeled by a negative resistor $-R_{\text{CPL2}}$.

If the input stage is assumed to be largely lossless, then current out of the input stage can be expressed as

$$i_{eb} = \frac{v_g i_g}{v_{eb}}. \tag{11}$$

When linearized about the operating point, the small-signal current is

$$\hat{i}_{eb} = \frac{I_g}{V_{eb}}\hat{v}_g + \frac{V_g}{V_{eb}}\hat{i}_g - \frac{V_g I_g}{V_{eb}^2}\hat{v}_{eb} \tag{12}$$

where capitalized variables are operating point quantities, and hatted variables are small-signal quantities. For the energy buffer, while any energy storage method may be used, here it is a capacitor C_{eb}. With these assumptions and linearizations, a simplified small-signal circuit model is shown in Fig. 7, in which

$$g_1 = \frac{I_g}{V_{eb}} \tag{13}$$

$$g_2 = \frac{V_g}{V_{eb}} \tag{14}$$

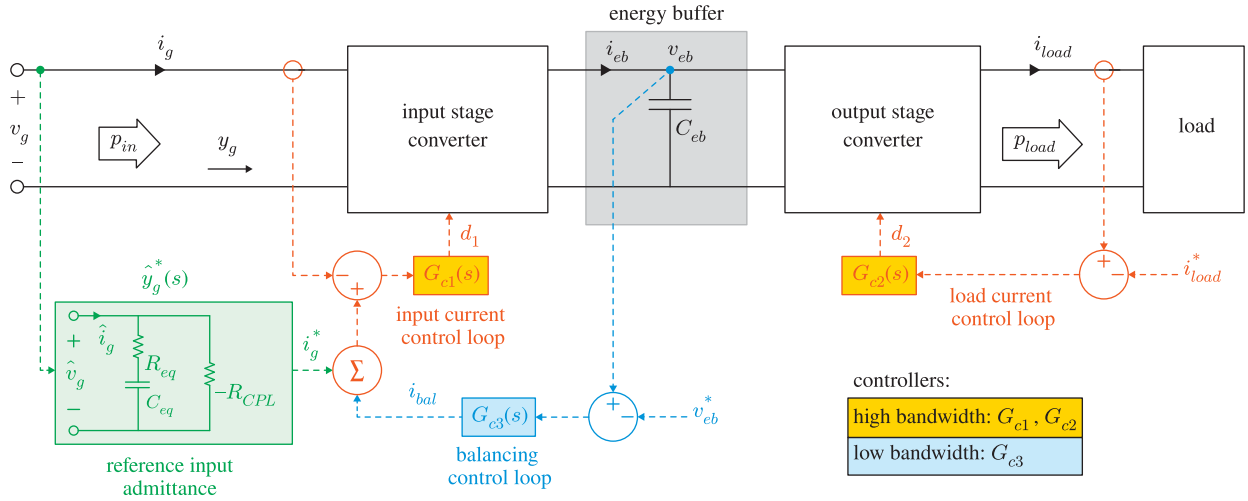

Fig. 6. Control scheme for variable-bandwidth CPL with energy buffer.

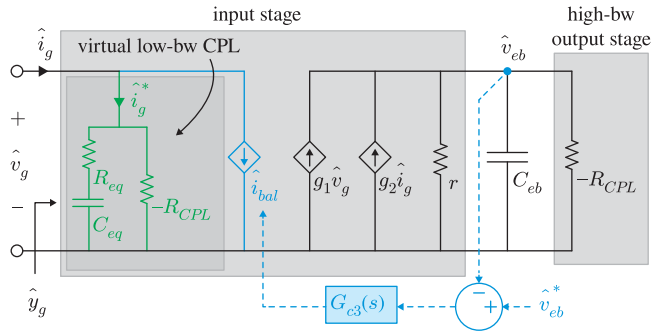

Fig. 7. Small-signal circuit for variable-bandwidth CPL with energy buffer and high-bandwidth CPL output.

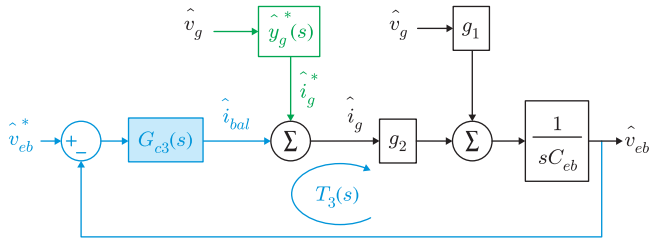

Fig. 8. Block diagram for small-signal circuit for variable-bandwidth CPL with energy buffer and high-bandwidth CPL output.

$$r = \frac{V_{eb}^2}{V_g I_g} = R_{\text{CPL2}}. \tag{15}$$

Input power p_{in} and output power p_{load} are equal to target power P during steady-state operation. Then,

$$R_{\text{CPL}} = \frac{V_g^2}{P}$$

$$R_{\text{CPL2}} = \frac{V_{eb}^2}{P}. \tag{16}$$

Components R_{eq} and C_{eq} reflect the input bandwidth as expressed in (10), with ω_{CPL} being the apparent input bandwidth. The input current, as commanded by the input stage, is

$$\hat{i}_g = \underbrace{\frac{1}{R_{\text{CPL}}} \frac{s - \omega_{\text{CPL}}}{s + \omega_{\text{CPL}}}}_{\hat{y}_g^*} \hat{v}_g + \hat{i}_{\text{bal}}. \tag{17}$$

The input stage output resistance $r = R_{\text{CPL2}}$ and the high-bandwidth CPL load $-R_{\text{CPL2}}$ cancel each other in the small-signal model, so energy buffer voltage is

$$\hat{v}_{eb} = \frac{1}{sC_{eb}}(g_1 \hat{v}_g + g_2 \hat{i}_g). \tag{18}$$

A block diagram for the model is shown in Fig. 8. The small-signal reference voltage $\hat{v}_{eb}^*$ is set to zero if the energy buffer is to remain at a constant voltage in steady state.

From the small-signal circuit and block diagram, the input voltage to energy buffer voltage transfer function can be determined

$$\frac{\hat{v}_{eb}}{\hat{v}_g} = \frac{\frac{1}{sC_{eb}}\left(g_2 \hat{y}_g^* + g_1\right)}{1 + g_2 \frac{G_{c3}}{sC_{eb}}}. \tag{19}$$

With (17) expressing input current, overall input admittance $\hat{y}_g$ can also be determined from the small-signal models

$$\hat{y}_g = \frac{\hat{i}_g}{\hat{v}_g} = \frac{\hat{y}_g^* - g_1 \frac{G_{c3}}{sC_{eb}}}{1 + g_2 \frac{G_{c3}}{sC_{eb}}}. \tag{20}$$

An example implementation of G_{c3} is a PID controller with a low-pass filter

$$G_{c3} = \frac{1}{1 + s/\omega_{Gc3}}\left(K_{p3} + K_{i3}/s + K_{d3}s\right). \tag{21}$$

The balancing loop controller G_{c3} bandwidth should be lower than that of either current controller G_{c1} or G_{c2}, as well as that of the reference input admittance $\hat{y}_g^*$. This bandwidth can be inspected from the loop gain T_3 gain crossover frequency, and

TABLE III
OPERATING POINT AND PARAMETERS FOR EXAMPLE ENERGY BUFFER CONVERTER

Param.	Value	Param.	Value	Param.	Value
V_g	90 V	I_{eb}	0.357 A	ω_{Gc3}	1 rad/s
I_g	0.556 A	V_{eb}	140 V	K_{p3}	130×10^{-6}
P	50 W	C_{eb}	82 µF	K_{i3}	18×10^{-6}
R_{CPL}	162 Ω			K_{d3}	100×10^{-6}

the closed loop transfer function $T_3/(1+T_3)$. For the example converter presented in the following section with operating point, as shown in Table III, the bandwidth of the balancing loop controller is 0.88 rad/s, and the 5% settling time is 10 s. This provides several decades of separation from higher bandwidth components in the scheme.

Current controllers G_{c1} and G_{c2} can also be implemented with PID controllers. High gains should be selected in order to achieve control bandwidths at least one decade higher than the highest bandwidth that the selectable input y_g^* may present. In the example converter presented in the following section, G_{c1} and G_{c2} operate at 5500 rad/s bandwidth, with a maximum y_g^* bandwidth of 550 rad/s.

B. Energy Buffer Sizing

At a minimum, the energy buffer C_{eb} must be large enough to never become depleted during expected input disturbances. However, additional constraints on the maximum allowable change in v_{eb} may require the use of a larger C_{eb}. This section develops a way to quantify the minimum C_{eb} required during a v_g disturbance of size Δv_g so that the energy buffer does not become depleted.

The balancing loop controls how quickly the energy buffer returns to its nominal level after an input disturbance, but it does not determine how much the charge level fluctuates during the disturbance. This is instead attributed to the reference input admittance $\hat{y}_g^*$ bandwidth ω_{CPL}. The lower the bandwidth, the longer the input draws variable power instead of constant power (and the greater the system stability). However, the energy buffer will need to provide or absorb more energy.

The energy buffer C_{eb} size and nominal voltage V_{eb} determine how great of an imbalance between input and output power can be handled, and for how long. This can be shown by expressing energy buffer power flow and determining a minimum C_{eb} required. Neglecting converter power losses, power into the energy buffer p_{eb} is

$$p_{eb} = p_{\text{in}} - P_{\text{load}} \tag{22}$$

where load power is considered constant. Separating input power into its large-signal operating point and small-signal quantities ($p_{\text{in}} = P_{\text{in}} + \hat{p}_{\text{in}}$), and noting that in steady-state input and output power are equal ($P_{\text{in}} = P_{\text{load}}$) reduces (22) to

$$p_{eb} = \hat{p}_{\text{in}}. \tag{23}$$

This means that power into the energy buffer is equal to small-signal input power. Substituting the linearized form of p_{in} into

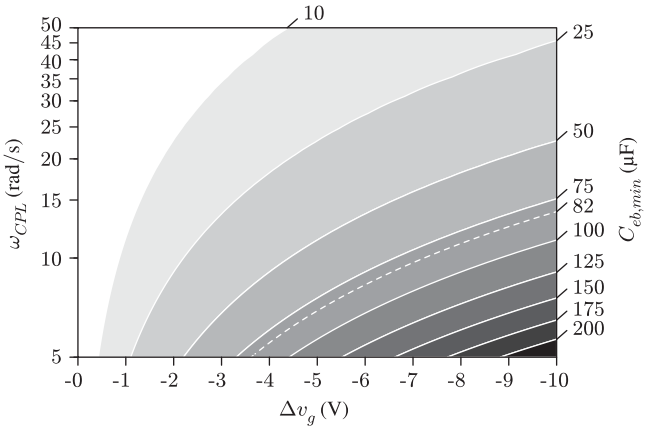

Fig. 9. Minimum energy buffer C_{eb} required during input voltage step Δv_g with input bandwidth ω_{CPL}.

(23) gives

$$p_{eb} = I_g \hat{v}_g + V_g \hat{i}_g. \tag{24}$$

To determine a minimum size for C_{eb}, consider a permanent input voltage step Δv_g, so that $\hat{v}_g = \Delta v_g$. Neglecting the small balancing current $\hat{i}_{\text{bal}}$ in (17) and taking an inverse Laplace transform, time-domain input current $\hat{i}_g$ following the voltage step is:

$$\hat{i}_g = \frac{\Delta v_g}{R_{\text{CPL}}} \left(2e^{-\omega_{\text{CPL}} t} - 1\right) \tag{25}$$

so that, from (24), power into the energy buffer is

$$p_{eb} = I_g \Delta v_g + \frac{V_g \Delta v_g}{R_{\text{CPL}}} \left(2e^{-\omega_{\text{CPL}} t} - 1\right). \tag{26}$$

Noting that operating point input current is $I_g = \frac{V_g}{R_{\text{CPL}}}$ gives

$$p_{eb} = \frac{2V_g \Delta v_g}{R_{\text{CPL}}} e^{-\omega_{\text{CPL}} t}. \tag{27}$$

Integrating p_{eb} following the input voltage disturbance at $t = 0$ gives the total energy into the energy buffer e_{eb}:

$$e_{eb} = \int_0^\infty p_{eb}\, dt = \frac{2V_g \Delta v_g}{\omega_{\text{CPL}} R_{\text{CPL}}}. \tag{28}$$

For energy buffer C_{eb} initially charged to voltage V_{eb}, during a negative step in input voltage and negative energy flow into energy buffer ($\Delta v_g < 0$, $e_{eb} < 0$), no more energy may be extracted than is initially stored, so e_{eb} must satisfy

$$-e_{eb} < \frac{1}{2} C_{eb} V_{eb}^2. \tag{29}$$

Substituting e_{eb} and solving for C_{eb} gives the minimum capacitance needed $C_{eb,\text{min}}$ to fully buffer such a step in input voltage

$$C_{eb,\text{min}} = \frac{-4V_g \Delta v_g}{\omega_{\text{CPL}} R_{\text{CPL}} V_{eb}^2}. \tag{30}$$

With nominal values, as shown in Table III, the minimum C_{eb} requirement is shown in Fig. 9 for various Δv_g and ω_{CPL}. Operating at lower bandwidth increases system stability, but requires a larger energy buffer if load power is to remain unaffected

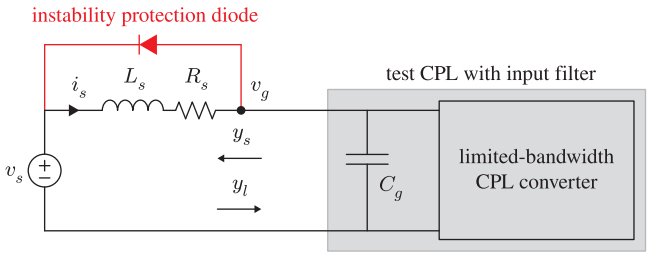

Fig. 10. Dc system test setup diagram with prototype limited-bandwidth CPL converter. A protection diode limits oscillations when system becomes unstable.

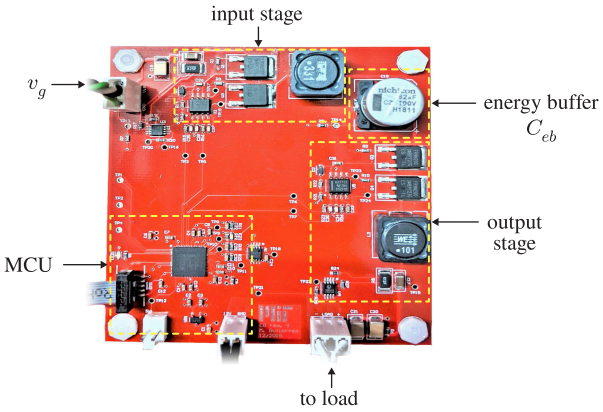

Fig. 11. Prototype variable-bandwidth CPL converter.

during input disturbances. An energy buffer sized $C_{eb} = 82\ \mu$F is chosen for this example converter and is shown in the figure with a dotted line.

IV. Test Setup and Measurements

For validation of the control scheme, the proposed converter has been implemented and tested on a dc system as diagrammed in Fig. 10, with large-signal source voltage $V_s = 93.3$ V and source impedance $L_s = 300$ mH, $R_s = 6\ \Omega$. A large source impedance allows for testing of CPL instability at a low power level P, in this case 50 W. All other parameters are as shown in Table III, and converter input capacitance is $C_g = 0.47\ \mu$F. Fig. 10 shows a protection diode is included for testing purposes to limit v_g oscillations when the system becomes unstable. The prototype converter used in testing is pictured in Fig. 11.

With the system and converter as described, a calculated locus of system poles as input bandwidth ω_{CPL} varies is shown in Fig. 12. As expected, increasing bandwidth leads to instability. The locus suggests that stability is achieved with $\omega_{\text{CPL}} < 500$, and overdamped performance is achieved with $\omega_{\text{CPL}} < 100$ rad/s.

Two models are used to compare converter performance. The first is a reference model that assumes the converter exactly resembles the limited-bandwidth CPL model from Fig. 4. The second is a linearized average model that includes the controllers and energy buffer shown in Fig. 6. To compare the converter with these models, a test is shown in Fig. 13 in which the source voltage v_g is stepped -5 V from its nominal 93.3 V while source current i_s is measured. The test is performed for varying

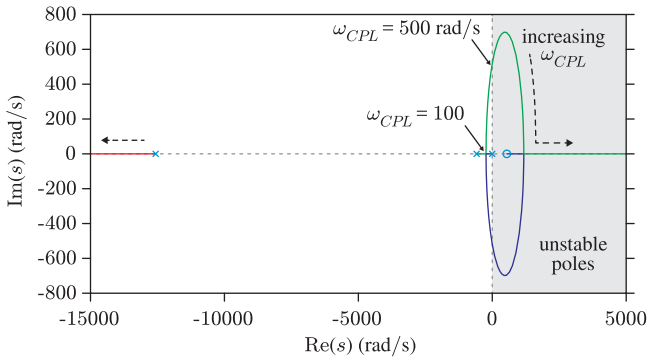

Fig. 12. Locus of system poles as ω_{CPL} varies. Suggests critical stability at $\omega_{\text{CPL}} = 500$ rad/s.

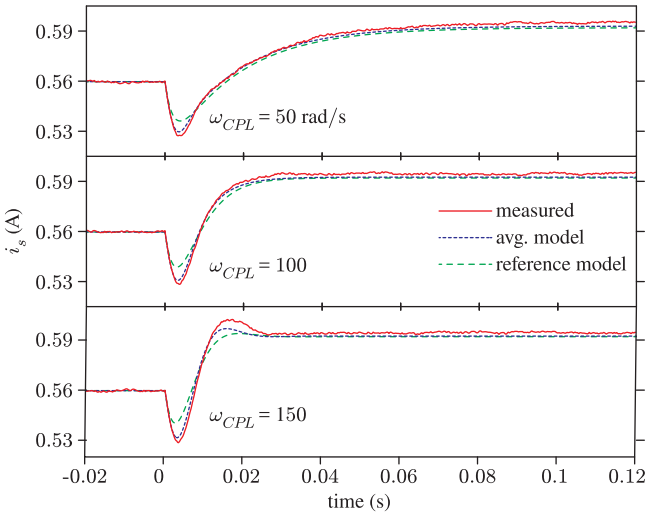

Fig. 13. Measured input current versus -5 V step in source voltage for three input bandwidths. Compared against linearized average model and reference model of limited-bandwidth CPL converter.

CPL bandwidths. Current falls as the converter initially appears resistive, and then steadily rises above nominal to draw constant input power in the long term. As CPL bandwidth is increased, input current rises more quickly and the load appears resistive for a shorter duration. Decreased stability is seen as bandwidth is increased. The measurements agree with the average model and agree with the reference model at lower CPL bandwidths. The effects of the energy buffer are seen in the difference between the average and reference model.

A longer time-scale transient test is shown in Fig. 14. A low CPL bandwidth allows additional comparison of the models and converter and displays operation of the energy buffer. Source current is again stepped -5 V, but with CPL bandwidth set to 10 rad/s. Additionally, input power, output power, and energy buffer voltage are measured. The effects of controller G_{c3} in recharging the energy buffer following an input disturbance are shown. Following the step, input current is slightly higher than that of the reference model as increased input power restores the depleted energy buffer. The test also shows that throughout the disturbance, output power remained undisturbed.

The benefit of a controllable input bandwidth is that unstable situations can be mitigated electronically by the load. A test

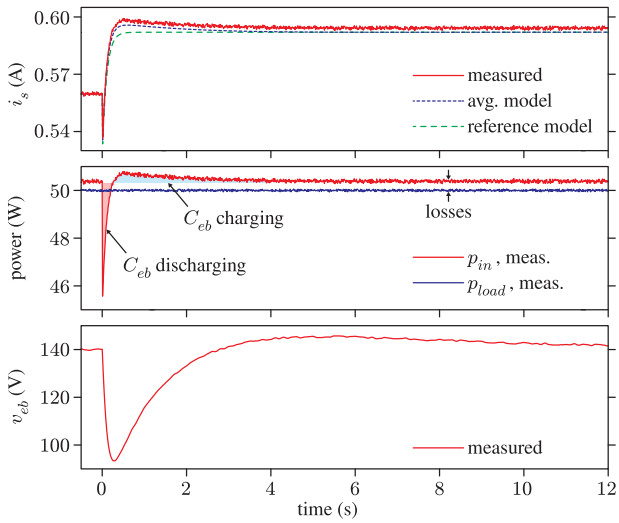

Fig. 14. Measured input current, input and output power, and energy buffer voltage versus −5 V step in source voltage with converter bandwidth $\omega_{\text{CPL}} = 10$ rad/s. Energy buffer is recharged by low-bandwidth controller G_{c3}.

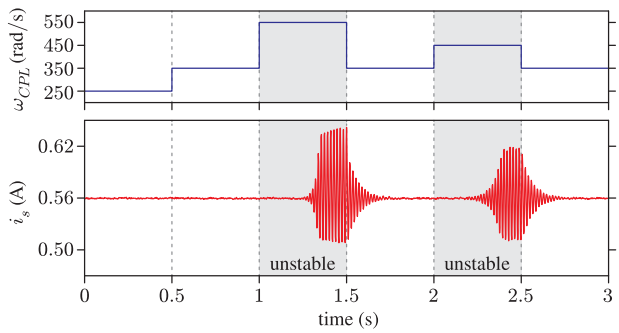

Fig. 15. Measured source current as ω_{CPL} varies. Unstable current occurs when ω_{CPL} exceeds 350 rad/s.

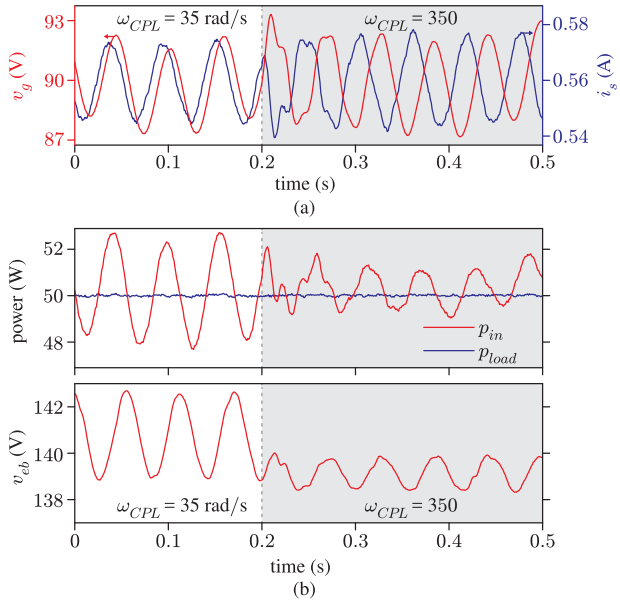

Fig. 16. (a) Source voltage and current as converter switches from $\omega_{\text{CPL}} = 35$ to 350 rad/s during a sinusoidal input fluctuation. (b) Input and output power, and energy buffer voltage during same test.

is shown in Fig. 15 in which source current is measured as selectable CPL bandwidth ω_{CPL} varies. Instability occurs when ω_{CPL} is pushed beyond 350 rad/s. However, stable operation is restored when the bandwidth is reduced. These on-demand bandwidth changes are made electronically by the converter.

Changing input bandwidth can also be observed in a change in phase between input voltage and input current. This is demonstrated in Fig. 16 in a test that shows the converter switching from $\omega_{\text{CPL}} = 35$ to 350 rad/s while source voltage is perturbed by a 2-V, 17.5-Hz sine wave. Fig. 16(a) shows the input is capacitive at $\omega_{\text{CPL}} = 35$, and negative resistive at $\omega_{\text{CPL}} = 350$ rad/s. Fig. 16(b) shows that a higher input bandwidth leads to a lower input power ripple, which leads to decreased energy buffer voltage ripple as well. Output power p_{load} remains tightly regulated.

V. Conclusion

This article explored how system stability can be approached from a load point of view, and that loads with programmable input behavior are a useful tool for this approach. As a specific example, the issue of CPL instability was analyzed. A nonideal CPL model was developed that showed how limitations of power electronics in CPLs can be used to develop a stabilization technique. The resulting limited-bandwidth CPL model was used to show that system instability due to CPLs can be mitigated if the CPL bandwidth is reduced. A control method was presented to virtually present a load as a limited-bandwidth CPL with a selectable bandwidth. This method includes the use and balance of an intermediate energy buffer that allows the load to retain high bandwidth regulation. Testing measurements from a prototype converter implementing this design on a small-scale dc system were presented. They showed that controllable input bandwidth allows the load to influence system stability, and the use of an energy buffer allows load power to remain constant throughout input fluctuations.

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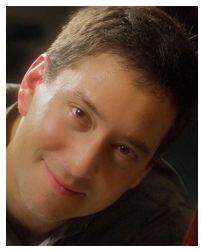

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