A Comparison of Multirate Digital Compensators for a Battery Charger

Deron K. Jackson Steven B. Leeb Aaron M. Schultz Ahmed Mitwalli

Laboratory for Electromagnetic and Electronic Systems
Massachusetts Institute of Technology
Cambridge, MA 02139, USA

Abstract — **In a *regulation* application, a power supply is typically tasked with maintaining a fixed voltage or current in the face of possible disturbances. In a *tracking* application, on the other hand, a controller works to cause an average output voltage or current to follow a desired reference waveform as a function of time or some other variable. This paper describes a large-signal linear, multirate digital controller for, among other possible applications, charging electric vehicle batteries. This controller permits the charger to track and deliver a desired current trajectory for a wide range of loads while providing a unity-power-factor interface to the electric utility.**

I. Introduction

We are engaged in exploring the use of a boost-type UPF rectifier in a charging system illustrated in the block diagram in Figure 1. This system is similar to topologies considered in [1]. Power is transferred to the vehicle through an inductive coupling, which is considered by some to maximize operator safety and connector life [2 – 7]. This architecture is general in the sense that, even if an inductively coupled connector interface is not desired, safety isolation and ground fault protection are nearly always desired. That is, some high-frequency transformer with an inverter is likely to be part of the charger. The system shown in Figure 1 could as easily be used with an ohmic connector by moving the entire charger into the vehicle.

A bridge inverter, operating from a DC link created by the UPF rectifier, impresses a high frequency AC signal on the primary of a relatively lightweight inductive coupling. Unity-power-factor operation is essential to ensure maximum power delivery for the fastest possible charging and to minimize the generation of harmonic currents. The voltage on the secondary side of the coupling is applied to the battery charging circuitry inside the vehicle. The inverter operates with a fixed frequency and duty cycle to maximize efficiency. To alter the charging current, the charging current controller modifies the DC-link voltage created at the output of the UPF rectifier. In our prototype, a fiber-optic transceiver relays information about the charging current to the charging station while maintaining safety isolation.

In contrast to UPF controllers for typical regulation applications, the charging system requires a controller whose stability is verifiably guaranteed over a wide range of operating conditions. Also, for adequate tracking performance, the controller may need to respond swiftly to command changes or load disturbances over this range. This paper describes a multirate digital controller for battery charging that meets these demands.

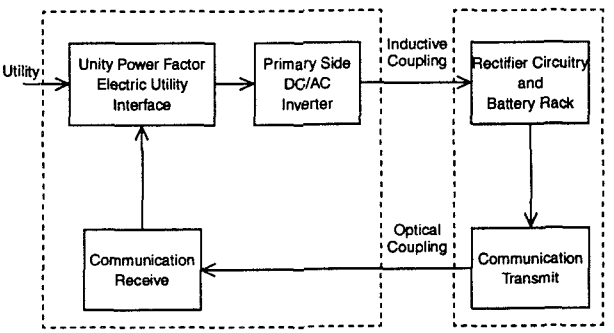

Figure 1: Charging system overview.

II. Background

A boost converter as shown in Figure 2 serves as the UPF rectifier in the battery charger. The input voltage is the rectified AC utility voltage. All voltage and current variables in Figure 2 refer to quantities averaged over at least one switch period, i.e., switching ripple will be ignored in the following discussion. An inner current loop controls the input or inductor current $i_L(t)$ to follow a desired reference waveform $i_p(t)$ by providing an appropriate pulse-width-modulated switching sequence to the controllable switch. To ensure UPF operation, the reference waveform $i_p(t)$ is a scaled copy of the rectified input voltage waveform. An outer, voltage-loop controller can adjust v_o to a desired value by varying the scale factor k used to compute $i_p(t)$. Changing k is tantamount to changing input power.

In [8] and [9], a large-signal linear, "power balance" model of the boost UPF rectifier was derived using Tellegen's theorem [10]. Assuming that the inner current loop works well, the inductor current waveform is presumed to be

0-7803-3977-0/96 $10.00 © 1996 IEEE

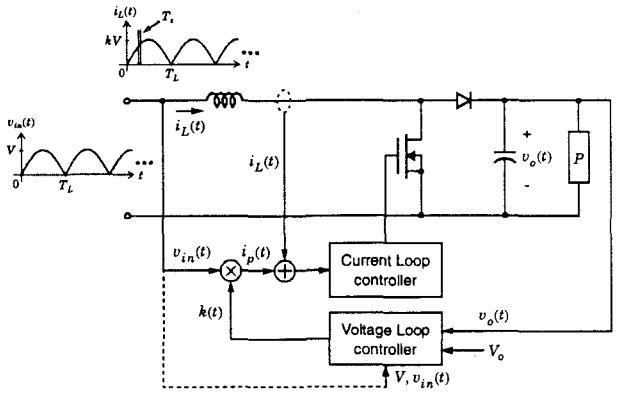

Figure 2: High-power-factor preregulator.

a scaled copy of the input voltage waveform, i.e., $i_L(t) = kv_{in}(t)$. Also, to ensure unity-power-factor operation, it is presumed that k and the load power, P, will vary no more frequently than once per rectified line cycle. With these assumptions, the following sampled data model of the boost rectifier may be developed:

$$x[n+1] = x[n] + \frac{T_L V^2}{C} k[n] - \frac{2T_L}{C} P[n] \qquad (1)$$

where the state variable $x[n]$ denotes the value of the squared output voltage at the beginning of the n^{th} cycle. Similarly, $k[n]$ and $P[n]$ represent the value of the scale factor k and the load power, respectively, during the n^{th} cycle. The variable T_L represents the period of one rectified input line cycle, i.e., $1/T_L = 120\text{Hz}$. The index n in the sampled data model, (1), increments once every T_L seconds. The sampled data, power balance model of the boost rectifier is illustrated schematically with the use of the z-transform [11] in Figure 3.

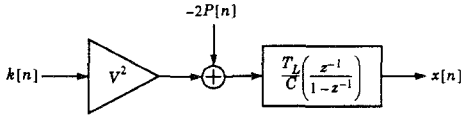

Figure 3: Boost converter sampled data model.

Because this model is not a small-signal approximation, it is especially suitable for use in developing a controller for tracking applications like the battery charger. Because it is a sampled data model, it is a convenient starting point for developing a digital controller. We begin by developing a discrete-time (DT) controller for the squared output voltage, since this is the state variable described by the power balance model. Charging current is controlled by a DT outer loop that computes the reference for the inner voltage loop. The total charging system consists of a multirate cascade of three nested control loops, listed from highest to lowest closed-loop tracking bandwidth: an innermost current loop to control and shape the input current to the boost converter; a voltage loop to control the output bus voltage; and an outermost current control loop to track the desired output charging current profile. In our prototype, the inner current loop is implemented with analog hardware. The outer voltage and current loops are implemented on a digital microcontroller.

III. Voltage Control

In [9], [10] and [12], the voltage loop is stabilized with the discrete-time version of a *proportional-integral* (*PI*) compensator. We have found, however, that an alternative *pole-placement* (*PP*) algorithm yields improved performance. This new algorithm is outlined below and compared to its *PI* counterpart.

The pole-placement algorithm employs full state feedback which, in principle, allows for arbitrary placement of the closed-loop poles. Formulation of the control loop begins with the control command k. The control command k is chosen as

$$k[n] = k[n-1] + \frac{C}{T_L V^2}\Big(G_1(X[n]-x[n]) + G_2(X[n]-x[n-1])\Big) \qquad (2)$$

where $X[n]$ is the squared-voltage reference. The constants G_1 and G_2 are feedback gains. The $k[n-1]$ term incorporates the effect of an accumulator directly. Therefore, $k[n]$ can only be in steady-state when the two error terms, $(X[n] - x[n])$ and $(X[n] - x[n-1])$, are both zero.

Combining (2) and (1) yields the following state-space description of the closed voltage loop:

$$\begin{bmatrix}\sigma_x[n+1]\\ x[n+1]\end{bmatrix} = \begin{bmatrix}0 & 1\\ -(1+G_2) & 2-G_1\end{bmatrix}\begin{bmatrix}\sigma_x[n]\\ x[n]\end{bmatrix} + \begin{bmatrix}0\\ G_1+G_2\end{bmatrix}X[n] + \begin{bmatrix}0\\ \frac{-2T_L}{C}\end{bmatrix}(P[n]-P[n-1]). \qquad (3)$$

The variable $\sigma_x[n]$ is defined as

$$\sigma_x[n+1] = x[n] \qquad (4)$$

and it accounts for the added state from the $x[n-1]$ term in (2). This compensation unfortunately results in a voltage loop that is dependent on the load power $P[n]$. We will see in the next section that the inability to guarantee the voltage-loop dynamics independently of the load would significantly complicate the development of the outer charging current control loop. To make the voltage-loop dynamics independent of load power, the control command in the charger pro-

totype is computed as in (2), but with the addition of a power feedfoward term:

$$\tilde{k}[n] = \tilde{k}[n-1] + \frac{2}{V^2}\Big(P[n]-P[n-1]\Big) + \frac{C}{T_L V^2}\Big(G_1(X[n]-x[n]) + G_2(X[n]-x[n-1])\Big). \quad (5)$$

In a charging circuit, both load terminal voltage and terminal current will be available, and computing load power requires little additional expense or computational effort. Substituting (5) into (1) yields a new second-order, large-signal linear model for the actively controlled boost converter:

$$\begin{bmatrix}\sigma_x[n+1]\\ x[n+1]\end{bmatrix} = \begin{bmatrix}0 & 1\\ -(1+G_2) & 2-G_1\end{bmatrix}\begin{bmatrix}\sigma_x[n]\\ x[n]\end{bmatrix} + \begin{bmatrix}0\\ G_1+G_2\end{bmatrix}X[n]. \quad (6)$$

A closed-loop DT transfer function from $X[n]$ to $x[n]$ is obtained using the z-transform.

$$\overline{H}_{PP}(z) = \frac{(G_1+G_2)z}{z^2+(G_1-2)z+(G_2+1)}. \quad (7)$$

The system poles are

$$z_1, z_2 = \frac{(2-G_1) \pm \sqrt{G_1^2-4(G_1+G_2)}}{2} \quad (8)$$

and there is a finite zero located at $z = 0$. The complete system with the voltage loop closed is shown schematically in Figure 4. Selecting gains G_1 and G_2 so that these poles have

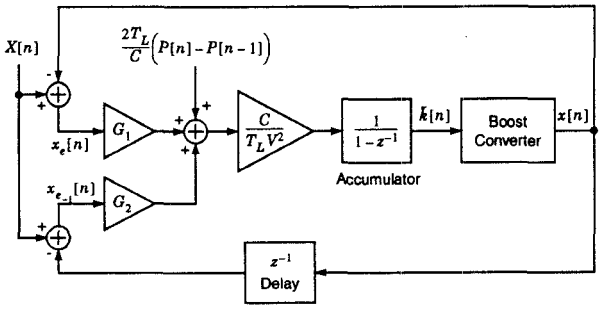

Figure 4: Voltage loop.

magnitude less than one results in a stable system. Once gains have been calculated to yield stable closed-loop pole locations, the system will remain stable for practically any load because (6) is independent of load power. The stable voltage loop will converge to any reference given sufficient time. This guaranteed convergence substantially simplifies the construction of the charging current control loop.

In [12], a *PI* controller was used to stabilize the voltage loop. This controller was formed using the following control command

$$\tilde{k}[n] = \frac{C}{T_L V^2}\Big(G_1(X[n]-x[n]) + G_2\sigma_v[n]\Big) + \frac{2}{V^2}P[n] \quad (9)$$

where $\sigma_v[n]$ is a voltage accumulator defined as

$$\sigma_v[n+1] = \sigma_v[n] + (X[n]-x[n]). \quad (10)$$

The resulting closed-loop DT state-space and transfer function descriptions are given in (11) and (12) below.

$$\begin{bmatrix}\sigma_v[n+1]\\ x[n+1]\end{bmatrix} = \begin{bmatrix}1 & -1\\ G_2 & 1-G_1\end{bmatrix}\begin{bmatrix}\sigma_v[n]\\ x[n]\end{bmatrix} + \begin{bmatrix}0\\ G_1\end{bmatrix}X[n] \quad (11)$$

$$\overline{H}_{PI}(z) = \frac{G_1\left(z+\frac{(G_2-G_1)}{G_1}\right)}{z^2+(G_1-2)z+(1+G_2-G_1)} \quad (12)$$

The closed-loop poles are

$$z_1, z_2 = \frac{(2-G_1) \pm \sqrt{G_1^2-4G_2}}{2} \quad (13)$$

and a finite zero exists at $z = -\frac{(G_2-G_1)}{G_1}$.

The relative performance of the two voltage loops can be judged by comparing their step responses. Values for G_1 and G_2 were calculated for each system that place the closed-loop poles at $z_1 = z_2 = 0.75$. The unit-step responses of the resulting systems are plotted in Figure 5. Figure 5

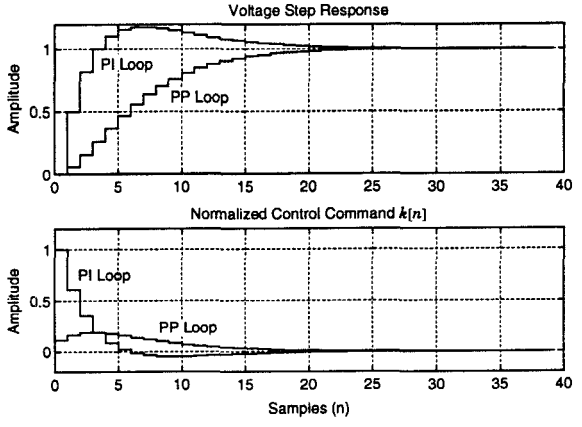

Figure 5: Simulated voltage-loop responses.

demonstrates two clear advantages of the *PP* loop in contrast to its *PI* counterpart. First, the response of the *PP* loop has zero overshoot versus about 18% for the *PI* loop. Voltage overshoot is undesirable in this application because it leads to a comparable current overshoot which may complicate design of the charging current loop. Second, the *PP* loop achieves settling times equal to the *PI* loop with a much

lower peak control command. Figure 5 shows the peak value of $k[n]$ for the *PP* loop to be only 19% of the peak *PI* command. This is critical to avoid input command (and hence input power) saturation.

The *PP* voltage loop was implemented in our prototype charging system. The closed-loop poles were set at $z_1 = z_2 = 0.75$. The voltage-loop command was programmed to step periodically between an output voltage of 300 and 350 Volts. The experimental results are plotted in Figure 6. The first two seconds in the figure show the soft-start mechanism of the converter after which closed-loop command following begins. The dashed line in Figure 6 represents the voltage command.

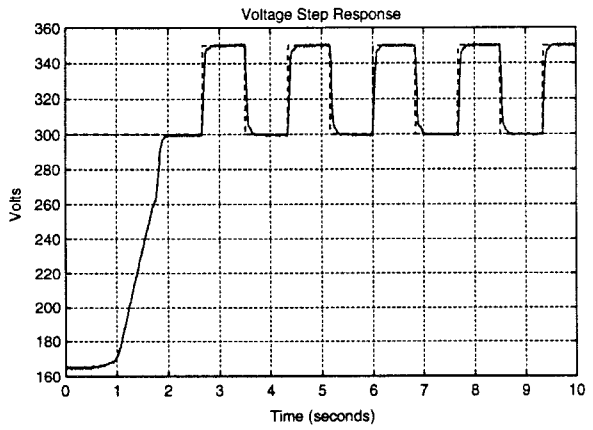

Figure 6: Step response of the voltage loop.

IV. Charging Current Control

The outermost control loop in the battery charger ensures that the output charging current tracks a current reference. This loop creates a desired charging current by computing an appropriate voltage command reference for the voltage loop to follow. The complete system is illustrated schematically in Figure 7. The dashed voltage-loop box in Figure 7 represents the boost converter and voltage-loop control circuitry shown in Figure 4.

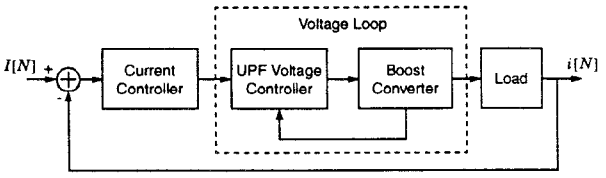

Figure 7: Current loop block diagram.

The load dynamics for a wide range of loads (e.g., battery types) are easily represented in the charging current loop by a driving point admittance. Given the availability of a function relating applied terminal voltage to load current, a natural and convenient formulation for the current loop is to assume that load or charging current will be sensed, and a desired terminal voltage will be created by the action of the current loop computation and the voltage amplifier (boost converter and voltage loop). However, it is not the output voltage but the squared output voltage that is the state controlled by the voltage loop. This complicates the formulation of a complete state-space description for the full three-loop system.

The guaranteed convergence of the voltage loop, independent of load dynamics, facilitates simplifying assumptions. Recall that the DT voltage loop operates with sample step index n. The current loop will be designed to operate with sample index $N = Qn$ where Q is a positive integer. That is, every step of the DT current loop corresponds to Q steps of the voltage loop. This *multirate* arrangement makes it possible to model the voltage-loop dynamics, from the standpoint of the outer current loop, in any of several simplified ways. Two approaches will be considered here: a delay

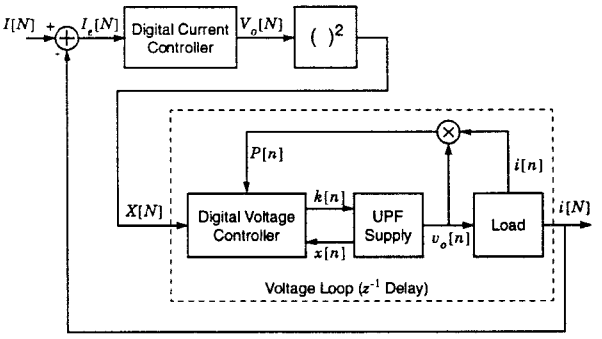

Figure 8: Current control system.

model of the voltage loop appropriate for resistive loads, and a zero-order-hold model appropriate for loads representable as combinations of linear, time invariant (LTI) circuit elements and independent sources.

A. Delay Model

One possibility, employed in our prototype with a resistive load, is to select Q and the closed-loop pole locations of the voltage loop so that the output bus voltage will converge to a new reference X in a single step of the current-loop index N. That is, the current loop computes a voltage reference at time N. This reference is squared and supplied as the command reference to the inner voltage loop. With the proper choice of Q and the voltage-loop poles, the output bus voltage will have converged to the reference command supplied by the current loop by time $N + 1$. Under these assumptions, the voltage loop may be modeled as a unit

delay on the slow, current-loop time scale. This arrangement is illustrated in Figure 8. Signals in the figure are indexed by "n" or "N", depending on whether they are part of the fast voltage loop or slow current loop, respectively.

With a resistive load, and modeling the voltage loop as a unit delay on the time scale of the current loop, the charging current loop may be stabilized most simply with a DT compensator similar to that used in the voltage loop. The reference voltage V_o is defined as

$$V_o[N] = V_o[N-1] + G_3(I[N] - i[N]) \tag{14}$$

where G_3 is a contained gain.

Modeling the action of the voltage loop as a unit delay on the time scale of the current loop, the output voltage applied to the load is equivalent to the delayed command signal, i.e.,

$$V[N+1] = V_o[N] = V_o[N-1] + G_3(I[N] - i[N]). \tag{15}$$

With a resistive load, a state equation for i can be written using (15) and Ohm's law:

$$i[N+1] = i[N] + \frac{G_3}{R}(I[N] - i[n]). \tag{16}$$

Application of the z-transform to (16) yields a transfer function from $I[N]$ to $i[N]$ for the charging current loop:

$$\overline{H}_I(z) = \frac{\frac{G_3}{R}}{z + \frac{G_3}{R} - 1}. \tag{17}$$

In the z-plane, the closed-loop system has a single pole at

$$z = \frac{G_3}{R} - 1. \tag{18}$$

The stability and transient characteristics of the current loop may be adjusted by selecting an appropriate gain G_3.

B. Zero-Order-Hold Model

For a resistive load, load terminal voltage is proportionally related to load terminal current. This made it easy to step from (15) to (16) while developing the current loop in the previous section. For a more complicated LTI load model, the delay model of the voltage loop may not be as easy to apply. In this case, we can exploit the guaranteed, large-signal transient characteristics of the voltage loop to develop other useful control models and approaches.

Once again, the DT current loop steps with index $N = Qn$ where n is the index of the voltage loop and Q is a positive integer. We now add the additional constraint that the voltage loop, given a new reference, will drive the output voltage to this reference in *many* fewer than Q steps of the index n. This condition is ensured through judicious selection of Q and the closed-loop pole locations of the voltage loop. Given these conditions, the voltage loop may be modeled as a zero-order-hold (ZOH) on the time scale of the outer current loop.

For an LTI load, the load terminal current can be related to the applied terminal voltage by an expression for the driving point admittance of the load, represented henceforth by the CT Laplace transform $H(s)$.[1] Assuming that Q steps of the index n are substantially longer than the time required for the voltage loop to settle to a new command reference, the CT voltage applied to the load will appear "pulse like" throughout one step of the index N, i.e., the operation of the voltage loop will closely approximate that of a zero-order-hold. The current-loop controller will provide a command reference to the voltage loop, and will also sample the load current, on each step of the current-loop index N. Figure 9 schematically illustrates this arrangement. The zero-order-hold block represents the boost converter with voltage loop.

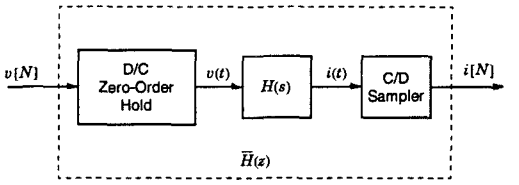

Figure 9: Driving point characteristic.

The ZOH and sampling operations in Figure 9 model the interface between the CT driving point characteristic of the load and the DT current loop [14]. The DT driving point admittance can be described as a z-transform $\overline{H}(z)$. The admittance $\overline{H}(z)$ is related to $H(s)$ by a *step-invariant transformation* [11].

Given $H(s)$, the DT transfer function $\overline{H}(z)$ may be computed as follows:

- Compute the step response of $H(s)$. That is, calculate the inverse Laplace transform of $\frac{H(s)}{s}$.
- Sample the resulting continuous-time step response $y(t)$ to obtain $y[N] = y(NT)$.
- Determine the z-transform of $y[N]$, denoted by $\overline{Y}(z)$.
- The z-transform $\overline{Y}(z)$ represents the step response of the DT transfer function $\overline{H}(z)$, i.e. $\frac{z\overline{H}(z)}{z-1}$. To find $\overline{H}(z)$, multiply $\overline{Y}(z)$ by $\frac{z-1}{z}$.

[1] Many loads of interest can be modeled as circuits consisting of LTI circuit elements, or as switched circuits that are piecewise LTI. Most batteries, on the other hand, tend to exhibit nonlinear driving point current/voltage characteristics. It is often possible, however, to develop LTI or piecewise LTI battery models; see [13] for example.

Tables relating common functions $H(s)$ to their "pulse" transfer functions $\overline{H}(z)$ may be found in many texts. (See [14], for example.)

In general, complex load models will add state variables to the overall current-loop state-space description. In such cases, the current-loop state equations will generally be more complicated than those summarized in (16). Gains might have to be adapted and/or different compensation schemes might be needed for different loads. Fortunately, the digital implementation of the current-loop controller accommodates these changes.

The approach outlined in this section requires that the voltage loop converge to its reference in many fewer than Q steps of the index n. This limits the performance of the current loop. In principle, however, the voltage loop can be made *deadbeat* [10], i.e., the voltage loop can converge in two steps of the index n, or one electrical input line cycle. This, of course, is subject to the limitations imposed by the maximum current command that can be followed by the inner current loop and by the discharge rate made possible by the loading conditions. Nevertheless, the achievable, practical performance appears to be more than adequate for high performance battery charging applications.

V. Experimental Results

The 1500W boost converter used in the prototype utilized an interleaved design. The converter consists of eight identical stages, which together feed an output capacitance of approximately 1410μF. For these preliminary tests, a 143.8Ω resistor was used as a load. Each boost stage is composed of a 540μH inductor, a Motorola MTW14N50E MOSFET, and a Motorola MUR 1560 diode. The switching frequency for each stage is 25 kHz, however, the individual clocks are shifted in phase from each other by $1/8^{th}$ of the 25 kHz period. This results in a net current ripple frequency of 200 kHz. This type of converter has several advantages over a conventional, non-interleaved, design and a thorough analysis of this converter can be found in [15].

The inner current loop operates using averaged current mode control similar to previous designs [9], [12]. However, this inner current loop was implemented with discrete analog circuitry since a single chip PFC controller such as the Unitrode UC3854 does not currently exist for interleaved converters [16]. Both the digital voltage and charging current controllers were implemented on a single Intel 80C196KC microcontroller (with plenty of spare processing power). Code for the microcontroller was developed in the C programming language using a cross-compiler from Intel [17].

The operation of the voltage-loop controller was synchronized to the period of the rectified line, T_L, by an external interrupt generated from the AC line. For tests with the resistive load, the delay model of the voltage loop was used to develop the charging current controller. The charging current-loop index N in the prototype increments once for every 15 steps of the voltage-loop index n. The gain G_3 was selected to locate the closed-loop pole at $z = 0.20$.

Figure 10 shows the steady-state input current and voltage before any control action commences. The input current and voltage are measured at the AC line before the full-wave rectifier that precedes the boost converter. Initially, all three control loops are inactive, and the MOSFETs in the boost converter are held in the off state. The input current exhibits the "spikey" shape that typically occurs when a sinusoidal voltage is rectified and used to charge a capacitor. When the output voltage stabilizes, the inner current loop is activated. The input current assumes the shape and phase of the input voltage waveform, indicating the inner current loop is functioning properly. The 80C196KC performs a "soft start" by sending open-loop scale factor commands to the inner current loop, causing the input current to rise gently until the output voltage/current is close to a desired initial operating point. At this time, the processor initializes the voltage and charging current loops in the microprocessor, and closed-loop control of the output current begins. Figure 11 shows the steady-state input current and voltage after the control loops have been activated.

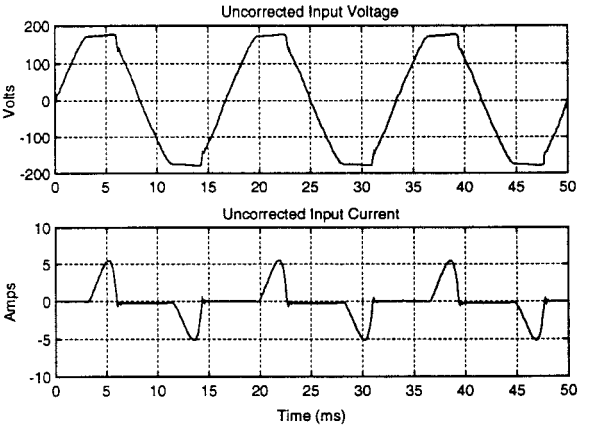

Figure 10: Input current and voltage without PFC.

Figures 12 and 13 show the output current during two different tests with the converter. Each figure shows a charging current command reference (dotted/dashed line) and the experimental curve (solid line) from the actual hardware prototype. In Figure 12 the current command reference is a square waveform, and in Figure 13 the command reference is a sawtooth waveform. The soft-start procedure dominates the first approximately 3 seconds of each output current pro-

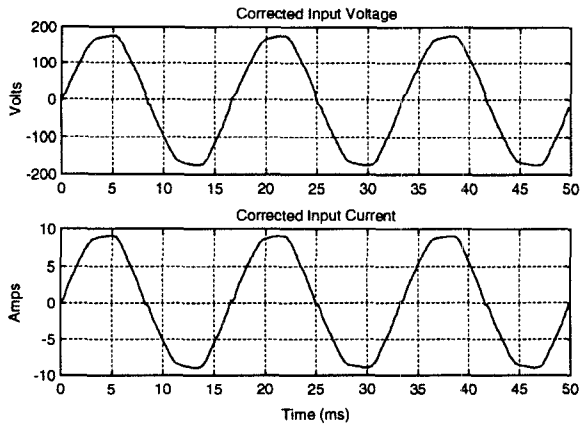

Figure 11: Input current and voltage with PFC.

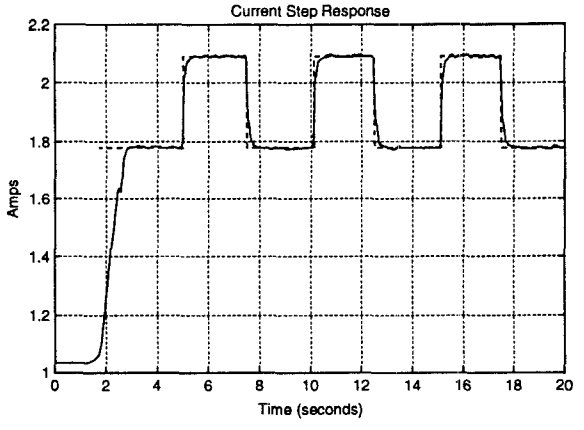

Figure 12: Step response of the charging current loop.

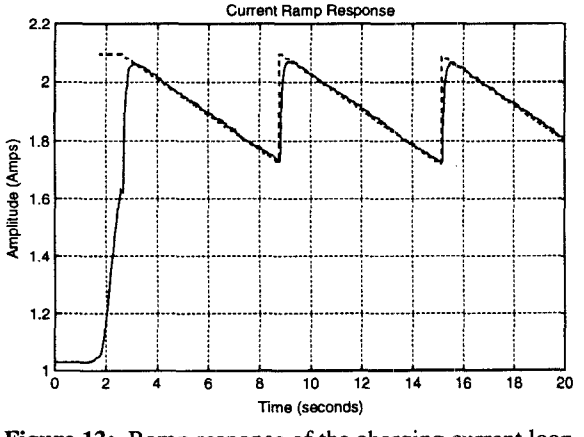

Figure 13: Ramp response of the charging current loop.

file. After the soft start, when the current- and voltage-loop controllers engage, the output current closely follows the command reference.

VI. Conclusions

The sample experiments reviewed in the previous section are representative of many similar laboratory tests. They indicate that the voltage-loop controller, with load power feedfoward as described in (6), operates as anticipated. The voltage-loop dynamics can therefore be guaranteed with minor restrictions on load behavior, permitting us to approximate the voltage-loop behavior in a number of different ways from the standpoint of the outer charging current loop. The experiments presented here directly demonstrate the performance of the charging current loop and its close agreement with predicted results.

The pole placements for the charging current and voltage loops in the prototype were not aggressive, i.e., the transient response could be improved, if necessary. We are working to test the performance of the controller with different, more challenging loads and load models. Also, we are engaged in studying the robustness of the multirate cascade controller in the face of load model errors or uncertainties, which may be of special concern in a field version of a battery charger, where significant deviations or drift in battery parameters may occur. The digital implementation of the charging current and voltage loops makes it easy to consider adaptive or scheduled control compensation for different loads in the field.

Acknowledgments

This research was funded by Amp, Incorporated. Additional funding was provided by MIT's Carl Richard Soderberg Career Development Chair. The authors gratefully acknowledge the valuable advice, support, and encouragement of Dr. Howard Peiffer, Joseph Sweeney, and Professor James L. Kirtley, Jr. Essential hardware for this project was made available through generous donations from the Intel Corporation and Tektronix.

References

[1] K.W. Klontz, A. Esser, P.J. Wolfs, and D.M. Divan, "Converter Selection for Electric Vehicle Charger Systems with a High-Frequency High-Power Link," *PESC*, June 1993, pp. 855–861.

[2] J.G. Bolger, C.A. Haslund, and R.J. Risser, "Inductive Charging of Electric Vehicles: Testing and Evaluation of an Automated System," *11th International Electric Vehicle Symposium*, September 1992, pp. 1–12.

[3] D.M. Divan, K.W. Klontz, R.D. Lorenz, and D.W. Novotny, "Contactless Power Delivery System for Mining Applications," *IEEE IAS Annual Meeting*, October 1991, pp. 1263–1269.

[4] A. Esser, "Contactless Charging and Communication System for Electric Vehicles," *IEEE IAS Annual Meeting*, October 1993.

[5] A.W. Kelley and W.R. Owens, "Connectorless Power Supply for an Aircraft-Passenger Entertainment System," *IEEE Transactions on Power Electronics*, Vol. 4, No. 3, July 1989, pp. 348–354.

[6] A. Ghahary and B.H. Cho, "Design of a Transcutaneous Energy Transmission System Using a Series Resonant Converter," *IEEE Transactions on Power Electronics*, Vol. 7, No. 2, April 1992, pp. 261–269.

[7] D.J. Hind, "Inductively Coupled Battery Charging System," *Seventh Annual Battery Conference*, April 1992.

[8] K. Mahabir, G.C. Verghese, V.J. Thottuvelil, and A. Heyman, "Linear Averaged and Sampled Data Models for Large Signal Control of High Power Factor AC-DC Converters," *PESC*, June 1990, pp. 291–299.

[9] A.H. Mitwalli, S.B. Leeb, G.C. Verghese, and V.J. Thottuvelil, "An Adaptive Digital Controller for a Unity Power Factor Converter," *IEEE Transactions on Power Electronics*, Vol. 11, No. 2, March 1996, pp. 374–382.

[10] J.G. Kassakian, M.F. Schlecht, and G.C. Verghese, *Principles of Power Electronics*, Addison-Wesley, 1991, pp. 395–399.

[11] W.M. Siebert, *Circuits, Signals, and Systems*, McGraw-Hill, New York, New York, p. 370.

[12] A.M. Schultz, S.B. Leeb, A.H. Mitwalli, D.K. Jackson, G.C. Verghese, S.R. Shaw, "A Multirate Digital Controller for an Electric Vehicle Battery Charger," *PESC*, June 1996, pp. 1919–1925.

[13] D.Temkin, M. McVey and U. Carlsson, "A Spacecraft Electrical Battery Simulator," *Intersociety Energy Conversion Engineering Conference*, August 1990, pp. 19–26.

[14] K. Astrom and B. Wittenmark, *Computer Controlled Systems*, Prentice-Hall, Inc., 1984.

[15] B.A. Miwa, "Interleaved Conversion Techniques for High Density Power Supplies", Ph. D. Thesis, Massachusetts Institute of Technology, May 1992.

[16] *Power Factor Correction with the UC3854*, Application Note, Unitrode Integrated Circuits, 1991.

[17] *EV80C196KC Microcontroller Evaluation Board User's Manual*, Intel Corporation, 1992.