A Digitally Controlled Amplifier With Ripple Cancellation

Deron K. Jackson, *Member, IEEE,* and Steven B. Leeb, *Senior Member, IEEE*

***Abstract*—This paper describes a large-signal linear, multirate digital controller for, among other possible servomechanical applications, charging electric vehicle batteries. This controller permits the power amplifier to track and deliver a desired current trajectory for a wide range of loads while providing a unity-power-factor interface to the electric utility. A computationally inexpensive technique for implementing output ripple cancellation is also described and demonstrated on a prototype converter.**

***Index Terms*—Digital control, multirate control, ripple cancellation.**

I. Introduction

WHERE cost permits or regulations require, conventional amplifiers for servomechanisms often employ a power-factor correcting utility (PFC) interface. Near-unity power factor operation is essential to ensure maximum power delivery capability and to minimize the generation of harmonic currents. In a two-stage servo drive, a bridge inverter may operate from a DC link created by the PFC rectifier [1]. This paper examines an inductively coupled, two-stage power conditioning architecture for all sorts of servomechanical drives, including for application as a battery charger. A schematic of a unidirectional (charge only) architecture is shown in Fig. 1. In fact, a bidirectional supply with two-way, charge and discharge capability is employed for the experiments in this paper [18]. This supply could, for example, provide drive and brake capability for a dc input electric machine. The control techniques developed here for the first PFC stage would also be applicable for controlling the dc link in an ac servo drive.

In contrast to PFC controllers for typical regulation applications, the charging system requires a controller whose stability is verifiably guaranteed over a wide range of operating conditions. Also, for adequate tracking performance, the controller may need to respond swiftly to command changes or load disturbances over this range. This paper describes a multirate digital controller that meets these demands.

In the battery charging application, the full-bridge inverter impresses a high frequency ac signal on the primary of a transformer. The secondary waveform is rectified to provide a dc output voltage for driving the load. This dc–dc stage provides isolation through an inductive coupling or separable transformer, which is considered by some to maximize operator safety and connector life [1]–[6]. The inverter is operated at a fixed frequency and near-unity duty ratio to minimize dissipation in the separable coupling, a significant concern for a practical connector. Control of the load, e.g., charging current, is accomplished by actively varying the output voltage of the PFC rectifier.

The power factor correction stage produces a controlled dc output voltage with a small, twice-line frequency ripple component. If the ripple is not eliminated during the second stage dc/dc conversion, it passes directly to the load. The battery load shown in Fig. 1 will typically include a filter to minimize high, switch-frequency voltage ripple. However, it is often not cost effective to provide filtering to eliminate low, near-utility-frequency ripple. The peak-to-peak amplitude of the voltage ripple at the dc bus might be on the order of 1% of its dc value.

For a resistive load or loads with a "low-pass" character, these small variations may be of little consequence. In a servomotor, this ripple voltage will lead to a ripple current and torque ripple in the machine. A speed servo in an air-handling system may not be particularly sensitive to this ripple. In a sensitive application like wafer handling or a drive system in a quiet submarine, this torque ripple could be unacceptable. In a battery charging application, the load behaves, at least to a simple approximation, as a voltage source with a relatively small series resistance [7]. This series resistance is often so small that even a slight voltage ripple will induce significant current ripple into the battery. Depending on the battery technology, this ripple could lead to excessive, unacceptable peak currents, and even discontinous charging current. Following a discussion of a high-performance, large-signal stable tracking compensator for the PFC stage, this paper presents a practical scheme for minimizing the effects of the dc bus voltage ripple without requiring feedback information from the secondary side of the transformer. All of these techniques are demonstrated with results from a 1500 W prototype.

II. Background

A boost converter as shown in Fig. 2 serves as the PFC rectifier in the battery charger. The input voltage is the rectified ac utility voltage. All voltage and current variables in Fig. 2 refer to quantities averaged over at least one switch period, i.e., switching ripple will be ignored in the following discussion. An inner current loop controls the input or inductor current $i_L(t)$ to follow a desired reference waveform $i_p(t)$ by providing an appropriate pulse-width-modulated switching sequence to the controllable switch. To ensure PFC operation, the reference waveform $i_p(t)$ is a scaled copy of the rectified input voltage waveform. An outer, voltage-loop controller can adjust v_o to

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D. K. Jackson is with Adept Technology, San Jose, CA 95134 USA.

S. B. Leeb is with the Laboratory for Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

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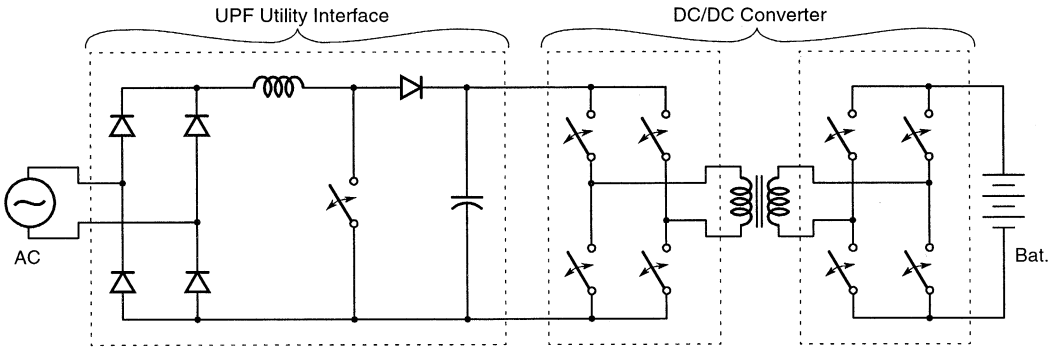

Fig. 1. Circuit topology for an inductively-coupled battery charger (see text).

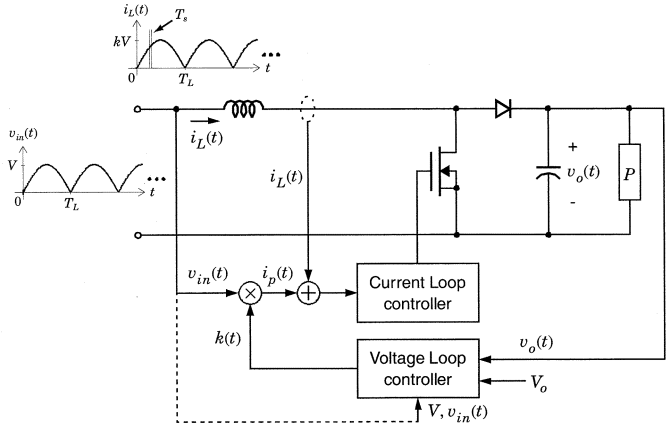

Fig. 2. High-power-factor preregulator.

a desired value by varying the scale factor k used to compute $i_p(t)$. Changing k is tantamount to changing input power.

In [8] and [9], a large-signal linear, "power balance" model of the boost PFC rectifier was derived using Tellegen's theorem [10]. Assuming that the inner current loop works well, the inductor current waveform is a scaled copy of the input voltage waveform, i.e., $i_L(t) = kv_{in}(t)$. Also, to ensure unity-power-factor operation, it is presumed that k and the load power, P, will vary no more frequently than once per rectified line cycle. With these assumptions, the following sampled data model of the boost rectifier may be developed:

$$x[n+1] = x[n] + \frac{T_L V^2}{C}\, k[n] - \frac{2T_L}{C}\, P[n] \qquad (1)$$

where the state variable $x[n]$ denotes the value of the squared output voltage at the beginning of the nth cycle. Similarly, $k[n]$ and $P[n]$ represent the value of the scale factor k and the load power, respectively, during the nth cycle. The variable T_L represents the period of one rectified input line cycle, i.e., $1/T_L =$ 120 Hz. The index n in the sampled data model, (1), increments once every T_L seconds. The sampled data, power balance model of the boost rectifier is illustrated schematically with the use of the z-transform [11] in Fig. 3.

Because this model is not a small-signal approximation, it is especially suitable for use in developing a controller for tracking applications like the battery charger. Because it is a sampled data

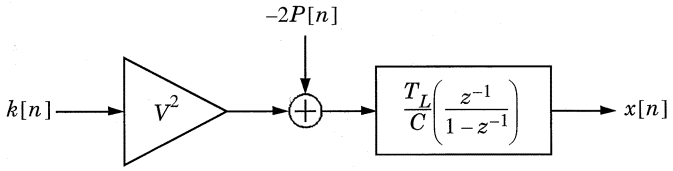

Fig. 3. Boost converter sampled data model.

model, it is a convenient starting point for developing a digital controller. We begin by developing a discrete-time (DT) controller for the squared output voltage, since this is the state variable described by the power balance model. Charging current is controlled by a DT outer loop that computes the reference for the inner voltage loop. The total charging system consists of a multirate cascade of three nested control loops, listed from highest to lowest closed-loop tracking bandwidth: an innermost current loop to control and shape the input current to the boost converter; a voltage loop to control the output bus voltage; and an outermost current control loop to track the desired output charging current profile. In our prototype, the inner current loop is implemented with analog hardware. The outer voltage and current loops are implemented on a digital microcontroller.

III. Voltage Control

In [9], [10] and [12], the voltage loop is stabilized with the discrete-time version of a proportional-integral (*PI*) compensator. We have found, however, that an alternative pole-placement (*PP*) algorithm yields improved performance. This algorithm is outlined below and compared to its *PI* counterpart.

The pole-placement algorithm employs full state feedback which, in principle, allows for arbitrary placement of the closed-loop poles. Formulation of the control loop begins with the control command k. The control command k is chosen as

$$k[n] = k[n-1] + \frac{C}{T_L V^2} \cdot (G_1(X[n] - x[n]) + G_2(X[n] - x[n-1])) \qquad (2)$$

where $X[n]$ is the squared-voltage reference. The constants G_1 and G_2 are feedback gains. The $k[n-1]$ term incorporates the effect of an accumulator directly. Therefore, when the two error terms, $(X[n] - x[n])$ and $(X[n] - x[n-1])$, are both zero, $k[n]$ can be in steady state.

Combining (2) and (1) yields the following state-space description of the closed voltage loop

$$\begin{bmatrix}\sigma_x[n+1]\\ x[n+1]\end{bmatrix}=\begin{bmatrix}0 & 1\\ -(1+G_2) & 2-G_1\end{bmatrix}\begin{bmatrix}\sigma_x[n]\\ x[n]\end{bmatrix}+\begin{bmatrix}0\\ G_1+G_2\end{bmatrix}X[n]+\begin{bmatrix}0\\ \dfrac{-2T_L}{C}\end{bmatrix}(P[n]-P[n-1]). \quad (3)$$

The variable $\sigma_x[n]$ is defined as

$$\sigma_x[n+1]=x[n] \quad (4)$$

and it accounts for the added state from the $x[n-1]$ term in (2). This compensation unfortunately results in a voltage loop that is dependent on the load power $P[n]$. We will see in the next section that the inability to guarantee the voltage-loop dynamics independently of the load would significantly complicate the development of the outer charging current control loop. To make the voltage-loop dynamics independent of load power, the control command in the charger prototype is computed as in (2), but with the addition of a power feedforward term

$$\tilde{k}[n]=\tilde{k}[n-1]+\frac{2}{V^2}(P[n]-P[n-1])+\frac{C}{T_LV^2}\cdot(G_1(X[n]-x[n])+G_2(X[n]-x[n-1])). \quad (5)$$

In a charging circuit, both load terminal voltage and terminal current will be available, and computing load power requires little additional expense or computational effort. Substituting (5) into (1) yields a new second-order, large-signal linear model for the actively controlled boost converter

$$\begin{bmatrix}\sigma_x[n+1]\\ x[n+1]\end{bmatrix}=\begin{bmatrix}0 & 1\\ -(1+G_2) & 2-G_1\end{bmatrix}\begin{bmatrix}\sigma_x[n]\\ x[n]\end{bmatrix}+\begin{bmatrix}0\\ G_1+G_2\end{bmatrix}X[n]. \quad (6)$$

A closed-loop DT transfer function from $X[n]$ to $x[n]$ is obtained using the z-transform

$$\overline{H}_{PP}(z)=\frac{(G_1+G_2)z}{z^2+(G_1-2)z+(G_2+1)}. \quad (7)$$

The system poles are

$$z_1,\, z_2=\frac{(2-G_1)\pm\sqrt{G_1^2-4(G_1+G_2)}}{2} \quad (8)$$

and there is a finite zero located at $z=0$. The complete system with the voltage loop closed is shown schematically in Fig. 4. Selecting gains G_1 and G_2 so that these poles have magnitude less than one results in a stable system. Once gains have been calculated to yield stable closed-loop pole locations, the system will remain stable for practically any load because (6) is independent of load power. The stable voltage loop will converge to any constant reference given sufficient time. This guaranteed convergence substantially simplifies the construction of the charging current control loop.

In [12], a *PI* controller was used to stabilize the voltage loop. This controller was formed using the following control command

$$\tilde{k}[n]=\frac{C}{T_LV^2}(G_1(X[n]-x[n])+G_2\sigma_v[n])+\frac{2}{V^2}P[n] \quad (9)$$

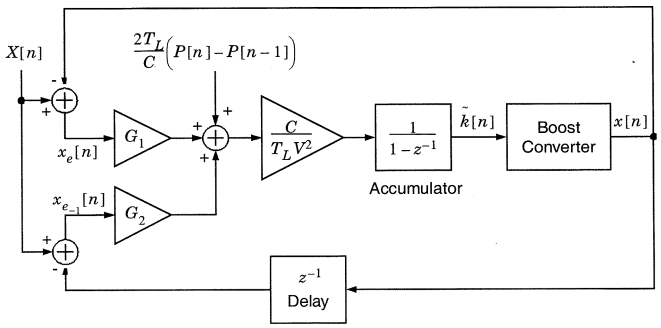

Fig. 4. Voltage loop.

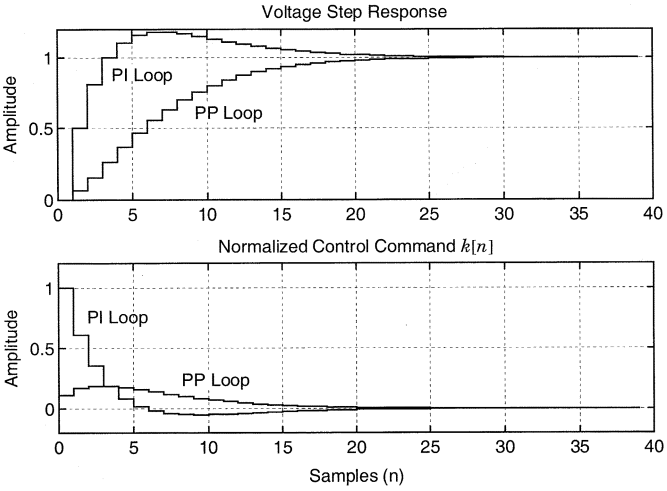

Fig. 5. Simulated voltage-loop responses.

where $\sigma_v[n]$ is a voltage accumulator defined as

$$\sigma_v[n+1]=\sigma_v[n]+(X[n]-x[n]). \quad (10)$$

The resulting closed-loop DT state-space and transfer function descriptions are given in (11) and (12) below

$$\begin{bmatrix}\sigma_v[n+1]\\ x[n+1]\end{bmatrix}=\begin{bmatrix}1 & -1\\ G_2 & 1-G_1\end{bmatrix}\begin{bmatrix}\sigma_v[n]\\ x[n]\end{bmatrix}+\begin{bmatrix}0\\ G_1\end{bmatrix}X[n] \quad (11)$$

$$\overline{H}_{PI}(z)=\frac{G_1\left(z+\frac{(G_2-G_1)}{G_1}\right)}{z^2+(G_1-2)z+(1+G_2-G_1)}. \quad (12)$$

The closed-loop poles are

$$z_1,\, z_2=\frac{(2-G_1)\pm\sqrt{G_1^2-4G_2}}{2} \quad (13)$$

and a finite zero exists at $-((G_2-G_1)/G_1)$.

The relative performance of the two voltage loops can be judged by comparing their step responses. Values for G_1 and G_2 were calculated for each system that place the closed-loop poles at $z_1=z_2=0.75$. The unit-step responses of the resulting systems are plotted in Fig. 5. Fig. 5 demonstrates two clear advantages of the *PP* loop in contrast to its *PI* counterpart. First, the response of the *PP* loop has zero overshoot versus about 18% for the *PI* loop. Voltage overshoot is undesirable in this application because it leads to a comparable current overshoot which may complicate design of the charging current loop. Second, the *PP* loop achieves settling times equal to the *PI* loop with a much

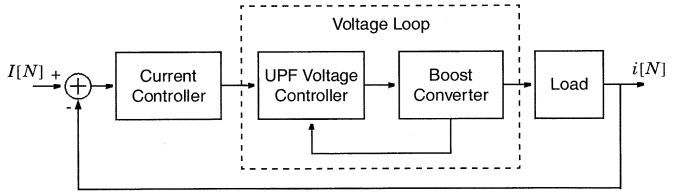

Fig. 6. Current loop block diagram.

lower peak control command. Fig. 5 shows the peak value of $k[n]$ for the *PP* loop to be only 19% of the peak *PI* command. This is critical to avoid input command (and hence input power) saturation.

IV. Charging Current Control

The outermost control loop in the battery charger ensures that the output charging current tracks a current reference. This loop creates a desired charging current by computing an appropriate voltage command reference for the voltage loop to follow. The complete system is illustrated schematically in Fig. 6. The dashed voltage-loop box in Fig. 6 represents the boost converter and voltage-loop control circuitry shown in Fig. 4.

The load dynamics for a wide range of loads (e.g., battery types) are easily represented in the charging current loop by a driving point admittance. Given the availability of a function relating applied terminal voltage to load current, a natural and convenient formulation for the current loop is to assume that load or charging current will be sensed, and a desired terminal voltage will be created by the action of the current loop computation and the voltage amplifier (boost converter and voltage loop). However, it is not the output voltage but the squared output voltage that is the state controlled by the voltage loop. This complicates the formulation of a complete state-space description for the full three-loop system.

The guaranteed convergence of the voltage loop, independent of load dynamics, facilitates simplifying assumptions. Recall that the DT voltage loop operates with sample step index n. The current loop will be designed to operate with sample index $N = Qn$ where Q is a positive integer. That is, every step of the DT current loop corresponds to Q steps of the voltage loop. This *multirate* arrangement makes it possible to model the voltage-loop dynamics, from the standpoint of the outer current loop, in any of several simplified ways. Two approaches will be considered here: a delay model of the voltage loop appropriate for resistive loads, and a zero-order-hold model appropriate for loads representable as combinations of linear, time invariant (LTI) circuit elements and independent sources.

A. Delay Model

One possibility, employed in our prototype with a resistive load, is to select Q and the closed-loop pole locations of the voltage loop so that the output bus voltage will converge to a new reference X in a single step of the current-loop index N. That is, the current loop computes a voltage reference at time N. This reference is squared and supplied as the command reference to the inner voltage loop. With the proper choice of Q and the voltage-loop poles, the output bus voltage will have converged to the reference command supplied by the current loop by time $N+1$. Under these assumptions, the voltage loop may be modeled as a unit delay on the slow, current-loop time scale. This arrangement is illustrated in Fig. 7. Signals in the figure are indexed by "n" or "N," depending on whether they are part of the fast voltage loop or slow current loop, respectively.

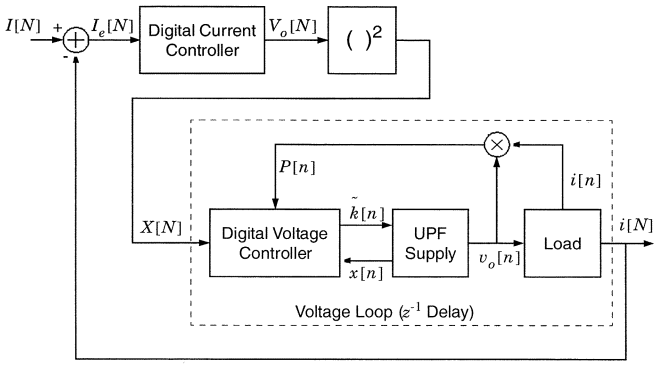

Fig. 7. Current control system.

With a resistive load, and modeling the voltage loop as a unit delay on the time scale of the current loop, the charging current loop may be stabilized most simply with a DT pole-placement compensator similar to that used in the voltage loop. The reference voltage V_o is defined as

$$V_o[N] = V_o[N-1] + G_3(I[N] - i[N]) \tag{14}$$

where G_3 is a constant gain.

Modeling the action of the voltage loop as a unit delay on the time scale of the current loop, the output voltage applied to the load is equivalent to the delayed command signal, i.e.,

$$V[N+1] = V_o[N] = V_o[N-1] + G_3(I[N] - i[N]). \tag{15}$$

With a resistive load, a state equation for i can be written using (15) and Ohm's law

$$i[N+1] = i[N] + \frac{G_3}{R}(I[N] - i[N]). \tag{16}$$

Application of the z-transform to (16) yields a transfer function from $I[N]$ to $i[N]$ for the charging current loop

$$\overline{H}_I(z) = \frac{G_3/R}{z + G_3/R - 1}. \tag{17}$$

In the z-plane, the closed-loop system has a single pole at

$$z = \frac{G_3}{R} - 1. \tag{18}$$

The stability and transient characteristics of the current loop may be adjusted by selecting an appropriate gain G_3.

B. Zero-Order-Hold Model

For a resistive load, load terminal voltage is proportionally related to load terminal current. This made it easy to step from (15) to (16) while developing the current loop in the previous section. For a more complicated LTI load model, the delay model of the voltage loop may not be as easy to apply. In this case, we can exploit the guaranteed, large-signal transient characteristics of the voltage loop to develop other useful control models and approaches.

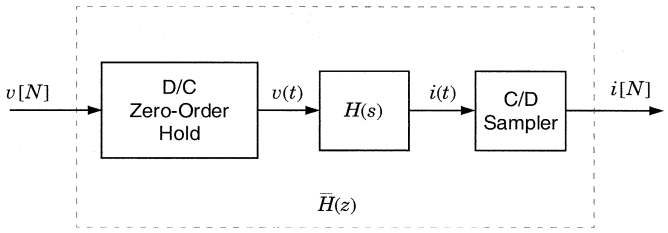

Fig. 8. Driving point characteristic.

Once again, the DT current loop steps with index $N = Qn$ where n is the index of the voltage loop and Q is a positive integer. We now add the additional constraint that the voltage loop, given a new reference, will drive the output voltage to this reference in *many* fewer than Q steps of the index n. This condition is ensured through judicious selection of Q and the closed-loop pole locations of the voltage loop. Given these conditions, the voltage loop may be modeled as a zero-order-hold (ZOH) on the time scale of the outer current loop.

For an LTI load, the load terminal current can be related to the applied terminal voltage by an expression for the driving point admittance of the load, represented henceforth by the CT Laplace transform $H(s)$.[1] Assuming that Q steps of the index n are substantially longer than the time required for the voltage loop to settle to a new command reference, the CT voltage applied to the load will appear "pulse-like" throughout one step of the index N, i.e., the operation of the voltage loop will closely approximate that of a zero-order-hold. The current-loop controller will provide a command reference to the voltage loop, and will also sample the load current, on each step of the current-loop index N. Fig. 8 schematically illustrates this arrangement. The zero-order-hold block represents the boost converter with voltage loop.

The ZOH and sampling operations in Fig. 8 model the interface between the CT driving point characteristic of the load and the DT current loop [14]. The DT driving point admittance can be described as a z-transform $\overline{H}(z)$. The admittance $\overline{H}(z)$ is related to $H(s)$ by a *step-invariant transformation* [11]. Tables relating common functions $H(s)$ to their "pulse" transfer functions $\overline{H}(z)$ may be found in many texts. (See [14], for example.)

In general, complex load models will add state variables to the overall current-loop state-space description. In such cases, the current-loop state equations will generally be more complicated than (16). Gains might have to be adapted and/or different compensation schemes might be needed for different loads. Fortunately, the digital implementation of the current-loop controller accommodates these changes.

The approach outlined in this section requires that the voltage loop converge to its reference in many fewer than Q steps of the index n. This limits the performance of the current loop. In principle, however, the voltage loop can be made *deadbeat* [10], i.e., the voltage loop can converge in two steps of the index n, or one electrical input line cycle. This, of course, is subject to the limitations imposed by the maximum current command that can be followed by the inner current loop and by the discharge rate made possible by the loading conditions. Nevertheless, the achievable, practical performance appears to be more than adequate for high-performance battery charging and servomechanical applications [19].

[1]Many loads of interest can be modeled as circuits consisting of LTI elements, or as switched circuits that are piecewise LTI. Most batteries, on the other hand, tend to exhibit nonlinear driving point current/voltage characteristics. It is often possible, however, to develop LTI or piecewise LTI battery models; see [13] for example.

V. Crossing the Isolation Barrier

A simplified sketch of the full-bridge converter topology is shown in Fig. 9. Only the components necessary for unidirectional forward power flow are illustrated, although the 1500 W prototype is capable of bidirectional operation for charging and discharging or conditioning operations. MOSFET's Q_1 through Q_4 form a full-bridge inverter. The inverter drives the primary of the inductive coupling through a large dc blocking capacitor C_{bl}. The four switches are gated at a frequency of 100 kHz using a phase-shifted pulse-width modulation pattern [21], [22].

In principle, pulse-width modulation (PWM) control could be used to vary the output voltage from its maximum all the way down to zero. However, the conversion efficiency decreases as the PWM duty ratio is lowered from unity. The decrease in efficiency is caused by an increase in the RMS switch currents relative to the output current. In the prototype, therefore, duty-ratio control is used only to cancel the 120-Hz small-signal voltage ripple. The nominal duty ratio remains within a few percent of unity. Large signal voltage control is accomplished by varying the PFC bus voltage at the input to the inverter.

Pulse-width modulation of the voltage V_{AB} seen across the primary of the inductive coupling is controlled by adjusting the phase shift between the gate drives applied to each leg of the converter. Zero phase shift yields an effective duty ratio of zero, while a phase shift of π yields a unity–duty ratio. By adjusting the phase shift for PWM control, active ripple cancellation is possible.

VI. Feedforward Ripple Cancellation

The steady-state bus voltage at the input to the dc/dc stage can be described as

$$v_{bst}(t) = V_{bst} + r(t) \tag{19}$$

where V_{bst} is the nominal or dc level and $r(t)$ is the 120-Hz ripple component. Under PWM control the output voltage of the dc/dc stage is linearly related to the duty-ratio command by

$$v_o(t) = d(t)Nv_{bst}(t) = d(t)N(V_{bst} + r(t)) \tag{20}$$

where $d(t)$ is the duty ratio and N is the effective transformer turns ratio. Voltage droop caused by the coupling leakage inductance does not affect the ripple cancellation. Therefore, it has been ignored to simplify the discussion. Exact ripple cancellation requires a duty ratio of

$$d(t) = \frac{DV_{bst}}{V_{bst} + r(t)} \tag{21}$$

where D is a constant slightly less than one. As desired, the expression for the steady-state output voltage becomes a constant $v_o(t) = DNV_{bst}$.

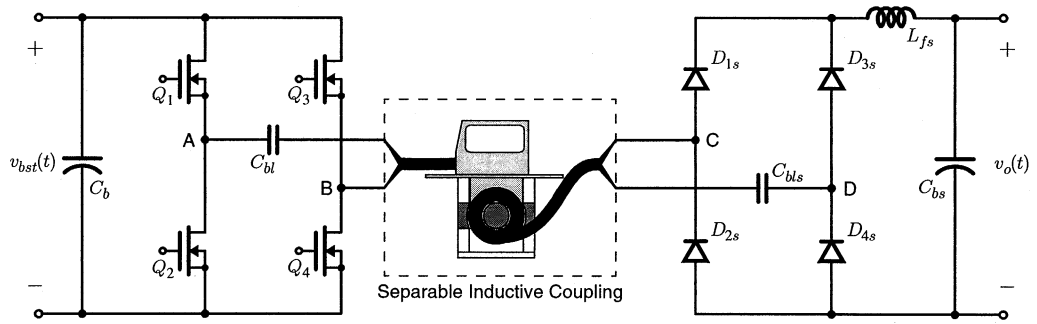

Fig. 9. Simplified schematic of the full-bridge prototype.

The nonlinear expression in (21) would require an expensive analog implementation or a digital solution using a time-varying division. A linear approximation of the expression in (21) can be found by taking the first term in its binomial series expansion, as

$$d(t) = D - \frac{D}{V_{bst}}\, r(t). \tag{22}$$

The linear approximation is simpler to implement and yields nearly ideal performance. The resulting output voltage is found by substituting (22) into (20)

$$v_o(t) = DNV_{bst} - \frac{DN}{V_{bst}}\, r(t)^2. \tag{23}$$

Although the expression in (23) is not a constant, the relative amplitude of the ac component is greatly reduced. Significant reduction in the ac component requires only that V_{bst} is much greater than the amplitude of $r(t)$, and this condition is automatically satisfied by a well-designed PFC stage. Thus, if the amplitude of the input voltage ripple is 1%, the output ripple amplitude should be reduced by over 99%. The amplitude of the remaining ripple is often insignificant.

VII. Experimental Results

The 1500 W boost converter used in the prototype utilized an interleaved design. The converter consists of eight identical stages, which together feed an output capacitance of approximately 1410 μF. For these preliminary tests, a 143.8 Ω resistor was used as a load. Each boost stage is composed of a 540 μH inductor, a Motorola MTW14N50E MOSFET, and a Motorola MUR 1560 diode. The switching frequency for each stage is 25 kHz, however, the individual clocks are shifted in phase from each other by 1/8th of the 25 kHz period. This results in a net current ripple frequency of 200 kHz. This type of converter has several advantages over a conventional, noninterleaved, design and a thorough analysis of this converter can be found in [15].

The inner current loop operates using averaged current mode control similar to previous designs [9], [12]. However, this inner current loop was implemented with discrete analog circuitry since a single chip PFC controller such as the Unitrode UC3854 does not currently exist for interleaved converters [16]. Both the digital voltage and charging current controllers were implemented on a single Intel 80C196KC microcontroller (with plenty of spare processing power). Code for the microcontroller

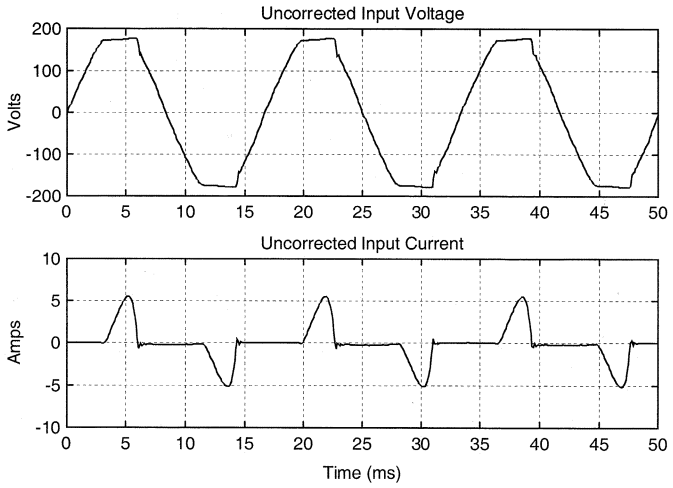

Fig. 10. Input current and voltage without PFC.

was developed in the C programming language using a cross-compiler from Intel [17].

The operation of the voltage-loop controller was synchronized to the period of the rectified line, T_L, by an external interrupt generated from the ac line. For tests with the resistive load, the delay model of the voltage loop was used to develop the charging current controller. The charging current-loop index N in the prototype increments once for every 15 steps of the voltage-loop index n. The gain G_3 was selected to locate the closed-loop pole at $z = 0.20$.

Fig. 10 shows the steady-state input current and voltage before any control action commences. The input current and voltage are measured at the ac line before the full-wave rectifier that precedes the boost converter. Initially, all three control loops are inactive, and the MOSFETs in the boost converter are held in the off state. The input current exhibits the "spikey" shape that typically occurs when a sinusoidal voltage is rectified and used to charge a capacitor. When the output voltage stabilizes, the inner current loop is activated. The input current assumes the shape and phase of the input voltage waveform, indicating the inner current loop is functioning properly. The 80C196KC performs a "soft start" by sending open-loop scale factor commands to the inner current loop, causing the input current to rise gently until the output voltage/current is close to a desired initial operating point. At this time, the processor initializes the voltage and charging current loops in the microprocessor, and closed-loop control of the output current begins.

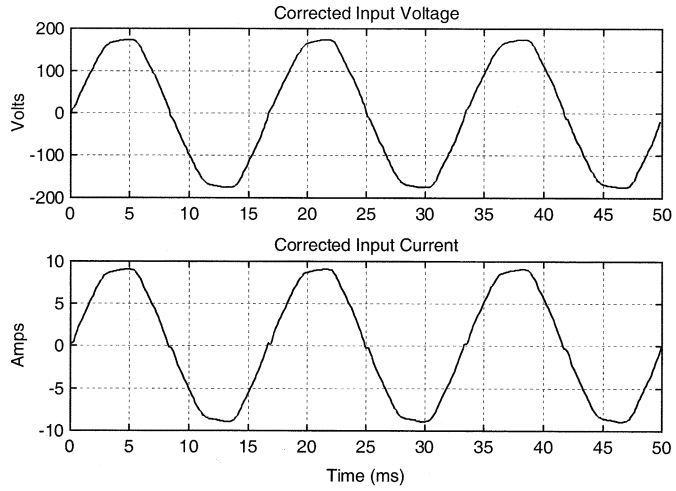

Fig. 11. Input current and voltage with PFC.

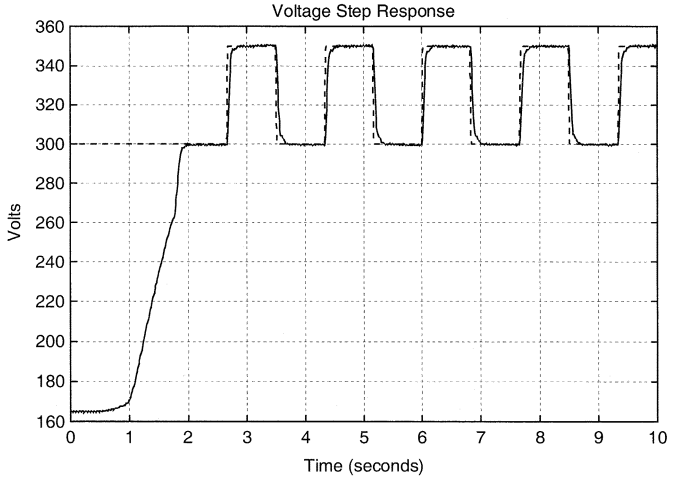

Fig. 12. Step response of the voltage loop.

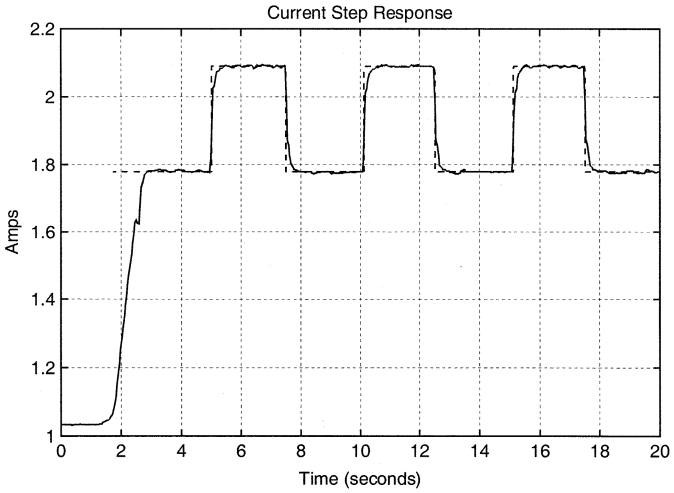

Fig. 13. Step response of the charging current loop.

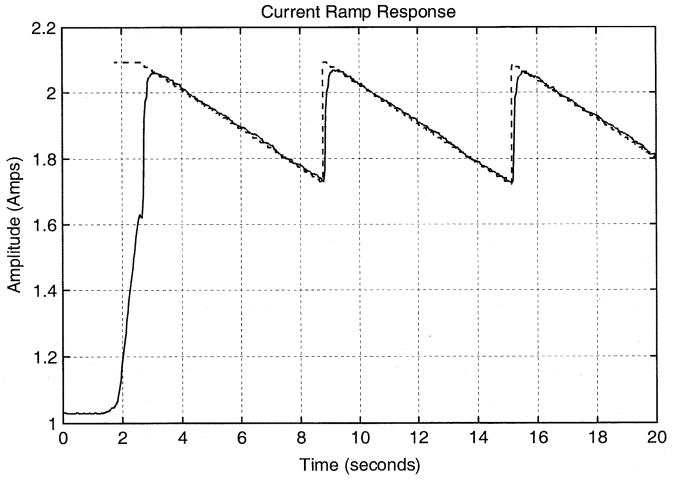

Fig. 14. Ramp response of the charging current loop.

Fig. 11 shows the steady-state input current and voltage after the control loops have been activated.

The *PP* voltage loop was implemented in our prototype charging system. The closed-loop poles were set at $z_1 = z_2 = 0.75$. The voltage-loop command was programmed to step periodically between an output voltage of 300 and 350 V. The experimental results are plotted in Fig. 12. The first two seconds in the figure show the soft-start mechanism of the converter after which closed-loop command following begins. The dashed line in Fig. 12 represents the voltage command.

Figs. 13 and 14 show the output current during two different tests with the converter. Each figure shows a charging current command reference (dotted/dashed line) and the experimental curve (solid line) from the actual hardware prototype. In Fig. 13 the current command reference is a square waveform, and in Fig. 14 the command reference is a sawtooth waveform. The soft-start procedure dominates the first approximately 3 s of each output current profile. After the soft start, when the current- and voltage-loop controllers engage, the output current closely follows the command reference.

This need for active ripple cancellation is exemplified by the experimental waveforms in Fig. 15. The experimental data in the top trace was recorded using the prototype hardware with the ripple cancellation circuitry disabled. The waveforms show a 25% (peak-to-peak) current ripple while charging a 120-V lead–acid battery pack with a nominal charging current of 2.3 A. The corresponding voltage ripple during this experiment is approximately 0.5% (peak-to-peak). Although the voltage ripple is relatively small, the current ripple is significant. As the nominal charge current is increased, the current ripple can easily exceed 100%, resulting in a discontinuous battery current.

In practice, the feedforward cancellation scheme just described was implemented as follows. A first-order high-pass filter, with a corner frequency of approximately 20 Hz [sufficiently below 120 Hz to avoid affecting $r(t)$], is used to separate $r(t)$ from a measurement of $v_{bst}(t)$. The measured ripple component $r(t)$ is scaled by D/V_{bst} and subtracted from a constant duty-ratio command D. The required perturbation in $d(t)$ is small, so D is selected as close to unity as possible. Setting D near unity ensures that there is little or no conduction loss penalty from the freewheeling current in the dc/dc stage.

Experimental waveforms demonstrating the effectiveness of the ripple cancellation technique are shown in Fig. 15. The expanded views demonstrate a measured reduction in current

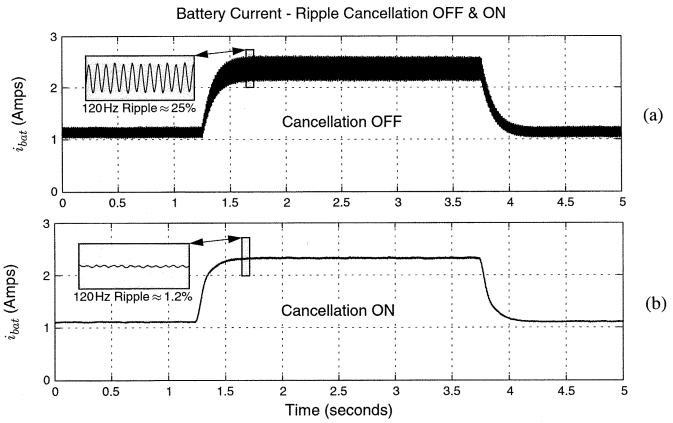

Fig. 15. Experimental waveforms showing the effect of ripple cancellation.

ripple from 25% to 1.2%. Also, note that the transient step changes in the output current have essentially no affect on the ripple cancellation. The remaining ripple in Fig. 15 can be attributed to the linear approximation of the optimum $d(t)$ and to a slight phase shift from the filtered measurement of $r(t)$, which is used to generate the feedforward command.

VIII. Conclusion

The sample experiments reviewed in the previous section are representative of many similar laboratory tests. They indicate that the voltage-loop controller, with load power feedforward as described in (5), operates as anticipated. The voltage-loop dynamics can therefore be guaranteed with minor restrictions on load behavior, permitting us to approximate the voltage-loop behavior in a number of different ways from the standpoint of the outer charging current loop. The experiments presented here directly demonstrate the performance of the charging current loop and its close agreement with predicted results.

The pole placements for the charging current and voltage loops in the prototype were not aggressive, i.e., the transient response could be improved, if necessary. We are working to test the performance of the controller with different, more challenging loads and load models. Also, we are engaged in studying the robustness of the multirate cascade controller in the face of load model errors or uncertainties, which may be of special concern in a field version of a battery charger, where significant deviations or drift in battery parameters may occur. The digital implementation of the charging current and voltage loops makes it easy to consider adaptive or scheduled control compensation for different loads in the field [19]. The favorable performance of the *PP* compensator makes it a likely candidate for use in many different digital control applications in power electronics [20].

Discontinuous or high-ripple charging current may increase the temperature and pressure of a battery during charge. Future battery chemistries and high-rate charge profiles may require that such ripple is eliminated. The PWM voltage control capability of the phase-shifted full-bridge dc/dc converter makes it possible to provide active ripple cancellation. The prototype full-bridge converter uses a feedforward control technique to accomplish this.

We expect that this cancellation technique could be extended to half-bridge configurations using the asymmetrical half-bridge control technique, discussed in [23]. However, with this control approach, the output voltage is nonlinearly related to the switch duty ratio. Hence, the ripple cancellation might be more complicated to implement in the half-bridge configuration.

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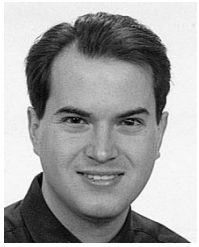

Deron K. Jackson (S'96–M'98) received the B.S. degree in electrical engineering from the University of California, Davis, in 1991 and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, in 1994 and 1998, respectively.

He is a Senior Hardware Engineer with Adept Technology, San Jose, CA. His research interests are in the areas of power electronics and control.

Steven B. Leeb (S'89–M'93–SM'01) received the S.B., S.M., E.E., and Ph.D. degrees from the Massachusetts Institute of Technology (MIT), Cambridge, in 1987, 1989, 1990, and 1993, respectively.

He has been a member of the MIT faculty in the Department of Electrical Engineering and Computer Science since 1993. He currently serves as an Associate Professor in the Laboratory for Electromagnetic and Electronic Systems. He is concerned with the design, analysis, development, and maintenance processes for all kinds of machinery with electrical actuators, sensors, or power-electronic drives.

Dr. Leeb is a member of the IEEE Power Electronics, Control Systems, Power Engineering, and Signal Processing Societies. He is a Fellow of M.I.T.'s Leader's for Manufacturing Program and a member of Tau Beta Pi and Eta Kappa Nu.