Capacitor-Less Photovoltaic Cell-Level Power Balancing using Diffusion Charge Redistribution

Arthur H. Chang, *Student Member, IEEE*, Al-Thaddeus Avestruz, *Member, IEEE*, and Steven B. Leeb, *Fellow, IEEE*

***Abstract*—This paper presents a new strategy, diffusion charge redistribution (DCR), for balancing power among photovoltaic cells to increase energy extraction and to improve maximum power-point tracking (MPPT) efficiency under partial shading conditions. With DCR, testing and binning during cell manufacturing can be eliminated and significant cost savings can be achieved during production. The proposed technique performs power balancing by taking advantage of the intrinsic diffusion capacitance of the solar cells and requires no external passive components for energy storage, thereby minimizing power electronics cost and complexity. Strings balanced by this technique exhibit power versus current curves that are convex, which also greatly reduces the cost and complexity of the required MPPT algorithm.**

***Index Terms*—Distributed power converters, maximum power point tracking (MPPT), PV energy optimization, solar cells, solar energy, switched capacitor networks, switched circuits.**

I. Introduction

PHOTOVOLTAIC (PV) power modules are traditionally configured as a string of solar cells [20]. In this series-connected configuration, the overall string current is limited by the available current of the lowest performing solar cell in the string. Therefore, external operating conditions such as partial shading and dirt accumulation can severely limit the available power from the string, even if only a few cells are affected out of a large string [1]–[8].

Bypass diodes in parallel with substrings can mitigate this problem. This approach enables the higher performing cells to output higher currents, bypassing lower performing substrings altogether, potentially extracting more power from the string. However, any possible power generation from the lower performing cells is completely forgone and additional losses are also incurred from the bypass diodes. Furthermore, this results in an output power characteristic curve that is nonconvex, which complicates maximum power-point tracking (MPPT) algorithms [2], [4].

Modular architectures such as cascaded dc–dc converters with a central inverter, microinverters, and their submodule variants, have been proposed to allow local MPPT through distributed control [7]–[9]. However, their operation requires the processing of the full power from each PV element, which is a major disadvantage in terms of insertion loss. In addition, it is impractical to scale these approaches down to the cell level, as per-cell inductors and capacitor banks may be required.

Manuscript received April 8, 2014; revised July 2, 2014; accepted July 6, 2014. Date of publication July 17, 2014; date of current version October 7, 2014. This work was supported by the Grainger Foundation and the Kuwait-MIT Program. Recommended for publication by Associate Editor B. Lehman.

The authors are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: arthurhc@mit.edu; avestruz@mit.edu; sbleeb@mit.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2340403

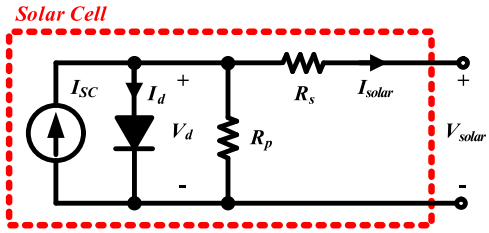


Fig. 1. Commonly used single diode solar cell model.

Recently, there has been a push toward differential power processing (DPP) to balance mismatches in a PV string [1]–[6]. By only processing the mismatch power instead of the full power, significant reduction in power loss due to conversion efficiency and in power electronics size can be achieved, and many different architectures based on this principle have been proposed [1]–[6]. Most of these approaches also rely on the availability of external energy storage elements. For example, the submodule integrated converter in [1] employs flyback converters, which require a discrete transformer per PV element as energy storage. In the PV-to-PV differential architecture proposed in [4] and [5], buck–boost converters with external inductors are used between adjacent PV elements. Lastly, discrete capacitors are needed in parallel with each PV submodule and in between adjacent PV submodules in the resonant switched-capacitor converter proposed in [2] and [3].

This paper explores the concept of DPP applied at cell level while making the tradeoff of eliminating the requirement of external passive component for intermediate energy storage. The proposed technique makes use of the intrinsic diffusion capacitance of the solar cells as the main energy storage element, at the cost of processing part of the common-mode generated power. This technique is termed diffusion charge redistribution (DCR). Theoretical background for quantifying the solar cell diffusion capacitance is presented along with experimental solar cell characterization results in Section II. Analytical derivations of the insertion loss from adopting a ladder DCR string structures are detailed in Section III. Circuit-level implementation of the experimental prototype is detailed in Section IV, and the experimental measurement of the proposed ladder DCR string is presented in Section V.

II. PV Cell Diffusion Capacitance

The commonly used single-diode equivalent circuit model of PV cells proposed in previous studies is shown in Fig. 1 [21]–[23]. The *I*–*V* characteristic of the equivalent solar cell

model can be expressed as

$$I_{\text{solar}} = I_{\text{SC}} - I_d - \frac{V_d}{R_p}. \tag{1}$$

However, the model in Fig. 1 does not completely capture the dynamics of a solar cell. There is a significant amount of diode capacitance associated with the cell, which is often ignored as a parasitic element when MPPT is considered. The complete equivalent circuit model with a shunt diode capacitance is illustrated in Fig. 2(a).

The capacitance of a PV device is equal to the sum of the diffusion and the depletion layer capacitance. Since the intended operating solar cell voltage is near the maximum power voltage (V_{mp}), the diffusion capacitance effect dominates and the depletion layer capacitance can be neglected [10]. Diffusion capacitance is the capacitance due to the gradient in charge density inside the cells, and is known to have an exponential dependence on the solar cell voltage, or a linear dependence on the solar cell diode current [10]–[13]. Specifically, the diffusion capacitance C_d can be expressed as

$$\begin{aligned} C_d &= \frac{\tau_F}{V_T} \cdot I_0 \cdot \exp\left(\frac{V_d}{\eta \cdot V_T}\right) = \frac{\tau_F}{V_T} \cdot (I_0 + I_d) \\ &= C_0 + \frac{\tau_F}{V_T} \cdot I_d \end{aligned} \tag{2}$$

where V_d is the solar cell diode voltage, I_d is the solar cell diode current, V_T is the thermal voltage, and η is the diode factor. Moreover, I_0 is the dark saturation current of the cell due to diffusion of the minority carriers in the junction, and C_0 is the dark diffusion capacitance. The time constant can be defined as

$$\tau_F^{-1} = \tau^{-1} + \tau_B^{-1} \tag{3}$$

where τ is the minority carrier lifetime and τ_B is the transit time of the carrier across the diode. If the solar cell base thickness is greater than the minority carrier diffusion length, τ_F can simply be approximated as τ. In general, solar cells made from materials with longer minority carrier lifetimes are more efficient because the light-generated minority carriers persist for a longer time before recombining [24].

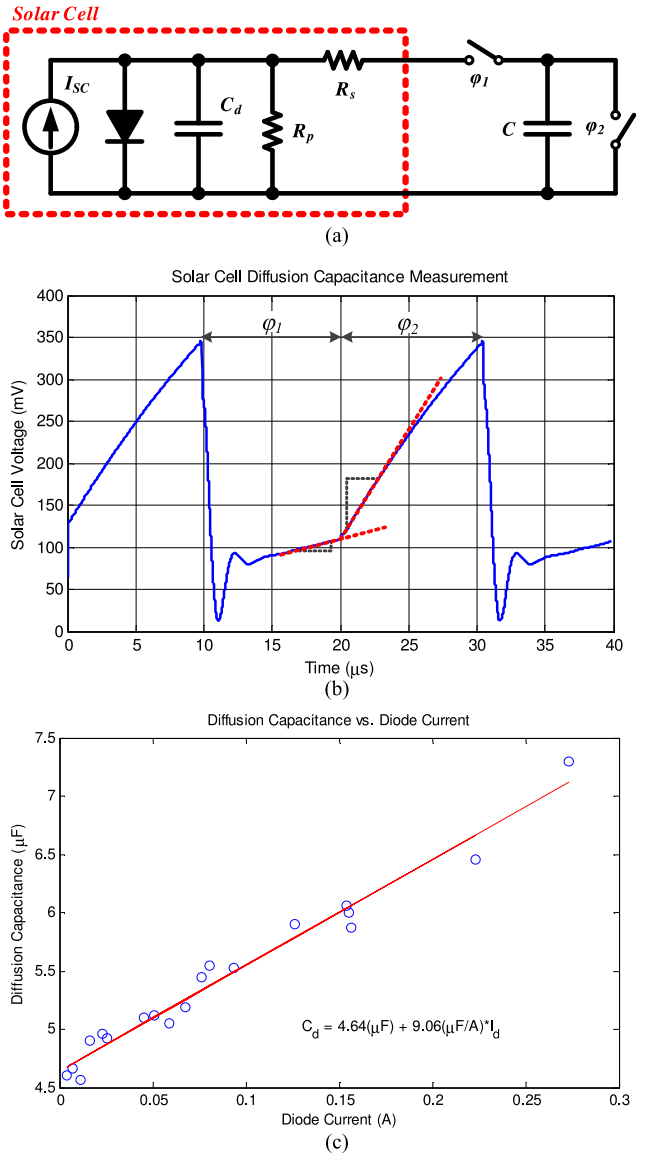


Fig. 2. Solar cell capacitance measurement results: (a) characterization switching circuit implementation, (b) switching waveform, and (c) capacitance versus diode current.

A. Solar Cell Diffusion Capacitance Characterization

Previous works have revealed that solar cells can exhibit diffusion capacitance in the range of microfarads to hundreds of microfarads near the maximum power point voltage [10], [11]. Comparing, for example, to the energy storage capacitance of seven 1 μF capacitors used in the resonant switched-capacitor converter in [2], the solar cell itself possesses a sufficient amount of capacitance and offers a great opportunity to drastically limit the number of external passive components. External energy storage capacitors are required in the case of the resonant switched-capacitor converter in [2] because power balancing is applied at the submodule string level, and the effective capacitance of a submodule string may not be adequate as it is a series combination of a large number of diffusion capacitors.

Published measurements of cell diffusion capacitance are typically performed by applying a bias voltage across the solar cells, which may not accurately represent the effect of diffusion capacitance in the context of a switched-capacitor converter. Therefore, the switching circuit shown in Fig. 2(a) is used here to characterize a commercially available monocrystalline solar cell (P-Maxx-2500 mA) as an example. The cell measures 15.6 cm $\times$ 6 cm and has an open-circuit voltage of 0.55 V and a short-circuit current of 2.5 A under maximum lighting conditions. The solar cell capacitance is measured ratiometrically by comparing the charging slopes during the two different phases of operation. The measurement was performed with a switching frequency of 50 kHz and repeated over a set of known external capacitances between 10 and 30 μF. The corresponding waveforms and the slopes are illustrated in Fig. 2(b), and the measured capacitance showing a linear relationship to the solar cell diode current is shown in Fig. 2(c).

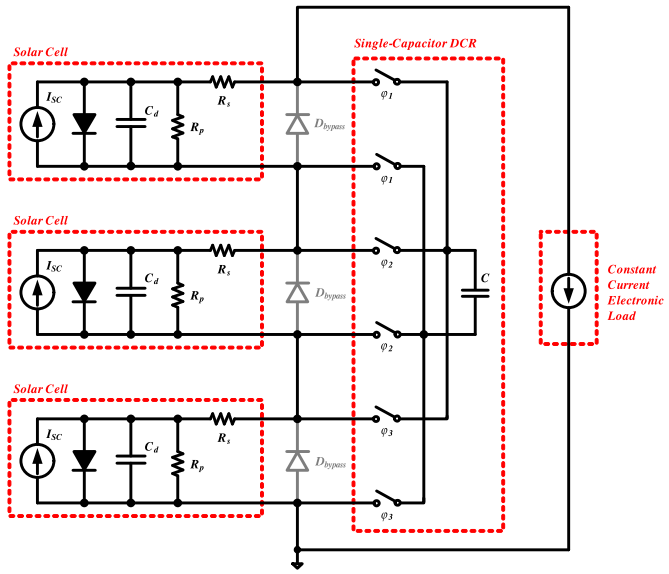


Fig. 3. Single-capacitor DCR validation setup.

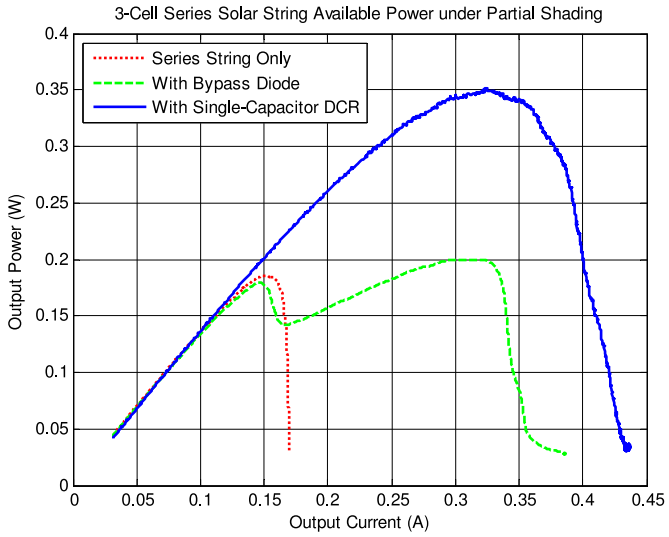


Fig. 4. Measured output power versus output current with and without single-capacitor DCR.

The measured solar cell has a worst-case, i.e., dark, capacitance of 4.64 μF, which matches very well with the measurement result for monocrystalline solar cells presented in [14]. This minimum capacitance will prove sufficient for DCR power balancing. The relationship between the available capacitance and power conversion loss will be discussed and quantified in Section III. Note that the solar cell diode current is roughly equal to the difference between the short-circuit current and the extracted current. With the typical maximum power current (I_{mp}) being approximately 80%–95% of the short-circuit current [1], [7], the diode current is 5%–20% of the short-circuit current at a maximum power point, assuming negligible current through the shunt resistance. Hence, the effective diffusion capacitance for this example cell during normal operation can be as high as 6–9 μF.

B. Single-Capacitor DCR

To demonstrate the utility of the solar cell diffusion capacitance as an energy handling component in a power converter, an initial DCR prototype was constructed with a single capacitor. Results from this experiment will lead to a DCR architecture with no external capacitors. The block diagram of this first experimental setup is illustrated in Fig. 3. The prototype consisted of three monocrystalline solar cells, six IRF9910 MOSFET switches, and a single flying capacitor.

The flying capacitor is connected to each cell sequentially to transfer the imbalance of power among the cells. Since there is no capacitor in parallel with the solar cells to serve as intermediate energy storage when the flying capacitor is disconnected from a cell, the solar cells must therefore rely on their own diffusion capacitance to buffer the different between their respective generated power and extracted power.

By having a single external energy storage element, it can be shown that DPP is preserved, and that insertion loss is insignificant. That is, if the cells are well matched and experience the same irradiance, the cell voltages at maximum power should be identical, resulting in nearly zero net current flow into the flying capacitor and therefore zero loss.

To evaluate the efficacy of the diffusion capacitances in the context of power balancing, a partial shading condition was imposed by covering half of the top cell. In the experiment, the flying capacitor is switched at approximately 300 kHz with a 33% duty cycle for each phase. The output current is swept linearly on an HP 6063B dc electronic load at 1 A/s and the output voltage and current are measured and recorded. The output power versus output current curve for a series string, a series string with bypass diodes, and a series string with single-capacitor DCR are shown in Fig. 4.

Under partial shading condition, the series string current is limited by the weakest link, and therefore the extracted power is reduced dramatically. With bypass diode in place, the system can extract additional power from the unshaded cells while bypassing the shaded one; the resulting nonconvex output power to current characteristic curve is also illustrated in Fig. 4. Finally, the diffusion capacitances are shown to be very effective in power balancing, extracting significantly more power compared to the series string and the bypassed cases. In addition, a convex output power to current profile is retained, allowing easy integration with existing MPPT-equipped string inverters.

III. Capacitor-Less DCR

It is possible to extend the DCR scheme to be completely capacitor-less by replacing the flying capacitor with a solar cell and its diffusion capacitance. This enables MPPT with cell-level granularity without needing any external passive components for energy storage, which translates to the maximum achievable tracking efficiency at the minimum possible cost for power processing. It has been estimated that cell-level maximum power-point tracking could improve the energy captured in shaded conditions by as high as 30%, a substantial improvement from the estimated 16% with only module-level granularity [15].

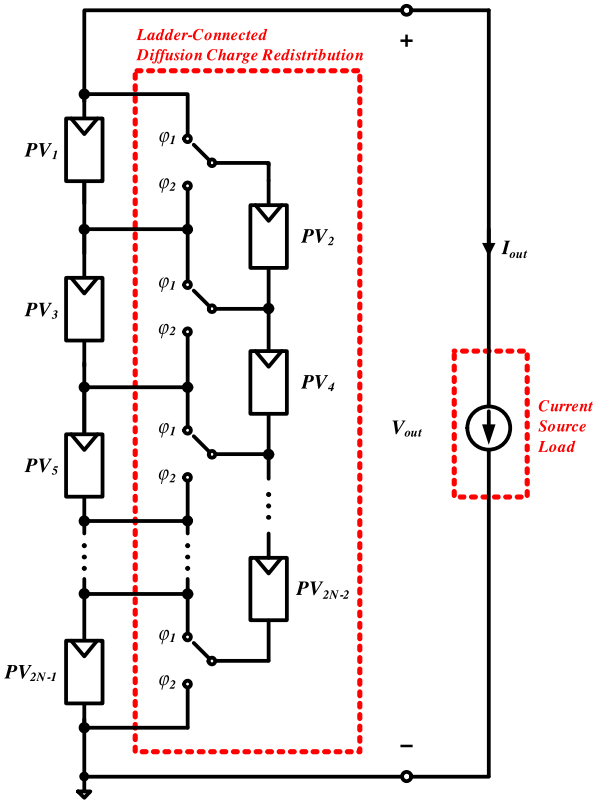


Fig. 5. Proposed fully scalable ladder-connected DCR architecture.

The proposed, fully scalable, cell-level power balancing architecture using DCR is illustrated in Fig. 5. In the proposed topology, a single series string is split into two strings: a load-connected string of N cells in parallel with a switched ladder-connected string of $N-1$ cells used for charge balancing. The load-connected cells are assigned odd designators while the ladder-connected cells are assigned even designators. This approach allows the construction of large series strings to meet the interfacing voltage requirement of a grid-connected inverter, while making the cells appear in pseudo-parallel to mitigate power loss due to mismatch conditions in real-world applications. In short, the switched configuration is able to convert a series string into an effective single "supercell."

The reduction in external energy storage does not come without cost—the implicit tradeoff of eliminating all external storage is having to process part of the string power, specifically the power generated from the ladder-connected string. In the following section, the power conversion efficiency of such a structure is carefully considered and compared to the traditional series string. The additional power conversion loss incurred from this structure compared to a series string under perfectly matching condition will be characterized as an insertion loss.

The switched-capacitor analysis presented in [16] can be generalized to distributed power generation for calculating the insertion loss of adopting DCR. The switched-capacitor conversion loss can be characterized by two asymptotic limits: slow-switching limit (SSL) and fast-switching limit (FSL). In the SSL, the output impedance of the switching converter is calculated assuming all switches and interconnects are ideal, and

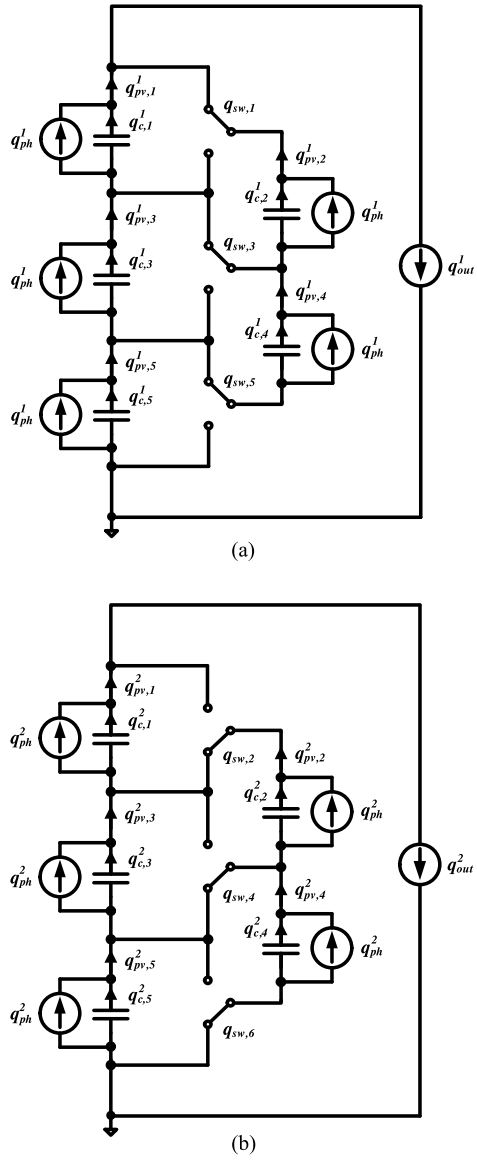


Fig. 6. Charge flow in proposed cell-level power balancing architecture using a 3–2 ladder DCR string configuration: (a) phase 1 and (b) phase 2.

the capacitors experience impulses of current. In the FSL, the capacitor voltages are assumed to be constant, and the switch and interconnect resistances dominate the losses. After deriving both the SSL and FSL losses, the total switched-capacitor loss can be computed as a combination of the SSL and FSL losses.

A. SSL Power Conversion Loss

For illustration, the SSL insertion loss calculation is performed on a 3–2 example string, where N is equal to 3 following the convention shown in Fig. 5. The charge flow diagram of the 3–2 example string in the two phases are illustrated in Fig. 6. The charge flow is designated as $q_{x,i}^{\varphi}$, where x describes the element, i represents the index number, and φ denotes the phase. For example, $q_{\mathrm{pv},2}^{1}$ corresponds to the total charge extracted from the second PV element during phase 1. For the insertion loss calculation, it is assumed that the solar cells are

TABLE I
SSL PV CELL CHARGE MULTIPLIER FOR 3–2 DCR STRING

	SSL PV Cell Charge Multiplier				
Phase (φ)	$a^{\varphi}_{\mathrm{pv},1}$	$a^{\varphi}_{\mathrm{pv},2}$	$a^{\varphi}_{\mathrm{pv},3}$	$a^{\varphi}_{\mathrm{pv},4}$	$a^{\varphi}_{\mathrm{pv},5}$
1	1/10	4/10	3/10	2/10	5/10
2	5/10	2/10	3/10	4/10	1/10

TABLE II
SSL CAPACITOR CHARGE MULTIPLIER FOR 3–2 DCR STRING

SSL Capacitor Charge Multiplier				
$a_{c,1}$	$a_{c,2}$	$a_{c,3}$	$a_{c,4}$	$a_{c,5}$
2/10	1/10	0	1/10	2/10

perfectly matched and each cell contains a constant photocurrent source generating a total charge of q_{ph} over a complete switching period. For a photocurrent source in this two-phase converter

$$q^1_{\mathrm{ph}} = q^2_{\mathrm{ph}} = \frac{q_{\mathrm{ph}}}{2}. \tag{4}$$

The output is represented by a constant current load drawing a total charge of q_{out} over a complete switching period. That is, q_{out} is the sum of the output charges delivered during phase 1 and phase 2, and therefore

$$q^1_{\mathrm{out}} = q^2_{\mathrm{out}} = \frac{q_{\mathrm{out}}}{2}. \tag{5}$$

By using capacitor charge balance in steady state, we can write

$$q^1_{\mathrm{pv},i} + q^2_{\mathrm{pv},i} = q_{\mathrm{ph}} \tag{6}$$

for $i = 1, 2, \ldots, 5$. By Kirchhoff's current law (KCL), we can further write (7) and (8) for the two phases

$$q^1_{\mathrm{pv},1} + q^1_{\mathrm{pv},2} = q^1_{\mathrm{pv},3} + q^1_{\mathrm{pv},4} = q^1_{\mathrm{pv},5} = \frac{q_{\mathrm{out}}}{2} \tag{7}$$

$$q^2_{\mathrm{pv},1} = q^2_{\mathrm{pv},2} + q^2_{\mathrm{pv},3} = q^2_{\mathrm{pv},4} + q^2_{\mathrm{pv},5} = \frac{q_{\mathrm{out}}}{2}. \tag{8}$$

Solving this system of (6)–(8) iteratively yields the relationship between the photocurrent from each cell and the string output current, as shown

$$q_{\mathrm{out}} = \frac{5}{3} \cdot q_{\mathrm{ph}}. \tag{9}$$

Each charge flow can then be expressed in terms of the output charge over a complete switching period. Following the convention in [16], the normalized charge flow, or the charge multiplier will be defined as

$$a^{\varphi}_{x,i} = \frac{q^{\varphi}_{x,i}}{q_{\mathrm{out}}}. \tag{10}$$

The SSL charge multiplier of each PV cell in the 3–2 DCR string during the two phases is summarized in Table I.

The net charge flowing into any diffusion capacitance over a complete switching cycle in steady state will be zero. Each capacitor in Fig. 6 will experience an equal but opposite charge delivery during the two phases. The magnitude of the charge flows for the capacitors can therefore be expressed as the difference between the charge extracted from the solar cell, and the charge generated by the photocurrent source within the cell during either phase

$$a_{c,i} = \frac{|q_{c,i}|}{q_{\mathrm{out}}} = \frac{q^{\varphi}_{\mathrm{pv},i} - (q_{\mathrm{ph}}/2)}{q_{\mathrm{out}}}. \tag{11}$$

Equation (11) can be used to determine the SSL charge multipliers of the capacitors, which are summarized in Table II.

The capacitor charge multiplier vector can be generalized to a DCR string with $2N-1$ cells, where there are N cells in the load-connected string and $N-1$ cells in the ladder-connected string. In the general case, the output current to photocurrent ratio and the capacitor charge multiplier expressions are shown in (12) and (13), respectively

$$q_{\mathrm{out}} = \frac{2N-1}{N} \cdot q_{\mathrm{ph}} \tag{12}$$

$$a_{c,i} = \frac{|q_{c,i}|}{q_{\mathrm{out}}} = \frac{|N-i|}{4N-2}. \tag{13}$$

The SSL output impedance [16] of the DCR string can then be written as

$$R_{\mathrm{SSL}} = \sum_{i=1}^{2N-1} \frac{(a_{c,i})^2}{C_d \cdot f_{\mathrm{sw}}} = \frac{1}{12} \cdot \frac{N \cdot (N-1)}{2N-1} \cdot \frac{1}{C_d \cdot f_{\mathrm{sw}}}. \tag{14}$$

In order to calculate percentage insertion loss, the ratio of the SSL output impedance to the load resistance must be calculated. This can be found as an expression in terms of the performance of each cell in steady state, operating at its maximum power point with voltage V_{mp} and current I_{mp}. Using (12), which effectively relates cell current to output current, and the fact that the DCR string voltage equals N times the cell voltage as shown in Fig. 5, the load resistance is

$$R_L = \frac{V_{\mathrm{out}}}{I_{\mathrm{out}}} = \frac{N \cdot V_{\mathrm{mp}}}{((2N-1)/N) \cdot I_{\mathrm{mp}}} = \frac{N^2}{2N-1} \cdot \frac{V_{\mathrm{mp}}}{I_{\mathrm{mp}}}. \tag{15}$$

The insertion loss fraction $\mathrm{IL}_{\mathrm{SSL}}$ can be calculated as the ratio of the SSL output impedance of the DCR string to the load resistance

$$\mathrm{IL}_{\mathrm{SSL}} = \frac{R_{\mathrm{SSL}}}{R_L} = \frac{1}{12} \cdot \frac{N-1}{N} \cdot \frac{1}{f_{\mathrm{sw}}} \cdot \frac{1}{V_{\mathrm{mp}}} \cdot \frac{I_{\mathrm{mp}}}{C_d} \tag{16}$$

and the SSL efficiency of the array can be defined as one minus the SSL insertion loss. Equation (16) represents a fundamental result that is dependent on technology and material choices. It states that the SSL efficiency of a solar array configured as a DCR string is effectively dictated by the ratio of the maximum power current to the diffusion capacitance, for large N. For illustration, assume the following rounded numbers for our solar cells under maximum illumination: a maximum power voltage

TABLE III
FSL SWITCH CHARGE MULTIPLIER FOR 3–2 DCR STRING

FSL Switch Charge Multiplier					
$a_{\mathrm{sw},1}$	$a_{\mathrm{sw},2}$	$a_{\mathrm{sw},3}$	$a_{\mathrm{sw},4}$	$a_{\mathrm{sw},5}$	$a_{\mathrm{sw},6}$
4/10	2/10	2/10	2/10	2/10	4/10

of 0.5 V, a maximum power current of 2 A, and a diffusion capacitance of 9 μF. For a DCR string with *N* of 20 and a switching frequency of 1 MHz, the insertion loss can be calculated to be a manageable 3.5%.

The SSL insertion loss is not the only loss mechanism. It is possible for the DCR string to operate near the SSL-FSL transition where the loss contributions are approximately equal or deep in FSL where the FSL losses dominate. Hence, to complete the system-level insertion loss characterization, the string output characteristics in the FSL is considered in the next section.

B. FSL Power Conversion Loss

In the FSL, the capacitor voltages are assumed to be constant during a switching period. In addition, the duty cycle becomes an important consideration [16]. For the following analysis, a 50% duty cycle is assumed for simplicity. The output impedance will again be derived in the context of the 3–2 DCR example string for illustration, then generalized to a DCR string of arbitrary size.

From Fig. 6, the charge flowing through the switches can be written using the PV cell charge multipliers as shown

$$a_{\mathrm{sw},i} = \begin{cases} |a^1_{\mathrm{pv},i+1} - a^1_{\mathrm{pv},i-1}|, & i \text{ odd} \\ |a^2_{\mathrm{pv},i} - a^2_{\mathrm{pv},i-2}|, & i \text{ even} \end{cases} \tag{17}$$

where boundary cases, i.e., $a^1_{\mathrm{pv},0}$ and $a^1_{\mathrm{pv},2N}$ are assumed to be zero. The resulting FSL charge multiplier vector for the 3–2 DCR string is summarized in Table III. For a DCR string with $2N-1$ total cells, the FSL switch charge multiplier vector can be derived as

$$a_{\mathrm{sw},i} = \begin{cases} (N-1)/(2N-1), & i = 1,\ 2N \\ 1/(2N-1), & \text{otherwise.} \end{cases} \tag{18}$$

Hence, the FSL output impedance of an arbitrarily sized DCR string is

$$R_{\mathrm{FSL}} = 2 \cdot \sum_{i=1}^{2N-1} R_{\mathrm{eff}} \cdot (a_{\mathrm{sw},i})^2 = 4 \cdot \frac{N \cdot (N-1)}{(2N-1)^2} \cdot R_{\mathrm{eff}} \tag{19}$$

where R_{eff} is the effective resistance of the switch on resistance in series with any interconnect resistance. Relating the FSL output impedance back to the load resistance, the FSL insertion loss can be calculated as

$$\mathrm{IL}_{\mathrm{FSL}} = \frac{R_{\mathrm{FSL}}}{R_L} = \frac{4}{2N-1} \cdot \frac{N-1}{N} \cdot \frac{I_{\mathrm{mp}}}{V_{\mathrm{mp}}} \cdot R_{\mathrm{eff}}. \tag{20}$$

The result in (20) makes intuitive sense because the loss from the FSL is expected to be inversely proportional to the number of cells behaving like current sources. The dissipated power in the switches is approximately constant for sufficiently large *N*, while the total generated power increases linearly with *N*. Note that the factor of 4 in (20) can be derived by using the fact that the power extracted from the ladder-connected string must pass through two switching devices. In addition, the current through the switches resemble a square wave, which gives an additional factor of two in power.

From (20), the FSL insertion loss, or conduction loss, can almost always be made negligible for a sufficiently large string. For example, for a DCR string with *N* of 20, maximum power current of 2 A, maximum power voltage of 0.5 V, and an effective switch on-resistance of 15 mΩ, the FSL insertion loss is only 0.58%.

The total insertion loss can be calculated by combining the SSL and FSL losses. A conservative approximation for loss components, will be used for the remainder of this paper [25]. That is

$$\mathrm{IL}_{\mathrm{TOT}} \cong \sqrt{(\mathrm{IL}_{\mathrm{SSL}})^2 + (\mathrm{IL}_{\mathrm{FSL}})^2}. \tag{21}$$

C. Recovered Power Loss From Process Variation

The DCR power processing approach also effectively corrects for process variation between cells, which normally would limit power extraction from a string of cells. DCR, therefore, can improve power extraction from an array of mismatched cells in comparison to other approaches for processing power. Alternatively, DCR can be viewed as easing the manufacturing problem of assembling a solar array by accommodating greater cell variation while maximizing power extraction.

Process variation in PV manufacturing typically refers to the *I–V* mismatch between the solar cells. For a series string of solar cells, *I–V* mismatch can negatively impact the overall tracking efficiency because the cells may not operate at their individual maximum power points. Instead, they operate at a collective maximum power current for all the cells present in the series string.

In order to improve the cell-level tracking efficiency by reducing cell-to-cell variation, solar panel manufacturers have invested greatly in improving their manufacturing process as well as evaluating different cell binning algorithms [17], [18]. In the past ten years, the manufacturers have been able to refine their production process and reduce the power tolerance from $\pm 10\%$ down to $\pm 3\%$ [19]. Nevertheless, the *I–V* mismatch can still have higher tolerance when cells are sorted by maximum power.

The subsequent analysis follows [8] in using a first-order approximation for cell output power under deviation from the maximum power point operation. Assuming approximately constant voltage near the maximum power point, the output power (P_{cell}) can be assumed to be step-wise linear when the cell output current (I_{cell}) is slightly perturbed around the maximum power current

$$I_{\mathrm{cell}} = (1-\delta) \cdot I_{\mathrm{mp}} \tag{22}$$

$$P_{\mathrm{cell}} = (1-|\delta|) \cdot P_{\mathrm{mp}}. \tag{23}$$

To understand the effect of variation on a string, let δ_i be a random variable that describes the deviation of the current at the collective maximum power of the string to the current of cell *i*

at its maximum power operation. That is, the total power from a series string can be written as

$$P_{\text{string}} = \sum_i (1 - |\delta_i|) \cdot P_{\text{mp}}. \tag{24}$$

Then, the expected power from a series string of N cells can be expressed as

$$E[P_{\text{string}}] = N \cdot P_{\text{mp}} \cdot (1 - E[|\delta|]). \tag{25}$$

Using (25), the power loss due to process variation can be approximated as the deviation from the maximum available string power $N \cdot P_{\text{mp}}$. This represents a conservative estimate; the actual power loss can be higher because the magnitude of dP/dI can be much higher when $I > I_{\text{mp}}$. For a more detailed treatment, a Monte Carlo analysis of the expected power with cell-to-cell variation can be found in [8].

Assuming a uniform distribution of δ_i with a range of $\pm 5\%$, the loss in tracking efficiency in a series string due to process variation is approximately 2.5%. Since the DCR string is able to mitigate even larger partial shading mismatches, it will be practically indifferent to the asymmetry from process variation. Hence, the loss in tracking efficiency from cell-to-cell variation, illustrated by $E[|\delta|]$ in (25), can be naturally recovered. A correction factor is introduced in the overall insertion loss calculation, and complete insertion loss from using a DCR string can then be approximated as

$$\text{IL}_{\text{DCR}} \cong \sqrt{(\text{IL}_{\text{SSL}})^2 + (\text{IL}_{\text{FSL}})^2} - E[|\delta|]. \tag{26}$$

Potentially, the greatest value in performing cell-level MPPT with DCR lies in the fact that the string output power becomes independent of cell-to-cell process variation. Therefore, it is possible to relax the extensive and stringent binning process currently employed in manufacturing. It may also greatly simplify manufacturing and assembly processes.

IV. Circuit Implementation

A DCR string experimental prototype was constructed to further validate the proposed concept. To ensure fair comparison across different configurations, the prototype was designed to be reconfigurable between a series string, a series string with bypass diodes, and the proposed DCR arrangements so that all measurements would be performed using the same set of solar cells. The schematic representation of the DCR prototype is outlined in Fig. 7(a), and the printed circuit board (PCB) implementation is illustrated in Fig. 7(b).

The experimental prototype consisted of five P-Maxx-2500 mA monocrystalline solar cells, six IRF9910 MOSFET switches, three MAX17600 gate drives, and five optional LSM115J Schottky diodes. While discrete switches, gate drives, and an external power supply are used in this proof-of-concept prototype, all the DCR enabling circuits can be integrated onto a single chip for real-life applications. A discussion on the required circuit subsystems for an IC implementation is elaborated below.

As shown in Fig. 7(a), the MOSFET switches and the gate-drives are the first targets for integration. Previously proposed ladder converter gate-drive circuits such as the one shown in [2] can be readily adopted. Furthermore, because the chip only

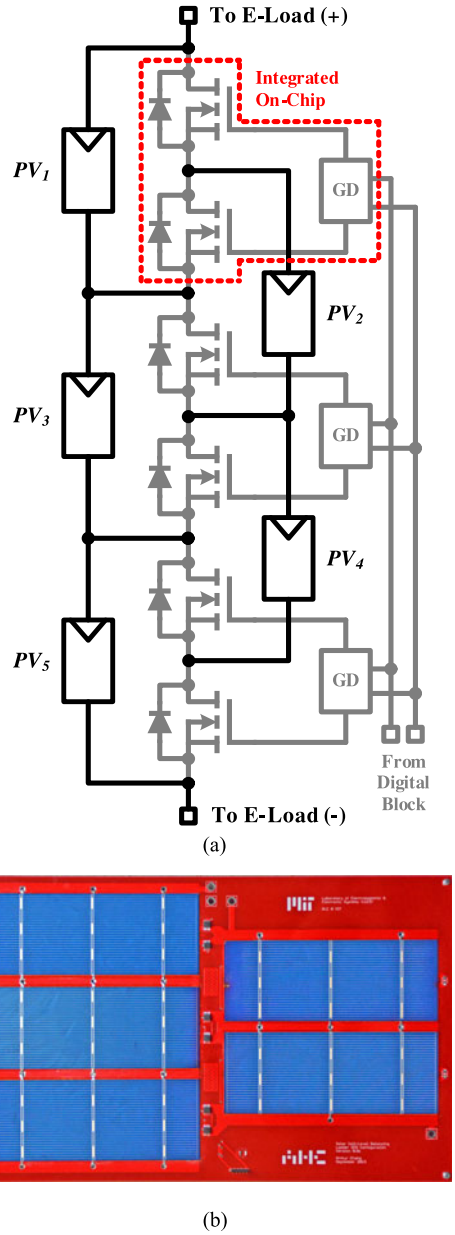


Fig. 7. Experimental prototype of the proposed DCR converter: (a) schematic representation and (b) PCB implementation.

processes small solar cell voltages, it is not necessary to fabricate using expensive high-voltage process nodes. Instead, relatively inexpensive and mature technology nodes such as the 0.35-μm CMOS and the 0.5-μm CMOS processes can be used. To self-power the circuit from the solar cells, the IC must also include a local power management unit consisting of an on-chip switched-capacitor dc–dc converter and a low-dropout (LDO) regulator. Finally, digital blocks for synchronization need to be included to control switching in all the ICs.

The number of MOSFETs and complementary gate drives to integrate onto a single chip is determined by trading off IC fabrication cost, supply voltage requirement, ease of integration, and integration cost. In particular, if the minimum two MOSFETS and one complementary gate drive are integrated, an IC would

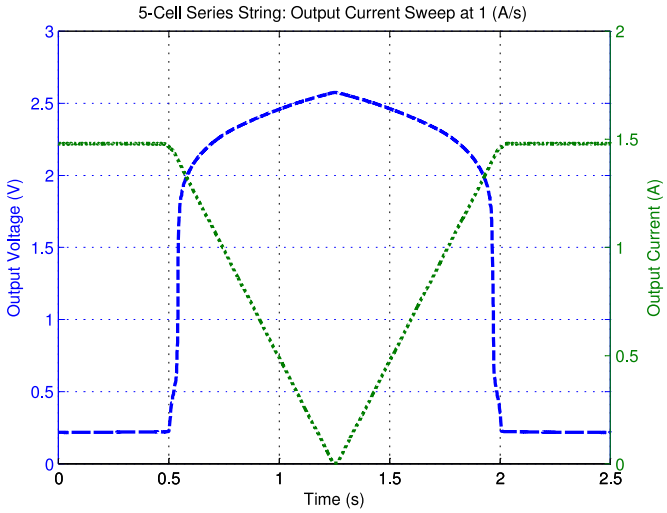


Fig. 8. Experimental measurement of output voltage and current of a five-cell series string by sweeping the output current at 1 A/s.

be required for every two solar cells. While the IC would only need to make contacts to two solar cells, which keeps the integration cost at a minimum, it would have to power up from a small forward voltage of a single diode. Alternatively, if more than one pairs of MOSFETs and complementary gate drives are integrated, the IC can balance multiple pairs of solar cells, and access to a higher input voltage with the added advantage of sharing the power management circuit. This leads to fewer ICs per panel and can potentially reduce the overall incremental cost per watt. However, the IC would have to make direct contacts to more solar cells, which complicates wiring and increases integration costs. These tradeoffs will ultimately dictate the level of integration as the PV market is highly cost-driven.

V. Experimental Results

The circuit shown in Fig. 7(b) was characterized in the laboratory with a power supply, an HP 6063B dc electronic load, and a Tektronix TDS5034B oscilloscope to collect current and voltage data. Specifically, the characteristic output power versus output current curve is obtained by recording both the string output voltage and the output current as the electronic load sweeps the output current from 0 to 10 A at a slew rate of 1 A/s. As the electronic load demands more current than the series string can supply, the current saturates at the short-circuit current of the string, as illustrated in Fig. 8. Furthermore, the effect of process variation can be observed in the voltage waveform. That is, if the short-circuit current of the individual cells are perfectly matched, the string is expected to have a zero output voltage at the short-circuit current. However, if there is mismatch between the cells, cells with higher short-circuit circuit can maintain a positive voltage as the string current is limited by the cells with lower short-circuit current.

Fig. 9 shows the experimental output power measurement of a five-cell series string with and without bypass diodes, compared to a 3–2 DCR string. From the five-cell series string measurement under uniform irradiance in Fig. 9(a), the maximum power

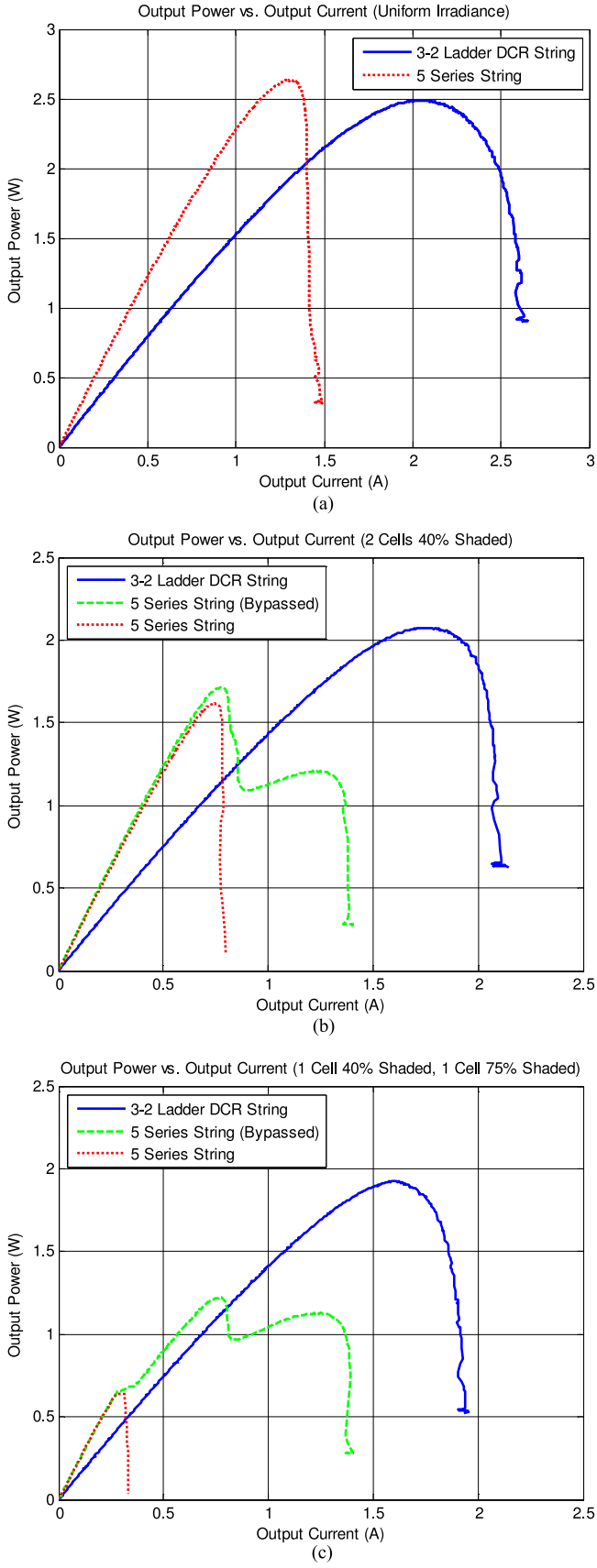


Fig. 9. Experimental measurement of a 3–2 DCR string under various partial shading conditions compared to the five-series string: (a) uniform irradiance, (b) two cells 40% shaded, (c) one cell 40% shaded, and one cell 75% shaded.

TABLE IV
MEASURED OUTPUT POWER COMPARISON AND EFFICIENCY SUMMARY

	Uniform Irradiance		**2 Cells 40% Shaded (16% Overall Shading)**		**1 Cell 40% Shaded, 1 Cell 75% Shaded (23% Overall Shading)**	
Configuration ($N = 3$)	*Power (W)*	*Conversion Efficiency*	*Power (W)*	*Extracted Percentage*	*Power (W)*	*Extracted Percentage*
Series String	2.63	100%	1.62	61.6%	0.64	24.3%
Series + Bypass	2.63	100%	1.71	65.0%	1.22	46.4%
DCR String	2.49	94.7%	2.075	83.3%	1.92	77.1%

current I_{mp} and voltage V_{mp} of the cells can be extracted to be 1.31 A and 0.40 V, respectively. The diffusion capacitance can then be calculated from Fig. 2(c) to be approximately 6.25 μF. The DCR string has a switching frequency of 500 kHz, and the expected SSL conversion loss is 5.8% from (16). Assuming the switch on resistance dominates the effective resistance, the expected FSL conversion loss is 4.1% from (20). Hence, the total insertion loss can be calculated from (21) to be 7.1%.

The measured output power of the five-cell series string has a peak at 2.63 W, and the measured output power of the 3–2 DCR string has a maximum of 2.49 W. This gives a measured efficiency of 94.7%, or a measured DCR insertion loss of 5.3%. The lower measured insertion loss, compared to the calculated 7.1%, can be attributed to the recovery of losses from process variation as shown in (26).

Fig. 9(b) and (c) illustrates the measured output power characteristic curves under different shading conditions, where the shading percentage is determined by measuring the change in short-circuit current of the shaded cells. The series string is shown to lose a significant portion of the string power even when only a small percentage of the total area is shaded. With bypass diodes in place, the string is able to extract more power. However, the resulting output power characteristic curve is nonconvex, i.e., with multiple maxima, which introduces additional constraints to the required MPPT algorithm. In the case of the DCR string, significantly more power can be extracted. Moreover, the output power characteristic curve remains convex, which greatly reduces the complexity of the required MPPT algorithm.

The maximum measured power for each configuration is tabulated in Table IV, where the extracted percentage column illustrates the ratio of power extracted to the total available power under uniform irradiance for the same configuration. It can be seen that in the case of DCR, the extracted percentage follows one minus the overall shading percentage quite closely, which validates the effectiveness of the proposed power balancing technique.

VI. CONCLUSION AND FUTURE CONSIDERATIONS

A new cell-level power balancing scheme, DCR, has been presented to increase energy extraction and improve MPPT efficiency under partial shading conditions. This technique makes an array of solar cells behave as an effective single supercell, which can also potentially eliminate the need for testing and binning during production. The proposed technique trades off processing power differentially to minimizing the number of external energy storage components. In the limit where only the intrinsic solar cell diffusion capacitances are used for cell-level power balancing, the finest achievable MPPT granularity can be reached at the minimum possible cost for power electronics.

With a reduced per-converter component count, i.e., no external capacitive or inductive energy storage, the proposed solution can potentially become cost effective at the cell-level, which has been cost prohibitive using the current state of the art, including cascaded module-level power electronic (MLPE) such as dc power optimizers [7], [8] and microinverters [9], and submodule-level DPP converters using switched-capacitor [2], [3] or switched-inductor [4]–[6] techniques. In addition, with power optimization granularity down to the cell level, substantial improvement in energy capture can also be achieved compared to module and submodule level solutions [15].

A fully scalable ladder-type DCR string architecture has been presented along with the analysis method to characterize the insertion losses at the SSL and FSL. A proof-of-concept system consisting of a 3–2 DCR string has been constructed and characterized. Experimental results show the DCR string extracting significantly more energy under various partial shading conditions compared to the traditional series string and series string with bypass diodes.

The proposed approach requires that the DCR circuits be integrated into the solar panels. This means that the proposed technique is not a retrofit solution and must be incorporated into the manufacturing process. While the additional wiring cost is typically secondary compared to the cost of the ICs, changing the stringing pattern of the solar cell will likely present a barrier to adoption. There is more room for work on manufacturing strategies that enable ease of integration [26] or new paradigms of solar cell fabrication that embed power electronics on the same substrate [27]–[29]. Associated with these are innovations in the areas of solar cell fabrication, chip packaging, interconnects, and panel lamination.

ACKNOWLEDGMENT

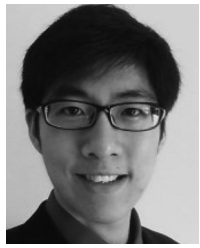
The authors would like to thank Prof. M. el-Sayed at Kuwait University for helpful discussions.

REFERENCES

[1] C. Olalla, M. Rodriguez, D. Clement, J. Wang, and D. Maksimovic, "Architecture and control of PV modules with submodule integrated converters," in *Proc. 2012 IEEE 13th Workshop Control Modeling Power Electron.*, Jun. 10–13, pp. 1–6.

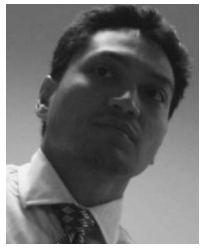
[2] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "A resonant switched-capacitor IC and embedded system for sub-module photovoltaic power

management," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3043–3054, Dec. 2012.
[3] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "Resonant switched-capacitor converters for sub-module distributed photovoltaic power management," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1189–1198, Mar. 2013.
[4] P. S. Shenoy, K. A. Kim, and P. T. Krein, "Comparative analysis of differential power conversion architectures and controls for solar photovoltaics," in *Proc. IEEE 13th Workshop Control Modeling Power Electron.*, Jun. 10–13, 2012, pp. 1–7.
[5] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, "Differential power processing for increased energy production and reliability of photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968–2979, Jun. 2013.
[6] Q. Shibin and R. C. N. Pilawa-Podgurski, "Sub-module differential power processing for photovoltaic applications," in *Proc. 2013 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 17–21, pp. 101–108.
[7] G. R. Walker and P. C. Sernia, "Cascaded DC–DC converter connection of photovoltaic modules," in *Proc. 2002 IEEE 33rd Annu. Power Electron. Spec. Conf.*, vol. 1, pp. 24–29.
[8] A. H. Chang, J. J. Cooley, and S. B. Leeb, "A systems approach to photovoltaic energy extraction," in *Proc. 2012 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 5–9, pp. 59–70.
[9] A. Trubitsyn, B. J. Pierquet, A. K. Hayman, G. E. Gamache, C. R. Sullivan, and D. J. Perreault, "High-efficiency inverter for photovoltaic applications," in Proc. *2010 IEEE Energy Convers. Congr. Expo.*, Sep. 12–16, pp. 2803–2810.
[10] G. Friesen and H. A. Ossenbrink, "Capacitance effects in high-efficiency cells," *Solar Energy Mater. Solar Cells*, vol. 48, no. 1–4, pp. 77–83, Nov. 1997.
[11] S. K. Sharma, D. Pavithra, G. Sivakumar, N. Srinivasamurthy, and B. L. Agrawal, "Determination of solar cell diffusion capacitance and its dependence on temperature and 1 MeV electron fluence level," *Solar Energy Mater. Solar Cells*, vol. 26, no. 3, pp. 169–179, Apr. 1992.
[12] R. A. Kumar, M. S. Suresh, and J. Nagaraju, "Measurement and comparison of AC parameters of silicon (BSR and BSFR) and gallium arsenide (GaAs/Ge) solar cells used in space applications," *Solar Energy Mater. Solar Cells*, vol. 60, no. 2, pp. 155–166, Jan. 15, 2000.
[13] R. A. Kumar, M. S. Suresh, and J. Nagaraju, "Silicon (BSFR) solar cell AC parameters at different temperatures," *Solar Energy Mater. Solar Cells*, vol. 85, no. 3, pp. 397–406, Jan. 31, 2005.
[14] C. R. Jeevandoss, M. Kumaravel, and V. J. Kumar, "A novel method for the measurement of the *C–V* characteristic of a solar photovoltaic cell," in *Proc. 2010 IEEE Instrum. Meas. Technol. Conf.*, May 3–6, pp. 371–374.
[15] S. M. MacAlpine, R. W. Erickson, and M. J. Brandemuehl, "Characterization of power optimizer potential to increase energy capture in photovoltaic systems operating under nonuniform conditions," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2936–2945, Jun. 2013.
[16] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," in *Proc. 2006 IEEE Workshops Comput. Power Electron.*, Jul. 16–19, pp. 216–224.
[17] H. Field and A. M. Gabor, "Cell binning method analysis to minimize mismatch losses and performance variation in Si-based modules," in *Proc. Conf. Rec. 29th IEEE Photovoltaic Spec. Conf.*, May 19–24, 2002, pp. 418–421.
[18] K. Wilson, D. De Ceuster, and R. A. Sinton, "Measuring the effect of cell mismatch on module output," in *Proc. Conf. Rec. IEEE 4th World Conf. Photovoltaic Energy Convers.*, May 2006, vol. 1, pp. 916–919.
[19] T. Noguchi, S. Togashi, and R. Nakamoto, "Short-current pulse based adaptive maximum-power-point tracking for photovoltaic power generation system," in *Proc. 2000 IEEE Int. Symp. Ind. Electron.*, vol. 1, pp. 157–162.
[20] E. Romero-Cadaval, G. Spagnuolo, L. G. Franquelo, C. A. Ramos-Paja, T. Suntio, and W. M. Xiao, "Grid-connected photovoltaic generation plants: Components and operation," *IEEE Ind. Electron. Mag.*, vol. 7, no. 3, pp. 6–20, Sep. 2013.
[21] R. F. Coelho, F. Concer, and D. C. Martins, "A proposed photovoltaic module and array mathematical modeling destined to simulation," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2009, pp. 1624–162.
[22] A. Chatterjee, A. Keyhani, and D. Kapoor, "Identification of photovoltaic source models," *IEEE Trans. Energy Convers.*, vol. 26, no. 3, pp. 883–889, Sep. 2011.
[23] M. G. Villalva, J. R. Gazoli, and E. R. Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1198–1208, May 2009.
[24] R. Jayakrishnan, S. Gandhi, and P. Suratkar, "Correlation between solar cell efficiency and minority carrier lifetime for batch processed multicrystalline Si wafers," *Mater. Sci. Semicond. Process.*, vol. 14, no. 3–4, pp. 223–228, Sep.–Dec. 2011.
[25] M. D. Seeman, "A design methodology for switched-capacitor DC–DC converters," Ph.D. dissertation, Dept. EECS, University of California, Berkeley, USA, May 2009.
[26] M. C. Barr, J. A. Rowehl, R. R. Lunt, J. J. Xu, A. Wang, C. M. Boyce, S. G. Im, V. Bulovic, and K. K. Gleason, "Direct monolithic integration of organic photovoltaic circuits on unmodified paper," *J. Adv. Mater.*, vol. 23, no. 31, pp. 3500–3505, Aug. 2011.
[27] C. L. Bellew, S. Hollar, and K. S. J. Pister, "An SOI process for fabrication of solar cells, transistors and electrostatic actuators," in *Proc. 12th Int. Conf. Transducers, Solid-State Sens., Actuators Microsyst.*, Jun. 8–12, 2003, vol. 2, pp. 1075–1078.
[28] A. M. Imtiaz and F. H. Khan, "AC solar cells: An embedded 'all in one' PV power system," in *Proc. 2012 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 5–9, pp. 2053–2059.
[29] A. M. Imtiaz and F. H. Khan, "Light-generated effects on power switches used in a planar PV power system with monolithically embedded power converters," *IEEE J. Photovoltaics*, vol. 3, no. 1, pp. 394–400, Jan. 2013.



Arthur H. Chang (S'09) received the B.S. and M.S. degrees in electrical engineering from the California Institute of Technology, Pasadena, USA, in 2009 and 2010, respectively. He is currently working toward the Ph.D. degree in electrical engineering and computer science at the Massachusetts Institute of Technology (MIT), Cambridge, USA, where he is affiliated with the Laboratory of Electromagnetic and Electronic Systems.

Dr. Chang was the recipient of the National Defense Science and Engineering Graduate (NDSEG) Fellowship (2009–2012), the Analog Devices Outstanding Student Designer Award (2010), and the Applied Power Electronics Conference & Exhibition (APEC) Outstanding Technical Presentation Awards (2013 and 2014). He was also the grand prize winner of the MIT Clean Energy Prize (2014), and the recipient of the Tau Beta Pi (Williams No. 30) Fellowship (2009) and the Caltech Upper Class Carnation Merit Scholarship (2008).



Al-Thaddeus Avestruz (M'90) received the S.B. degree in physics in 1994, and the S.M. and E.E. degrees in electrical engineering in 2006, from the Massachusetts Institute of Technology (MIT), Cambridge, USA, where he is currently working toward the Ph.D. degree in electrical engineering in the Laboratory for Electromagnetic and Electronic Systems.

He was with several companies, including Talking Lights, LLC, Brighton, MA, USA; Teradyne Corporation, North Reading, MA; Thornton, Inc. (presently Mettler-Toledo Thornton, Bedford, MA); and Diversified Technologies, Inc., Bedford, MA, before returning to MIT. His current research interests include design, modeling, and realization of circuits, power conversion, energy, and electromagnetic systems. Recent topics include solar energy, induction heating, and wireless power transfer for biomedical systems.

Steven B. Leeb (S'89–M'91–SM'01–F'07) received the Ph.D. degree from the Massachusetts Institute of Technology (MIT), Cambridge, USA, in 1993.

He was a Commissioned Officer in the USAF reserved. Since 1993, he has been a Member on the MIT faculty in the Department of Electrical Engineering and Computer Science. He also holds a joint appointment in MIT's Department of Mechanical Engineering. He currently a MacVicar Fellow and Professor of Electrical Engineering and Computer Science in the Laboratory of Electromagnetic and Electronic Systems, MIT, where he is involved in the design, development, and maintenance processes for all kinds of machinery with electrical actuators, sensors, or power electronic drives. He is the author or coauthor of over 100 publications and 15 U.S. patents in the fields of electromechanics and power electronics.