Analysis and Design of DC System Protection Using Z-Source Circuit Breaker

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***Abstract*—A modified Z-source breaker topology is introduced to minimize the reflected fault current drawn from a source while retaining a common return ground path. Conventional Z-source breaker topologies do not provide steady-state overload protection and can only guard against extremely large transient faults. The Z-source breaker can be designed for considerations affecting both rate of fault current rise and absolute fault current level, analogous in some respects to a thermal-magnetic breaker. Detailed analysis and design equations are presented to provide a framework for sizing components in the Z-source breaker topology. In addition, the proposed manual tripping mechanism enables protection against both instantaneous current surges and longer-term overcurrent conditions. The fault operation intervals of the proposed Z-source breaker topologies are both demonstrated in SPICE simulation and validated in experimental characterization.**

***Index Terms*—Circuit breakers, circuit faults, electrical fault detection, fault currents, power filters, power system protection, Q-factor, thyristor circuits.**

I. Introduction

DIRECT current power distribution is under examination for many applications such as the MVDC power architecture of future naval vessels [1]–[4], and the dc or hybrid ac/dc grid networks with distributed energy resources [5]–[8]. The dc power system architecture has attracted interest as a means for achieving higher overall efficiency for dc loads, enabling easier integration of renewable and distributed energy sources, and providing uninterruptible power with readily available energy storage elements [9]–[11].

However, to enable widespread adoption of dc power systems, the reliability of fault protection is essential. The lack of a natural voltage or current zero-crossing to extinguish an arc that can occur when opening a breaker presents a well-known challenge to protecting dc distribution systems [12]–[15]. Traditional solid state dc breakers typically rely on an auxiliary solid-state switching device and a precharged commutation capacitor or a passive network to force commutate the main solid-state switching device by reverse biasing. This can enable fast and arcless current interrupting capabilities. However, the auxiliary solid-state switching device must be actively driven to reverse bias the main switch before the fault current rises beyond the interrupt capability of the breaker. Hence, strict detection and timing requirements must be imposed on the existing design. Additional active circuitry is also needed to precharge the force commutation circuit.

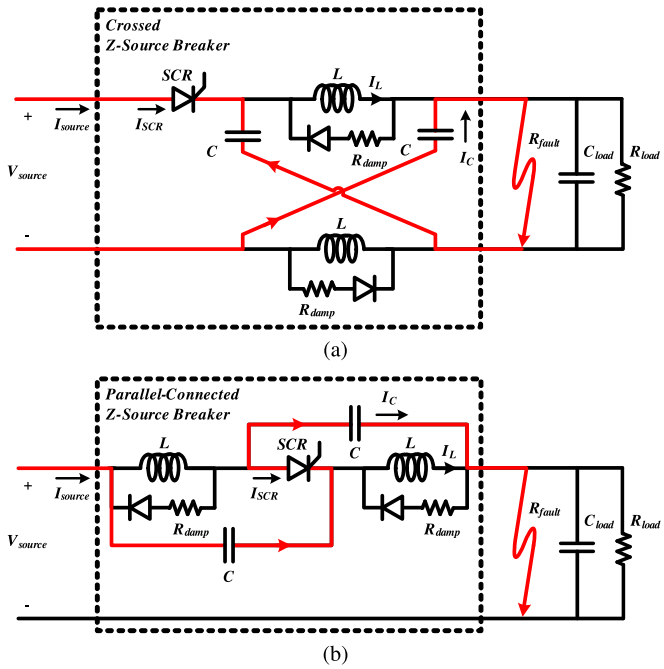

Fig. 1. Previously proposed Z-source circuit breaker: (a) crossed Z-source topology and (b) parallel-connected Z-source topology.

By creatively reconfiguring the Z-source inverter, the recently introduced Z-source circuit breaker potentially mitigates these problems [16]–[19]. Previously proposed Z-source circuit breaker topologies are illustrated in Fig. 1. The Z-source breaker operates on the principle of natural commutation for critical fault conditions. Under critical fault conditions, it may be difficult to ensure fast detection and accurate timing for forced commutation. When a large transient fault occurs, the Z-source breaker provides a fraction of the transient fault current through the Z-source capacitors and thereby forces a current zero-crossing in the SCR (silicon-controlled rectifier). Once the current in the SCR reaches zero, the SCR naturally commutates off and the faulty load becomes isolated from the source. Natural commutation of the Z-source configuration allows the fault to be cleared before having to apply control signals to disable sending gate pulses to the SCR. However, practical uses of this technique are limited because the existing Z-source breaker does not provide steady-state overload protection and can only guard against large

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transient faults. For faults of lesser severity and slower dynamics, the fault current may not be sufficiently large to naturally commutate the breaker. In these cases, a new forced commutation circuitry can be introduced to the breaker topology. The boundary between natural and forced commutation will also be derived in the paper.

Furthermore, the previously proposed Z-source breaker topology shown in Fig. 1(a) does not provide a common ground between the generation source and the load, and the topology shown in Fig. 1(b) reflects a large fault current to the generation source. This paper aims to address the aforementioned shortcomings by presenting a new Z-source breaker topology which minimizes the reflected fault current drawn from the generation source while retaining a common return ground path [17]. This will provide designers more flexibilities when evaluating a Z-source circuit breaker for protection in their respective applications. Comparison to the previously proposed Z-source breakers is discussed in Section II. Comprehensive analyses, including minimum detectable fault current magnitude and ramp rate, component sizing of the Z-source circuit breaker are presented in Section III. In addition, manual tripping mechanisms, which enable protection under both instantaneous large current surges and longer-term overcurrent conditions, are introduced and analyzed in Section IV. Finally, experimental results of the proposed Z-source circuit breaker with extended protection schemes are presented in Section V.

II. Z-Source Breaker Overview

The Z-source breaker consists of an SCR, a pair of *LC* legs, and snubber diodes and resistors. Different topologies of the Z-source breaker arise from different *LC* configurations while maintaining the same operating principle. When a fault occurs, the fault current is supplied from both the load capacitor and the high-frequency conduction path through the Z-source capacitors as illustrated in red in Fig. 1. Note that the high-frequency conduction path through the Z-source capacitors, or the shoot-through path, is antiseries to the SCR forward current, which forces commutations if the Z-source capacitor current reaches the level of the Z-source inductor current.

The Z-source topology shown in Fig. 1(a) uses a crossed *LC* connection and will therefore by referred to as the crossed Z-source configuration. The crossed Z-source topology requires an inductor to be placed in the return path of the dc source, which can be seen as a disadvantage in systems where a common ground is preferred. The Z-source topology shown in Fig. 1(b) places the *LC* pairs completely in-line with the power source to provide a common ground. This topology will be referred to as parallel-connected Z-source because the *LC* legs are connected in parallel after the SCR commutates off. The parallel-connected Z-source topology allows for common ground connection between the source and all loads, but it reflects a large fault current at the source because the high-frequency conduction path through the Z-source capacitors is directly in-line with the source.

In order to preserve a common ground connection while reducing the amount of fault current reflected to the source, a new Z-source breaker topology is proposed and shown in Fig. 2. The source-connected capacitor in the parallel-connected topology is replaced by a shunt capacitor to ground. The new topology is termed series-connected because the *LC* legs are connected in series once the SCR commutates off. The series-connected topology provides the fault current from an energy storage element instead of the source. Hence, the reflected current to the source during breaker operation is greatly reduced.

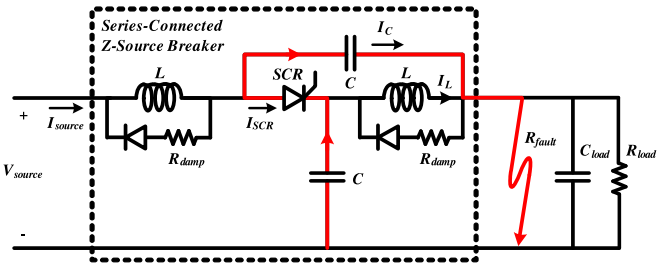

Fig. 2. New series-connected Z-source circuit breaker topology.

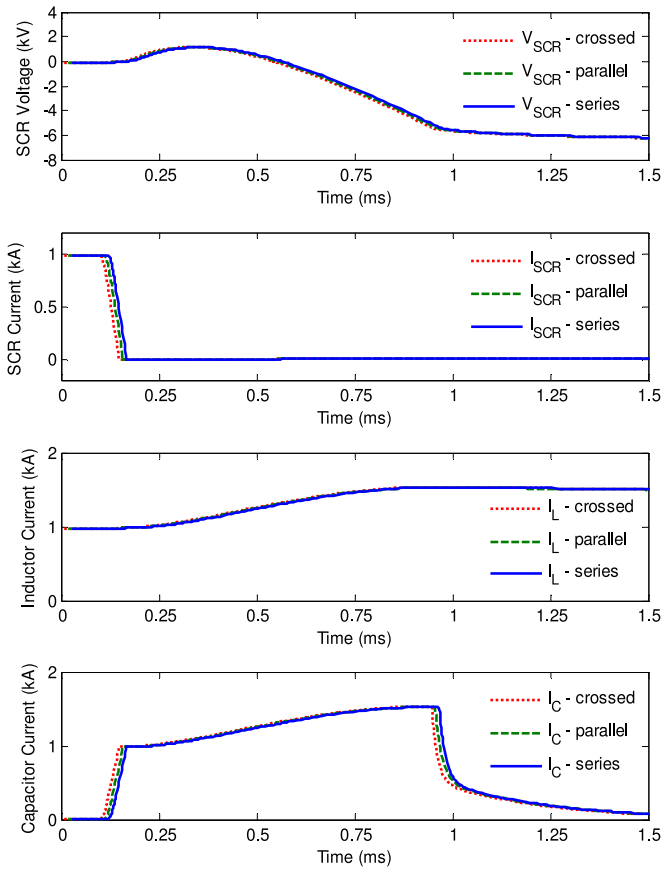

Fig. 3. Fault clearing waveforms for the three Z-source circuit breakers. Waveforms for the parallel-connected and series-connected are shifted right by 10 and 20 μs, respectively, for clarity.

A. Fault Clearing Waveforms

The full set of fault clearing waveforms for the three Z-source topologies is shown in Fig. 3. The waveform variables are as

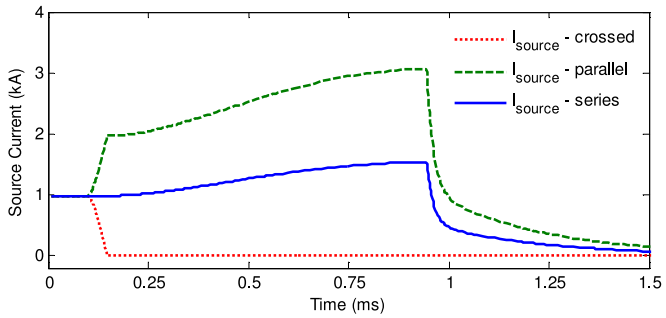

Fig. 4. Comparison of the reflected fault current at the source among the three Z-source circuit breaker topologies.

labeled in Figs. 1 and 2. The simulated system has a source voltage of $V_{\text{source}} = 6$ kV with a maximum load power of 6 MW, i.e., a load resistance of $R_{\text{load}} = 6\ \Omega$. The load capacitance is assumed to be $C_{\text{load}} = 1$ mF, and the Z-source parameters are chosen to be $C = 200\ \mu$F and $L = 2.4$ mH.

In the simulation, the system first operates under steady-state condition until a fault with conductance $G_{\text{fault}} = 5\ \Omega^{-1}$ occurs near 100 μs. It is assumed that the fault conductance ramps up linearly to the final value in $\Delta t = 0.1$ ms, which translates to a fault conductance ramp rate of $50\,000\ \text{s}^{-1}\Omega^{-1}$. This corresponds to to an effective cable inductance of 20 μH, which is comparable to the estimate presented in [20]. In addition, these numbers are chosen for illustrative purposes only. In a real system, the fault conductance can be determined by the failure type, and the fault conductance ramp rate can be bounded by the cable inductance.

As shown in Fig. 3, the characteristic fault clearing waveforms—SCR voltage and current, Z-source inductor and capacitor currents—are shown to be identical across all three topologies. When the fault is introduced, the transient fault current will be supplied by both the Z-source capacitors and the load capacitor because the Z-source inductor current cannot change instantaneously. The Z-source capacitor current will increase until it reaches the Z-source inductor current. At this point, the SCR experiences a current zero-crossing and is allowed to commutate off naturally. Once the SCR turns off, the two *LC* legs start a resonance where they supply the fault from their respective energy storage. This resonance will continue until the inductor voltage tries to become negative. At this point, the snubber diodes turn on to steer the current away from the capacitors, and the current will continue to flow in the snubber loop until the energy stored in the inductor decays to zero.

However, there are important differences in the amount of fault current reflected back to the source, as illustrated in Fig. 4. In the case of the crossed Z-source circuit breaker, the current drawn from the source equals the SCR current. Therefore, no fault current is reflected to the source as soon as the SCR commutates off.

In the parallel-connected Z-source breaker, the current drawn from the source during a fault interval equals the sum of the Z-source inductor and capacitor currents. Hence, in order to trip the Z-source breaker, the source must be able provide a transient current that is at least twice its maximally rated nominal steady-state current. This large transient current requirement may be seen as a major disadvantage for this topology and may impose additional requirements on the input filter.

In the series-connected Z-source breaker, the high-frequency conduction path is intentionally directed away from the source by the use of a shunt capacitor. As a result, the current drawn from the source during a fault interval becomes the Z-source inductor current alone. This reduces the source transient current requirement by half compared to the parallel-connected topology.

B. Voltage Transfer Function

In this section, the ac transfer function of the unfaulted Z-source circuit will be evaluated—The frequency response of each circuit not only indicates behavior as an input filter, either alone or in conjunction with an explicit filter, but also highlights issues in input stability that may arise when dc–dc converters appear as an active load. A discussion of input filter design and the related stability for power converters can be found in [21]. The following input-output voltage transfer functions are derived assuming matching pairs of Z-source inductors and capacitors, which gives the most optimal capacitive current divider ratio. The effect of the capacitive current divider and its relations to the minimum detectable fault current will be discussed at length in Section III. In addition, a resistive load is used for illustration purposes; for other loads, the designer can quickly arrive at the appropriate transfer function by replacing R_{load} with a general Z_{load}

$$H_{\text{crossed}}(s) = \frac{-s^2 + (1/LC)}{s^2 + (2/R_{\text{load}}C)\cdot s + (1/LC)} \tag{1}$$

$$H_{\text{parallel}}(s) = \frac{s^2 + (1/LC)}{s^2 + (2/R_{\text{load}}C)\cdot s + (1/LC)} \tag{2}$$

$$H_{\text{series}}(s) = \frac{(1/LC)}{s^2 + (2/R_{\text{load}}C)\cdot s + (1/LC)}. \tag{3}$$

As shown in the above equations, all Z-source circuit topologies have unity gain with zero phase at low frequencies. This can be understood by observing the inductor conduction path while ignoring the presence of capacitors. However, the high-frequency behaviors are different due to the dissimilar capacitor configurations.

For the crossed Z-source topology, the crossed capacitor connections create a unity gain with 180° phase at high frequencies. For the parallel-connected Z-source topology, the capacitors form a high-frequency conduction path that results in unity gain with zero phase at high frequencies. In particular, the crossed Z-source circuit transfer function resembles that of a resonator and actually amplifies perturbations near the resonance frequency. On the other hand, the parallel-connected Z-source circuit forms a notch filter at the resonant frequency. The Bode plots for the two transfer functions are shown in Fig. 5(a) and (b). The design of a filter network is generally needed for dc–dc converters to reduce electromagnetic interference and to achieve high input noise rejection at the source. Since neither of these two

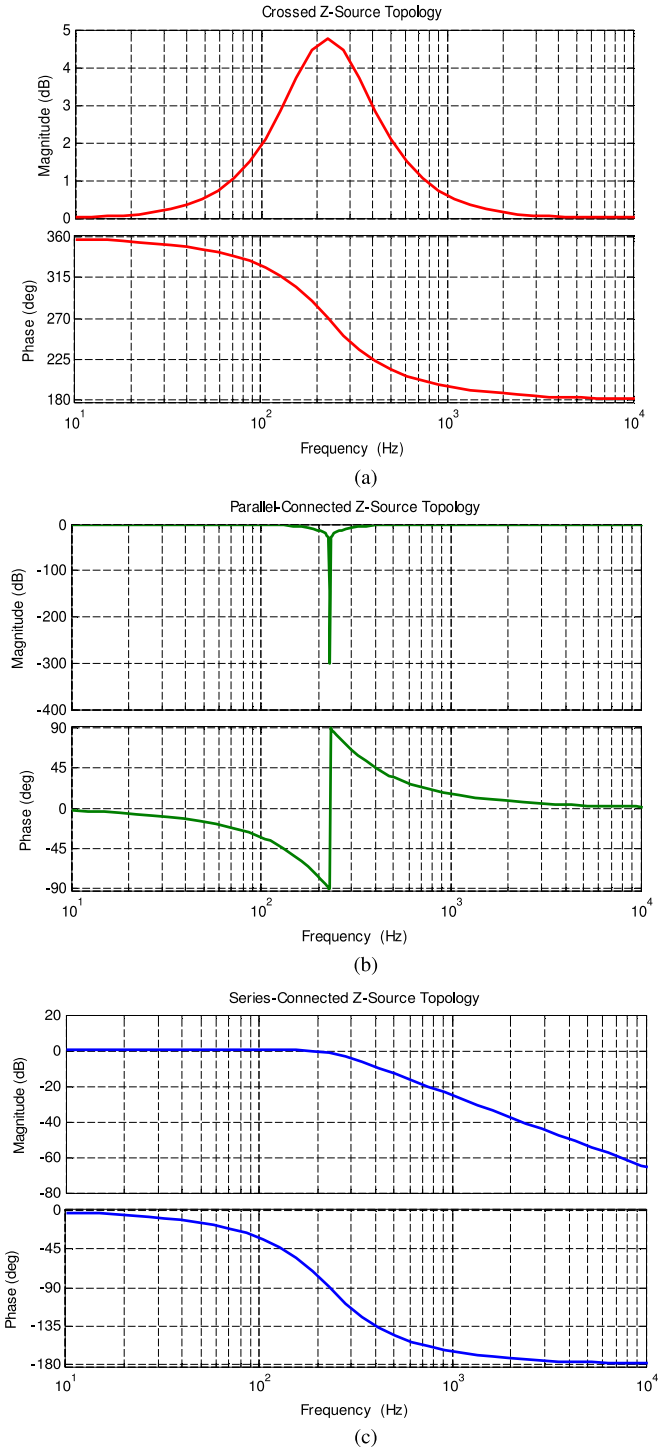

Fig. 5. Input-output voltage transfer function of the Z-source circuit breaker assuming resistive load. Component values are $R = 6\ \Omega$, $C = 200\ \mu$F, and $L = 2.4$ mH.

topologies provides any filtering capability at high frequency, when used in conjunction with downstream dc–dc converters, explicit input filters must also be designed.

The series-connected Z-source circuit has a low-pass characteristic due to the shunt capacitor placement. Specifically, the transfer function is a second order low-pass filter with a quality factor of

$$Q = \frac{R_{\text{load}}}{2}\sqrt{\frac{C}{L}}. \tag{4}$$

The Bode plot is shown in Fig. 5(c). The response is slightly underdamped using the recommended inductor sizing with a Q of $\sqrt{3}/2$ from Section III, where Z-source component sizing and Q selection will also be discussed in more detail.

Because the series-connected Z-source circuit topology offers inherent low-pass characteristic, it is possible to incorporate the input filter as part of the breaker. This allows dual-use of the Z-source passive components, as part of a circuit breaker and an input filter network for dc–dc converters, to further reduce the component count. Additional *RC* damping leg can also be introduced in parallel with the shunt Z-source capacitor, without affecting normal breaker operation, to address any potential unwanted interaction between the Z-source components and the negative effective input impedance of a regulated dc–dc converter. Having a low-pass filter function does not influence power transmission negatively as cable inductance and local energy storage capacitance already impose a low-pass characteristic in the dc power distribution system. Along with other attributes such as a common ground connection and a low reflected fault current at the source, the new series-connected Z-source circuit topology offers additional design flexibility not available in the previously proposed topologies, which may enable its use in application such as building dc power distribution systems. Table I summarizes the key differences among the three Z-source circuit breaker topologies.

TABLE I
Z-SOURCE BREAKER TOPOLOGY COMPARISON

Features	**Z-Soure Topology**		
	Crossed	*Parallel*	*Series*
Common Ground	No	Yes	Yes
Fault Current at Source	I_{SCR}	$I_L + I_C$	I_L
Z-Source Transfer Function	Resonator	Notch Filter	Low-Pass
Input Filter Integration	No	No	Yes

III. Z-Source Breaker Design Considerations

In the following sections, the transient fault response of the Z-source breaker is analyzed and a design methodology for component sizing is presented. Since the three Z-source breakers follow the same principle of operation, the following analyses are universal across the three topologies unless stated otherwise. One notable exception is the reflected fault current magnitude as previously discussed.

A. Minimum Detectable Fault Magnitude

One important metric for characterizing a breaker circuit is the minimum detectable fault current, which is defined as the minimum amount of fault current required to trip the breaker. Since the Z-source breaker consists of frequency-dependent components, the minimum detectable fault magnitude must also be frequency dependent. However, for this analysis, the minimum detectable fault current across all frequency range is desired.

Thus, an instantaneous load step is assumed for the following analysis.

For an instantaneous step transient in load current, i.e., with infinite fault conductance ramp rate, the current through the inductor leg during the fault transient can be assumed constant at the nominal load level while the Z-source capacitors and the load capacitor collectively supply the full fault current. The amount of the fault current supplied through the Z-source capacitor path can be calculated using the following capacitive divider ratio:

$$i_C = \frac{C}{C + 2C_{\text{load}}} \cdot i_{\text{fault}} \tag{5}$$

where C is the capacitance of the Z-source capacitor, C_{load} is the capacitance of the load capacitor, and i_{fault} is the fault current. Note that the in the crossed and parallel-connected Z-source topologies, the source inductance may have an effect on this ratio, whereas in the series-connected topology, the relationship is exact. Nevertheless, the impact of source inductance is small, and will be assumed to be negligible. Since the Z-source would not trip unless $i_C = i_L = I_{\text{load}}$, the minimum detectable fault current can be calculated as

$$i_{\text{fault}} = \frac{C + 2C_{\text{load}}}{C} \cdot I_{\text{load}}. \tag{6}$$

In other words, the fault conductance must be greater than the load conductance by the same factor, as illustrated in (7)

$$G_{\text{fault}} = \frac{C + 2C_{\text{load}}}{C} \cdot \frac{1}{R_{\text{load}}}. \tag{7}$$

For example, using the Z-source parameter values from the previous section, the breaker would not trip unless the fault current exceeds 11 times the nominal operating current. For slower transient faults, an even greater fault current is required because the inductor current ramps up along with the shoot-through capacitor current. Even in the limiting case where C is infinitely larger than C_{load}, the magnitude of the fault current must be at least equal to that of the nominal operating current. Therefore, the Z-source breaker offers no protection against, for example, a 20% overload condition.

The Z-source breaker offers limited longer-term overcurrent protection and is only effective in protecting against large transient faults. Thus, additional tripping mechanisms must be introduced for practical use of the Z-source breaker, as will be discussed in Section IV.

B. Minimum Detectable Fault Ramp Rate

In addition to the minimum detectable fault current, the efficacy of the Z-source breaker is also limited by a minimum detectable fault ramp rate. The minimum detectable fault ramp rate is defined as the cutoff fault ramp rate below which the Z-source breaker would not trip regardless of how large the fault eventually becomes.

The inductance of the Z-source breaker plays a part in determining the minimum detectable fault ramp rate. However, even for a Z-source breaker with infinite inductance, there exists a fundamental limit on the minimum detectable fault ramp rate determined by the load resistance, the load capacitance, and the Z-source capacitance. In order to compute this limit, the analytical expressions for the output voltage and transient Z-source capacitor current will be derived while assuming an infinitely large Z-source inductor. The size of the inductor required to asymptotically achieve this minimum detectable fault ramp rate limit will then be derived in the next section.

In this analysis, the fault conductance is assumed to ramp linearly from zero to the final fault conductance linearly with a rate of

$$K = \frac{G_{\text{fault}}}{\Delta t} \tag{8}$$

where G_{fault} is the final fault conductance and Δt is the time interval for the ramp. The fault current can then be defined using the load voltage and the fault ramp rate as

$$i_{\text{fault}} = v_{\text{out}} \cdot K \cdot (t - t_0) \tag{9}$$

for $t_0 \le t \le t_0 + \Delta t$, where t_0 is the instant of time the fault occurs and v_{out} is the output load voltage. Without loss of generality, t_0 will be assumed to be zero, so (9) simplifies to

$$i_{\text{fault}} = v_{\text{out}} \cdot K \cdot t \tag{10}$$

for $0 \le t \le \Delta t$.

Assuming the source inductance is negligible and the Z-source inductor current and the load current remain constant, the amount of fault current supplied by the load capacitor can be calculated using a capacitor divider ratio between the load capacitor and the two Z-source capacitors. Therefore, a differential equation for the output voltage across the load capacitor can be written as

$$C_{\text{load}} \frac{dv_{\text{out}}}{dt} = -\frac{2C_{\text{load}}}{C + 2C_{\text{load}}} \cdot v_{\text{out}} \cdot K \cdot t. \tag{11}$$

Solving the above equation yields the following solution for the output load voltage:

$$v_{\text{out}} = V_{\text{source}} \cdot \exp\left(-\frac{K \cdot t^2}{C + 2C_{\text{load}}}\right) \tag{12}$$

and the fault current then can be rewritten as

$$i_{\text{fault}} = V_{\text{source}} \cdot K \cdot t \cdot \exp\left(-\frac{K \cdot t^2}{C + 2C_{\text{load}}}\right). \tag{13}$$

Combining (5) and (13) yields the analytical expression for the Z-source capacitor current during the fault interval as shown in (14)

$$i_C = V_{\text{source}} \cdot K \cdot t \cdot \frac{C}{C + 2C_{\text{load}}} \cdot \exp\left(-\frac{K \cdot t^2}{C + 2C_{\text{load}}}\right). \tag{14}$$

Furthermore, the time at which the current is maximized can be solved as

$$t_{\max} = \sqrt{\frac{C + 2C_{\text{load}}}{2K}} \tag{15}$$

and the maximum Z-source capacitor current during the fault interval is

$$i_{C,\max} = \sqrt{\frac{K}{2e \cdot (C + 2C_{\text{load}})}} \cdot C \cdot V_{\text{source}}. \tag{16}$$

In order for the Z-source breaker to trip, the Z-source capacitor current must reach the level of the nominal load current through the Z-source inductors during the fault interval. In other words, the maximum Z-source capacitor current must be equal to or greater than the nominal load current. Hence, the minimum detectable fault ramp rate K must be

$$K_{\min} = 2e \cdot \frac{1}{R_{\text{load}}C} \cdot \frac{C + 2C_{\text{load}}}{C} \cdot \frac{1}{R_{\text{load}}}. \tag{17}$$

(17) is intentionally written in an expanded form to illustrate the intuition behind this fundamental limit. The product of the last two terms from (17) is equivalent to the minimum detectable conductance from (7). So the minimum detectable fault ramp rate is determined by the minimum detectable fault conductance and the time constant set by the *RC* product of the load resistance and the Z-source capacitance. Given the component values from the previous section, the minimum detectable fault ramp rate is roughly $8300\ \text{s}^{-1}\Omega^{-1}$. The Z-source breaker would only trip automatically if the actual fault ramp rate K is larger than this minimum detectable ramp rate.

The design of a dc system fault protection is dictated by the cable inductances and the capacitance of loads feeding faults. Given the rated load current, the load capacitance, and the cable inductance, the minimum detectable fault current and fault ramp rate can be designed to ensure system survivability under more severe fault conditions. For example, given the capacitance of loads feeding faults, the designer has the flexibility to choose the load-to-Z-source capacitance ratio to set the minimum detectable fault current, or the maximum tolerable fault current subject to manual detection and forced breaker commutation. Given the distribution cable inductance, the Z-source capacitance can be further increased to guarantee autonomous fault handling even when cable inductance slows down the fault dynamics. It can be seen that increasing the Z-source capacitance can improve both the minimum detectable fault magnitude and ramp rate. However, the tradeoff is not only an increased capacitor volume, but also an increased inductance requirement to achieve this fundamental limit, as will be shown in the following section. Faults that do not trip the Z-source breaker automatically can be handled with manual tripping mechanism introduced in Section IV. Note that these types of faults are of smaller magnitude and slower dynamics, which allows the system more time to respond. The minimum detectable fault magnitude and ramp rate can also be designed to avoid false tripping from load steps in the output, instead of introducing additional *RC* or *LC* legs into the Z-source breaker as discussed in [22]. For instance, by setting the minimum detectable fault ramp rate faster than any possible load step, the system is guaranteed to stay on during normal changes in the load current.

C. Z-Source Inductor Relative Sizing

Having too little Z-source inductance would not allow the Z-source breaker to achieve the minimum detectable fault ramp rate, while having too much Z-source inductance adds unnecessary cost, volume, and weight to the design. In this section, the inductor current during the fault interval will be approximated and the inductance threshold where this current becomes negligible will be derived.

In order to avoid nonclosed form solutions, i.e., error functions, the Taylor Expansions of (12) and (14) will be adopted for the following analysis:

$$v_{\text{out}} = V_{\text{source}} \cdot \left(1 - \frac{K \cdot t^2}{C + 2C_{\text{load}}} + \frac{K^2 \cdot t^4}{2\left(C + 2C_{\text{load}}\right)^2}\right) + O\left(t^6\right) \tag{18}$$

$$i_C = V_{\text{source}} \cdot \frac{C}{C + 2C_{\text{load}}} \cdot \left(K \cdot t - \frac{K^2 \cdot t^3}{C + 2C_{\text{load}}}\right) + O\left(t^5\right). \tag{19}$$

By subtracting (18) from the source voltage, the voltage across the Z-source inductor can be derived, and the inductor current can be found to be

$$i_L = I_{\text{load}} + \frac{V_{\text{source}}}{6L} \cdot \frac{K \cdot t^3}{C + 2C_{\text{load}}} - O\left(t^5\right). \tag{20}$$

Finally, combining (19) and (20) gives the current through the Z-source breaker SCR during the fault interval, as illustrated in (21)

$$i_{\text{SCR}} = I_{\text{load}} - \frac{V_{\text{source}} \cdot C \cdot K}{C + 2C_{\text{load}}} \cdot t + \frac{V_{\text{source}} \cdot K}{C + 2C_{\text{load}}} \cdot \left(\frac{1}{6L} + \frac{C \cdot K}{C + 2C_{\text{load}}}\right) \cdot t^3 - O\left(t^5\right). \tag{21}$$

(21) represents a conservative approximation in terms of the Z-source breaker operation because the capacitor current is underestimated and the inductor current is overestimated. In addition, the contribution of the inductor current relative to the capacitor current on the third order term is exposed. In order to achieve the minimum detectable fault ramp rate limit derived in the previous section, the inductor current must be negligible compared to the capacitor current. Thus, the following relationship must hold:

$$L \gg \frac{1}{6K} \cdot \left(\frac{C + 2C_{\text{load}}}{C}\right). \tag{22}$$

Plugging in $K_{\min}$ from (17) into (22) gives a minimum inductance required that would ensure the inductor current can be safely ignored for all detectable fault ramp rate K

$$L \gg \frac{1}{12e} \cdot R_{\text{load}}^2 \cdot C. \tag{23}$$

Choosing an inductor approximately ten times the limit derived in (23) gives the following expression for inductor sizing:

$$L_{\min} = \frac{1}{3} \cdot R_{\text{load}}^2 \cdot C. \tag{24}$$

(23) and (24) uncover an interesting relationship between the Z-source inductance and the load resistance. The inductance requirement can actually be relaxed as the nominal load increases, i.e., as the nominal load resistance decreases. Furthermore, it is

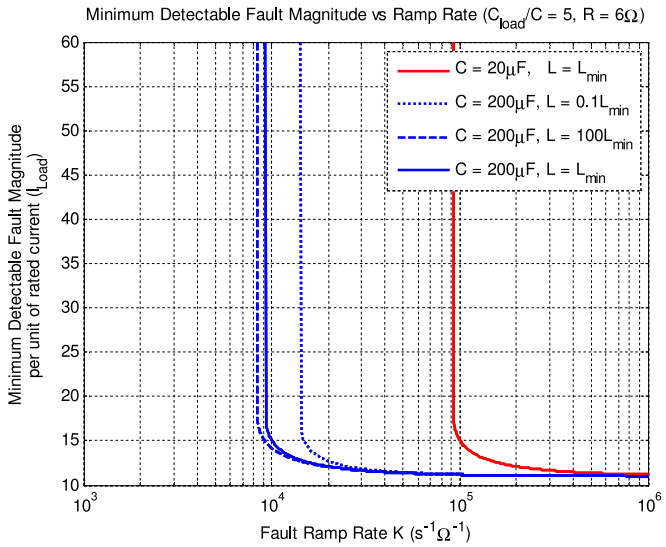

Fig. 6. Minimum detectable fault magnitude versus fault ramp rate with fixed load to Z-source capacitor ratio of 5 and a load resistance of 6 Ω.

shown that the required inductance is directly proportional to the Z-source capacitance.

Fig. 6 summarizes the relationship between the minimum detectable fault magnitude and the fault ramp rate. As expected, the minimum detectable fault magnitude increases as the fault ramp rate increases. The minimum detectable fault ramp rate is shown as the point when the required fault magnitude blows up. With the capacitor ratio fixed at 5, the minimum detectable fault magnitude at high ramp rates is expected to be 11. The effect of the absolute capacitance on the minimum detectable fault ramp rate is shown by comparing the solid blue and solid red curves.

The inductor sizing equation is verified by comparing the minimum detectable fault ramp rate using three different Z-source inductances. Very little improvement in minimum detectable fault ramp rate is achieved even when increasing the recommended inductor size from (24) by a hundredfold. Nevertheless, decreasing the recommended inductor size by a factor of ten causes a much more significant change in the minimum detectable fault ramp rate as illustrated in Fig. 6.

D. Constant Power and Resistive Loads

In the above formulation, the load current is assumed to be constant during the fault interval. However, in practical systems, a constant power load with high enough bandwidth would draw additional current as the output voltage drops. On the other hand, a resistive load would draw less current as the output voltage drops. To characterize the effect of this change in current on our analysis, the differential equation in (11) is modified to incorporate the additional current contribution

$$C_{\text{load}}\frac{dv_{\text{out}}}{dt} = -\frac{2C_{\text{load}}}{C+2C_{\text{load}}} \cdot \left(v_{\text{out}}\cdot K\cdot t \pm \frac{V_{\text{source}}-v_{\text{out}}}{R_{\text{load}}}\right). \quad (25)$$

The plus-minus accounts for both constant power load and resistive load cases. In particular, the plus sign with additional current draw corresponds to the case with a constant power load with sufficiently high bandwidth, and the minus sign with less current corresponds to the case with a resistive load.

The solution to (25) is shown as a Taylor series, again to avoid working with nonclosed form solutions and to illustrate the effect of having a finite load resistance

$$\begin{aligned} v_{\text{out}} = {} & + V_{\text{source}} \\ & - V_{\text{source}}\cdot\frac{K\cdot t^2}{C+2C_{\text{load}}} \\ & \cdot\left(1 \pm \frac{2\cdot t}{3\cdot(C+2C_{\text{load}})\cdot R_{\text{load}}}\right) \\ & + V_{\text{source}}\cdot\frac{K^2\cdot t^4}{2\cdot(C+2C_{\text{load}})^2} \\ & \cdot\left(1 - \frac{2}{3K\cdot(C+2C_{\text{load}})\cdot R_{\text{load}}^2}\right) \\ & + O\left(t^5\right). \end{aligned} \quad (26)$$

Comparing (26) and (18), the following two equations must hold so that the results derived under the constant current load assumption can be justified and applied in practical situations:

$$R_{\text{load}} \gg \frac{2\cdot t}{3\cdot(C+2C_{\text{load}})} \quad (27)$$

$$R_{\text{load}} \gg \sqrt{\frac{2}{3K\cdot(C+2C_{\text{load}})}}. \quad (28)$$

For the time period of interest, i.e., the fault interval, (27) can be written in terms of the fault resistance and the fault ramp rate

$$R_{\text{load}} \gg \frac{2}{3\cdot(C+2C_{\text{load}})\cdot K\cdot R_{\text{fault}}}. \quad (29)$$

Using the minimum detectable fault ramp rate and the minimum detectable fault magnitude, (29) can be simplified to

$$1 \gg \frac{1}{3e}\cdot\frac{C}{C+2C_{\text{load}}} \quad (30)$$

which is guaranteed to hold regardless of the actual nominal load resistance. Using the component value from the previous section, the current contribution from the change in load current is only about 1.1% of the total fault current.

A similar condition can be derived from (28) by using the minimum detectable fault ramp rate, as illustrated in (31)

$$1 \gg \frac{1}{\sqrt{3e}}\cdot\frac{C}{C+2C_{\text{load}}}. \quad (31)$$

Again, the inequality in (31) will always hold as the constant term is guaranteed to be less than one. If the Z-source capacitance is on the same order or less than the load capacitance, the current contribution from the load is constrained to about 10% of the total fault current. Using the component values before, the constant is evaluated to be 3.2%, which is negligible.

E. SCR Reverse Recovery Time

To ensure complete turn off of the SCR after a fault interruption, sufficient time must be available for the SCR to undergo its proper reverse recovery process. Specifically, the turn-off time of the SCR must be shorter than the time it takes the *LC* resonance to create a forward bias on the SCR. To the zeroth order, the available time can be approximated by the *LC* circuit resonance alone as discussed in [16].

However, the previous approach does not capture the initial conditions set by source voltage and the nominal load current. Using the series-connected Z-source breaker as an example, as the breaker responds to a fault with the SCR open-circuited and the output shorted, two sets of *LC* resonances will begin simultaneously. The series capacitor initially holds zero voltage and will be charged to the source voltage while the shunt capacitor initially holds the source voltage and will discharge through the second Z-source inductor. By symmetry, the SCR will become forward biased as the capacitor voltages reach half of the source voltage. Using the initial conditions, the available turn-off time can be calculated to be

$$t_{\text{off,max}} = \sqrt{LC} \cdot \cos^{-1}\left(\frac{2Q^2 + \sqrt{1+3Q^2}}{1+4Q^2}\right) \tag{32}$$

where Q is the quality factor as defined in (4) and captures the effects of the initial conditions by taking the load resistance into account.

The criteria in (32) provides additional considerations for sizing the Z-source inductors and capacitors. Given a system with particular a set of source voltage and nominal load current, and a SCR capable of carrying such load current and its turn-off time, the Z-source inductor and capacitor must also be sized large enough to ensure sufficient turn-off time for the SCR.

SCRs are still some of the most capable high power devices available, and SCRs that can block a high voltage and carry a large current are readily available. When scaling the Z-source breaker to higher power levels with higher rated voltage and currents, the larger SCR may require a longer turn-off time. Hence, the Z-source inductance and capacitance must be sized up accordingly. In general, if the inductance and capacitance are kept to the same order, their required orders of magnitude can be quickly estimated from the SCR turn-off time. Using the MVDC system mentioned in Section II-A as an example, an ABB 5STP 12K6500 SCR may be used. It has a peak voltage rating of 6.5 kV, an average current rating of 1.2 kA, and a turn-off time of 800 μs, which means the required inductance and capacitance can be estimated to be on the order of 800 μH and 800 μF, respectively.

To keep the overall breaker volume small, it is also possible to utilize multiple fast-switching SCR devices, which are typically only available at lower voltage ratings, to construct a fast SCR switch stack [23]. For the MVDC system mentioned above, the SCR can be constructed by a series stack of four ABB 5STF 14F2063 thyristors, which is each capable of blocking 2 kV and carrying 1.44 kA. The assembled unit can achieve a voltage rating of 8 kV, while achieving a fast turn-off time of 63 μs. This allows more than an order of magnitude reduction in both inductive and capacitive energy storage requirements.

While the above analysis was presented in the context of the series-connected topology, similar derivations can be performed for the crossed and parallel-connected topologies. As expected, these derivations would lead to the same result shown in (32), since the principle of operation is the same across all three topologies.

F. Reflected Fault Current

The amount of reflected fault current at the source is greatly reduced by adopting the series-connected Z-source topology. Nevertheless, it remains an important consideration when designing and sizing the inductors and capacitors for the Z-source breaker. It also provides additional design guidelines for input filter and energy storage requirements.

As discussed in the previous section, once a series-connected Z-source breaker has tripped after the output is shorted to ground through a fault, the *LC* circuit begins to resonate. The source-connected inductor current will continue to increase to charge up the series capacitor until the voltage across the series capacitor reaches the source voltage. Using the initial conditions, the peak source-connected inductor current can be calculated to be

$$I_{\text{source,peak}} = \frac{V_{\text{source}}}{R_{\text{load}}} \cdot \sqrt{1+4Q^2} \tag{33}$$

where Q is again the quality factor as defined in (4). The square root term can be defined as the overshoot factor. The quality factor is shown to be an important characteristic of the Z-source breaker. It not only describes the filter damping factor, impacts the SCR reverse recovery time, but also dictates the amount of source current overshoot under fault conditions. (33) can be interpreted as a sizing requirement for the Z-source inductor after selecting a Z-source capacitance. That is, the inductance must be sufficiently large to keep the quality factor low, so that the peak current overshoot does not exceed the maximum current rating of the input source.

Finally, the reflected fault current at the source for a parallel-connected breaker topology is the sum of the Z-source inductor and capacitor currents. Hence, the peak overshoot factor for a parallel-connected topology is $2 \cdot \sqrt{1+4Q^2}$, twice as large as the series-connected topology.

IV. Extended Protection Schemes

From the previous section, it is clear that the Z-source circuit breaker can only protect against faults that exceed both the minimum detectable fault magnitude and the minimum detectable fault ramp rate thresholds. These faults are the most critical type and it is an inherent advantage of the Z-source breaker that they can be handled autonomously. However, this only covers a subset of faults that can occur in practical systems. Additional detection and triggering schemes must be introduced to the Z-source circuit breaker to protect power systems from faults that satisfy only one or none of these two criteria.

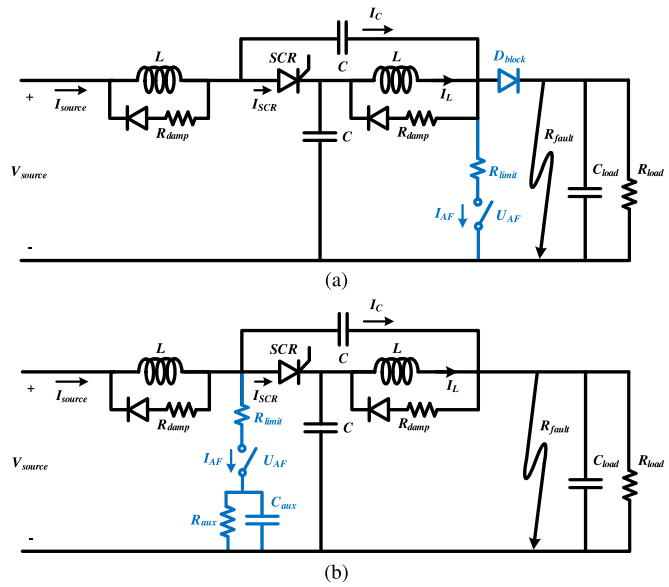

Fig. 7. Two ways of manually tripping the Z-source breaker. (a) Inducing an external artificial fault near the output and (b) inducing an internal artificial fault within the Z-source breaker.

A. Manual Tripping of Z-Source Breaker

It is possible to trip the Z-source breaker manually via an artificially induced fault current. A sufficiently large and fast artificial fault current can force current commutation of the Z-source SCR. This can be accomplished by introducing additional controlled or semicontrolled devices into the breaker topology. The main artificial fault inducing mechanism must also be able to turn off safely after the SCR commutation occurs, i.e., the artificial short must not form a direct dc path from source to ground after turning on.

Two embodiments are illustrated in Fig. 7 where the additional components for manual tripping are shown in blue. In Fig. 7(a), the artificial fault, with magnitude set by current limiting resistor $R_{\rm limit}$, is induced at the same point where a natural fault would typically occur. This will be referred to as an external artificial fault. Moreover, it would be counter-productive if the induced fault is divided between the load and Z-source capacitors—The artificial fault current must again be 11 times the nominal load current using the component values in the previous section. Consequently, a blocking diode $D_{\rm block}$ is inserted into the design.

With the blocking diode present, the required artificial fault current becomes independent of the capacitor ratio and is reduced to twice the nominal load current. This can be understood by considering an artificial current larger than the nominal load current. By KCL, the artificial fault can sink current from three places: Z-source inductor, blocking diode, and Z-source capacitor. If the artificial fault current is larger than the nominal load current, it would have steered away the full Z-source inductor current, leaving no current through the blocking diode. The remaining current of the artificial fault must then come from the Z-source capacitor conduction path. The Z-source breaker would trip if the remainder current is at least as large as the nominal load current, thus arriving at the artificial fault current requirement of twice the nominal load current.

The artificial fault inducing element $U_{\rm AF}$ can be either a power transistor or an auxiliary SCR. In this arrangement, the fault inducing element does not form a direct dc path to ground once the Z-source SCR commutates off. So the current through in the artificial fault path will naturally decay to zero, allowing the transistor implementation to be turned off safely and the auxiliary SCR implementation to turn off naturally once the current drops below the SCR holding current.

In efficiency constrained designs, the additional diode conduction loss from the blocking diode during normal operation may be seen as a disadvantage. A different embodiment of the manual tripping circuit is proposed and shown in Fig. 7(b) to induce an internal artificial fault current. In this configuration, the portion of the induced fault current through the Z-source SCR, antiseries with the nominal load current can be found to be

$$i_{\rm SCR,AF} = \frac{C + C_{\rm load}}{C + 2C_{\rm load}} \cdot I_{\rm AF}. \tag{34}$$

The capacitive divider in (34) has a minimum of one half and a maximum of one. Hence, having an artificial fault of twice the nominal load current would guarantee that the Z-source breaker can be properly tripped to isolate the source.

The artificial fault inducing element $U_{\rm AF}$ can again be either a power transistor or an auxiliary SCR. The auxiliary resistor and capacitor are introduced to prevent the fault inducing element from forming a direct dc path to ground with the Z-source inductor. When an auxiliary SCR is chosen as the fault inducing element, the auxiliary resistor is chosen so that the current $(V_{\rm source}/R_{\rm aux})$ is less than the holding current of the auxiliary SCR. The auxiliary capacitor is then used to set the duration of the induced fault interval.

During normal operation, the auxiliary SCR is turned off and the auxiliary capacitor is completely discharged by the parallel auxiliary resistor. When a fault is detected, the auxiliary SCR is turned on to draw a surge of current to force commutation of the Z-source SCR. This current drawn by the auxiliary SCR will gradually decrease as the auxiliary capacitor is charged up. Once the current level drops below the SCR holding current, the auxiliary SCR naturally turns off and the auxiliary capacitor starts to discharge through the auxiliary resistor again, resetting the trip mechanism.

Similarly, a power transistor can be used as the fault inducing element. The power transistor is turned on for a fixed amount of time to force the Z-source SCR commutation. In this case, the capacitor is chosen to set decay constant to ensure that the current through the power transistor is sufficiently small by the end of the fixed artificial fault interval, allowing the transistor to be turned off safely.

While both embodiments shown in Fig. 7 require an artificial fault current of only twice the nominal load current, i.e., the current limiting resistor should be half the nominal load resistance, a greater artificial fault current may be needed in practice. For example, any delay in the fault detection and actuation control loop translates into time for the Z-source inductor current to

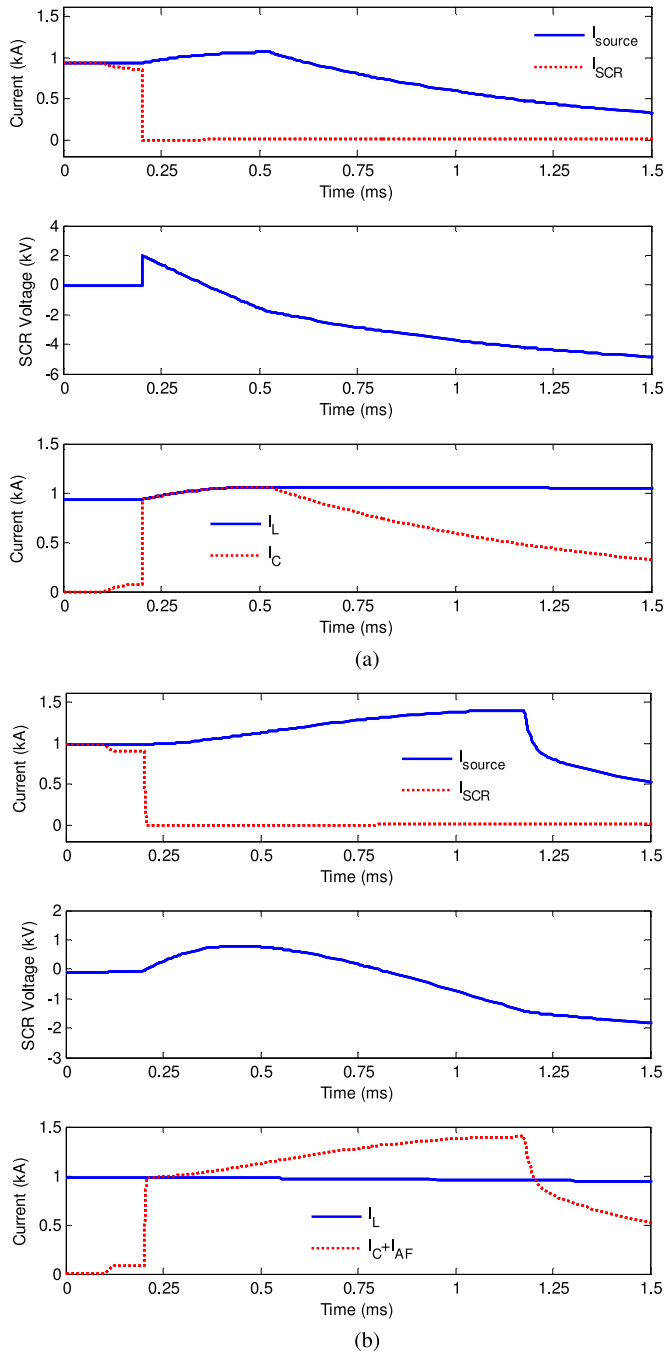

Fig. 8. Fault clearing waveforms using manual tripping methods: (a) external artificial fault current and (b) internal artificial fault current.

increase from its nominal load level, raising the amount of current required to trip the breaker.

To verify the efficacy of the two proposed manual trip modes, two simulations are presented in Fig. 8, where the waveform variables are as labeled in Fig. 7. The simulated system has a source voltage of $V_{\text{source}} = 6$ kV with a maximum load power of 6 MW, i.e., a load resistance of $R_{\text{load}} = 6\ \Omega$. The load capacitance is assumed to be $C_{\text{load}} = 1$ mF, and the series-connected Z-source topology is adopted with design values of $C = 200\ \mu$F and $L = 2.4$ mH.

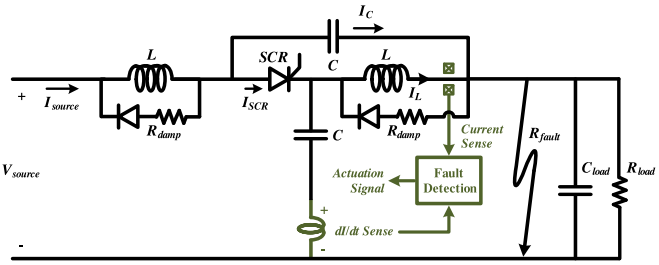

Fig. 9. Fault detection sense nodes in a Z-source circuit breaker.

In the simulation presented in Fig. 8(a), the external artificial fault inducing mechanism from Fig. 7(a) is used with a limiting resistor of $2\ \Omega$. A value less than half the nominal load resistance is used to provide some margin in case the Z-source inductor current was given time to deviate from the nominal load level. The system experiences a transient fault of $R_{\text{fault}} = 6\ \Omega$ at $100\ \mu$s, which is not sufficient to trip the Z-source breaker automatically; only a small dip in the SCR current is observed. However, by inducing an external artificial fault, the breaker can be tripped successfully to isolate and protect the source as shown in Fig. 8(a). Manual tripping occurs near $200\ \mu$s to emulate a $100\ \mu$s delay in the fault detection and actuation control loop.

Similarly, the internal artificial fault inducing mechanism from Fig. 7(b) is used in the simulated fault clearing waveforms shown in Fig. 8(b). A limiting resistor of $2\ \Omega$ is again used in this system. The auxiliary capacitor is set to be $200\ \mu$F to set the fault interval time constant to 0.4 ms and the auxiliary resistor is set to $6\ \text{k}\Omega$ to limit the turn off current to be 1 A. The system again experiences a transient fault of $R_{\text{fault}} = 6\ \Omega$ at $100\ \mu$s, and the internal artificial fault is induced at $200\ \mu$s. The sum of I_C and I_{AF} can exceed I_L in this configuration because additional current is drawn from the source as illustrated in Fig. 8(b).

B. Dual-Mode Fault Detection

With means of manually tripping the Z-source breaker, additional fault detection schemes can be incorporated to protect against the types of faults that the Z-source breaker cannot deal with autonomously. Analogous in some respects to a thermal-magnetic breaker [24], faults in the power system can be detected using two methods: dI/dt and absolute magnitude I.

Fig. 9 illustrates the points of detection within a Z-source breaker. Instantaneous current surges can be detected via dI/dt by measuring the voltage across a small inductor or a transformer winding placed in series with the high-frequency conduction path. The small sense inductor must have a much lower inductance than the Z-source inductors in order to minimize its effect on normal Z-source breaker operations. The voltage across the small inductor in relation to the linearly ramped fault current can be approximated as

$$v_{\text{sense}} = -L_{\text{sense}} \cdot V_{\text{source}} \cdot K \cdot \frac{C}{C + 2C_{\text{load}}}. \qquad (35)$$

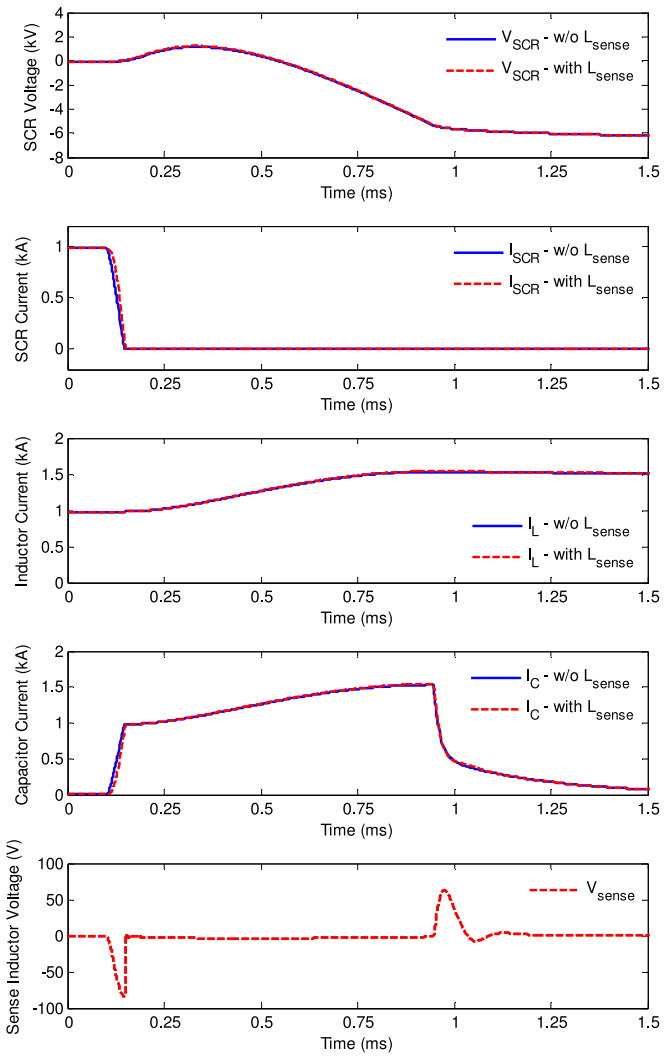

Fig. 10. Fault clearing waveforms demonstrating negligible effects from the current sense inductor on the normal operation of the Z-source breaker.

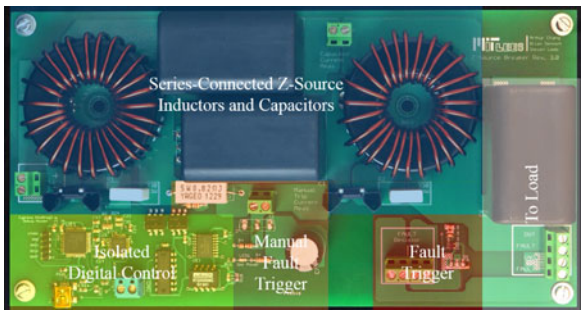

Fig. 11. Photograph of the series-connected Z-source breaker experimental prototype.

Even though the sense voltage is negative from a sense inductor, a transformer-based sensing scheme can easily flip the polarity while providing gain or attenuation as needed. Assuming the load is regulated and given the control bandwidth of the power regulator, the maximum current change rate induced by the controller is known. Any faster changing current transient should be classified as a fault, and the detection threshold can be calculated using (35).

TABLE II
DETAILED EXPERIMENTAL PROTOTYPE COMPONENTS

SCR	$I_{T\,(\mathrm{AV})}$	35 A
	t_q	35 μs
	V_{DRM}	400 V
C	Capacitance	100 μF
	ESR	3 mΩ
L	Inductance	200 μH
	I_{SAT}	31 A
R_{load}	Resistance	2.5 Ω
$Fault$	I_D	180 A
	$R_{\mathrm{DS(on)}}$	3.4 mΩ
U_{AF}	I_{TSM}	550 A
	I_H	60 mA
R_{limit}	Resistance	820 mΩ
R_{aux}	Resistance	1.2 kΩ
C_{aux}	Capacitance	20 μF

Longer-term overcurrent conditions can be detected by monitoring the current through the Z-source inductor. This can be accomplished in various manners, two of which will be discussed here. First, a high-side current sense resistor circuit can be placed in series with the Z-source inductor. This allows for accurate current reading at the cost of additional power loss and lack of galvanic isolation. Second, in power systems where efficiency is constrained or galvanic isolation is desired, a Hall effect current sensor may be used in place of the current sense resistor.

A final simulation illustrates the effect of the sense inductor and verifies the approximation in (35). The same Z-source component values are used, and the system experiences a transient fault of $G_{\mathrm{fault}} = 5\ \Omega^{-1}$ with a fault conductance ramp rate of $K = 50\,000\ \mathrm{s}^{-1}\Omega^{-1}$. Note that this fault is detectable and will trip the Z-source breaker automatically.

The simulated results shown in Fig. 10 compare the fault clearing waveforms with and without an additional sense inductor of 2.4 μH placed in the high-frequency conduction path as illustrated in Fig. 9. The sense inductor is chosen to be three orders of magnitude less than the Z-source inductor. As shown in Fig. 10, the fault clearing waveforms are nearly identical during the fault interval. The sense inductor voltage is shown to exceed the calculated value of -65 V from (35) due to higher order effects. Thus, the approximation in (35) is conservative and the detection system will not make false negative errors.

V. EXPERIMENTAL VALIDATION

A series-connected Z-source circuit breaker experimental prototype was designed and constructed to further validate the proposed breaker topology as well as the presented design equations. The low-power prototype was designed for a 490 W system with an input voltage of 35 V and a nominal load current of 14 A. In other words, the nominal load resistance is set to be 2.5 Ω. After selecting an SCR capable of carrying the nominal load current, the Z-source components are sized using the design equations in Sections II and III, and the manual trip

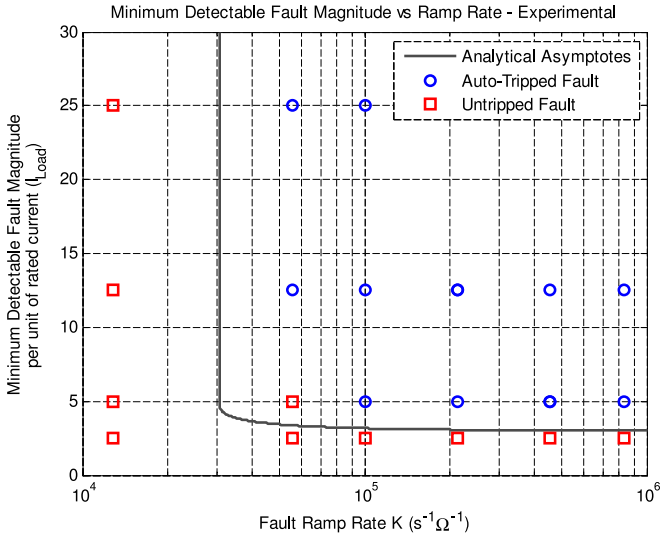

Fig. 12. Experimental validation of the calculated minimum detectable fault magnitude and the minimum detectable fault ramp rate.

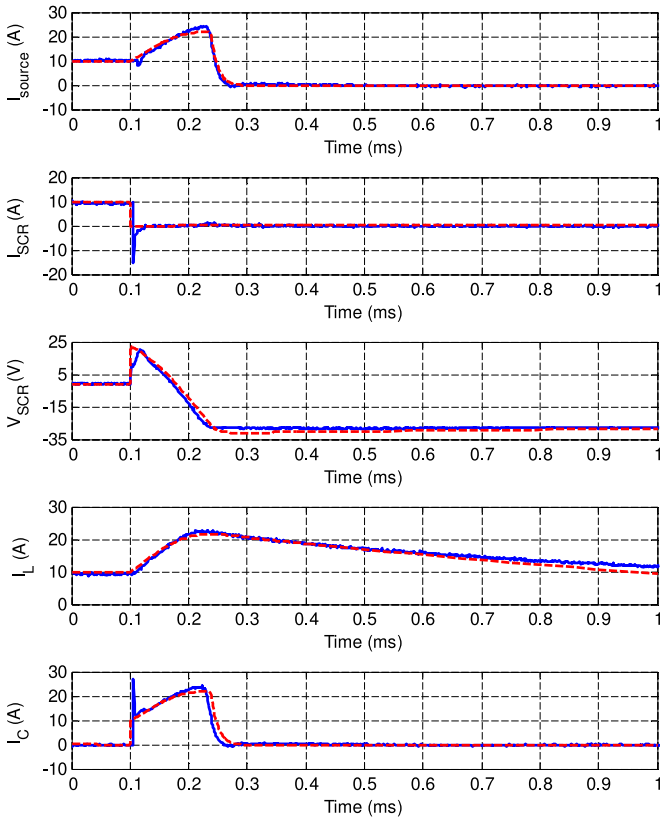

Fig. 13. Measured fault clearing waveforms (solid blue) of the series-connected Z-source breaker prototype compared to simulation (dashed red).

subcircuit is designed based on the discussion in Section IV. The fabricated experimental PCB prototype is shown in Fig. 11, and the detailed component values are outlined in Table II.

The circuit was characterized in the laboratory using an HP 6012A dc power supply. A Tektronix TDS3014B with Tektronix A6303 current probes are used to take current measurements.

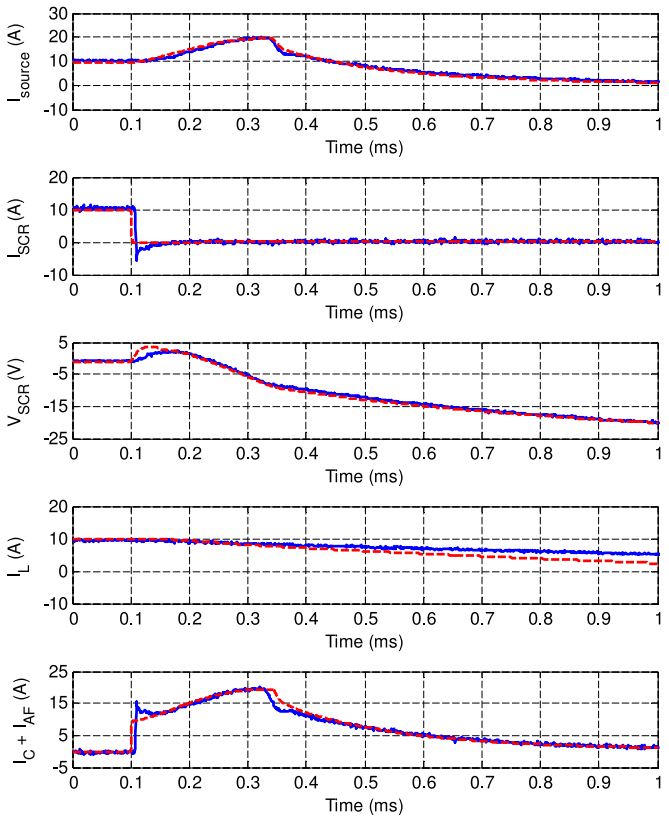

Fig. 14. Measured manually tripped waveforms (solid blue) of the series-connected Z-source breaker via an internal artificial fault current compared to simulation (dashed red).

An instantaneous fault is simulated by turning on a MOSFET switch to short out the output of the breaker. Different fault conditions are simulated by adding a fault resistor to control the fault conductance and a fault inductor to control the fault ramp rate in series with the MOSFET.

Fig. 12 validates the notion of the minimum detectable fault magnitude and the minimum detectable fault ramp rate. The manual tripping mechanism is disabled for this part of the experiment to observe whether the Z-source breaker can automatically trip on different fault conditions. The fault ramp rate K is approximated by adding a series fault inductor with an inductance of $1/K$. The experimental data points are plotted with the derived limits from Section III. The measured results match well with analytical prediction. Only one corner case in the autotrip zone failed to trip, which can be attributed to using inductors for emulating the desired ramp rates. The *RL* combination conservative approximates the fault ramp rate—The fault current ramps exponentially to the final value, which means the effective ramp rate is actually lower. With experimental validation, the derived limits provide a simple framework for designers to quickly evaluate the autonomous protection zone when designing a Z-source circuit breaker.

Fig. 13 shows the fault clearing waveforms of the series-connected Z-source breaker prototype. The measured SCR turn-off time of approximately 75 μs can be verified with (32) and the measured peak source current overshoot factor of 2.4 can be

compared with (33). The peak source current overshoot factor is larger than the calculated factor of 2.0, and the discrepancy can be explained by accounting for the inductor core material property. Specifically, the inductance factor A_L derates under large dc (amp-turn) bias condition. By including the 70% derating in the SPICE simulation, the measured and simulated results are shown to be in good agreement.

Finally, the efficacy of the manual trip mechanism is validated. The internal artificial fault current method is adopted to avoid introducing additional loss by adding an additional SCR in the main conduction path. Fig. 14 illustrates the manually tripped Z-source breaker waveforms. The measured result shows good matching compared to the SPICE simulation. The extension enables the breaker to protect against any kind of fault, not just the ones that exceed the minimum detectable fault magnitude and ramp rate.

VI. Conclusion

The Z-source circuit breaker topology has promise in protecting against faults in dc power distribution systems by creating a natural current zero-crossing. This breaker could be evaluated and modified to enable protection for all sorts of dc distribution, including renewable arrays and microgrid applications. For instance, antiparallel combinations of the presented Z-source breakers could further enable bidirectional power flow as well as bipolar circuit breaking required in many dc distribution systems, and can be investigated in future work.

This paper presents a comprehensive analysis and design methodology of the Z-source circuit breaker and proposes a new series-connected topology to maintain a common ground connection while mitigating the problem of reflected fault current at the source. In addition, with the formulation of the minimum detectable fault magnitude and ramp rate, designers can analyze the autonomous protection zone of a Z-source breaker design. In addition, the Z-source can be designed to handle normal load steps, instead of mistaking a large change in the load current for a fault. Manual tripping mechanisms along with fault monitoring methods are introduced to enable dual-mode protection against both instantaneous large surges in current and longer-term overcurrent conditions.

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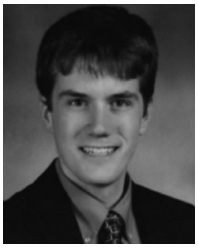

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