A Fast Analog Controller For A Unity-Power-Factor AC/DC Converter

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Abstract

This paper presents an analog implementation of a fast controller for a unity-power-factor (UPF) AC/DC converter. Unlike low bandwidth controllers associated with many state-of-the-art UPF converters, this fast controller can exercise control action at a rate comparable to the switching frequency rather than the line frequency. In order to accomplish this while maintaining unity power factor, the fast controller employs a ripple-feedback cancellation scheme. In addition to responding faster to disturbances, the controller facilitates the replacement of bulky bus capacitors with smaller, less expensive alternatives.

1 Introduction

Conventional AC/DC power converters draw a non-sinusoidal input current. Harmonic content in a current waveform flowing through the impedances in the electric utility distribution system can create harmonic voltages that interfere with other electrical equipment connected to the same electrical service [1], [2], [3]. In addition, a distorted current waveform prohibits the extraction of the maximum possible real power from the utility service. Unity-Power-Factor converters are designed to overcome these shortcomings. Typical control schemes employed in state-of-the-art UPF converters have fairly low bandwidth in order to limit the impact of output voltage ripple on the control loops. In such controllers, disturbances are attended to by control actions taken at most on the order of twice per line cycle.

The fast controller presented here exercises control action at a much faster rate. As a result, the fast controller achieves a much smaller response time to disturbances. A key feature of this controller is its ability to reject feedback of the ripple on the bus capacitor by actively canceling it, so that high-bandwidth control can be maintained without distorting the input current. This facilitates the replacement of expensive and bulky bus capacitors used in conventional UPF converters with smaller and less expensive capacitors, thus saving valuable circuit board space and reducing the overall size and cost of the power converter.

A large-signal periodically-varying *linear* model of a UPF boost converter serves as the basis for the design of the fast controller. The large-signal linear model permits reliable, well-characterized control action in the presence of large deviations from a nominal operating point, as opposed to controllers designed on the basis of a small-signal model.

2 Background

A popular scheme for implementing a UPF utility interface is based on a boost preregulator, as shown in Figure 1.

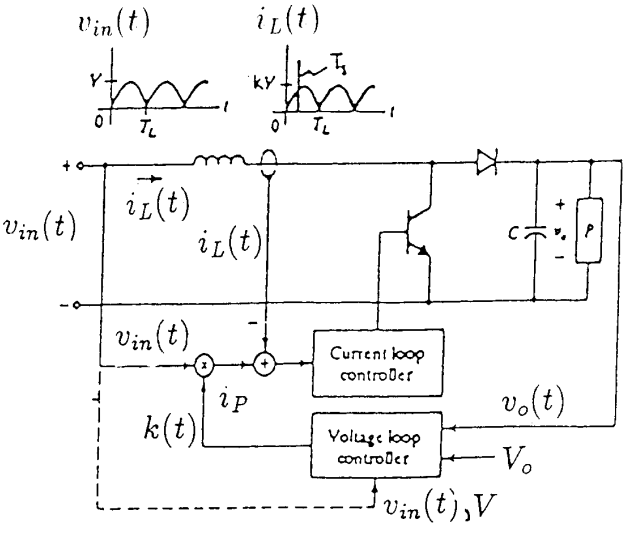

Figure 1: A Unity-Power-Factor AC/DC switching preregulator [4].

The current loop or inner loop controls the inductor current (input current) to the shape and phase of the input voltage, $v_{in}(t) = V \mid \sin(\frac{\pi t}{T_L}) \mid$. The switching sequence for the transistor forces the local average of the inductor current $i_L(t)$ to essentially equal the commanded current $i_p(t)$. The current $i_p(t)$ is in turn made proportional to the input voltage, $i_p(t) = k(t)v_{in}(t)$. The voltage loop or outer loop in state-of-the-art UPF converters regulates the av-

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erage output voltage, $v_o(t)$, around a *constant* reference voltage, V_o, by appropriately adjusting $k(t)$ to vary the amplitude of the commanded current, and hence the input current. The variation in $k(t)$ typically occurs at the maximum rate of once per rectified line cycle [5]. The fast controller designed and implemented here instead regulates the *instantaneous* voltage around an appropriate *periodically varying* reference, with $k(t)$ allowed to vary significantly within each cycle.

3 System Modeling and Control Design

As outlined in [6], the modeling of the UPF converter is based on a power balance equation that assumes the current loop is working ideally (i.e. $i_L = i_p$) and ignores the ripple at the switching frequency. This power balance equation is

$$\frac{1}{2}C\frac{dv_o(t)^2}{dt} = k(t)v_{in}^2 - \frac{1}{2}L\frac{d(k^2(t)v_{in}(t)^2)}{dt} - P \quad (1)$$

where we have assumed a constant-power load, P. An additional resistive load is easily incorporated into the modeling, but is omitted here. Equation (1) in effect involves variables averaged over the switching period T_S and is referred to as a T_S-averaged model. To transform it to a state-space form, we define a state variable to be

$$y(t) = v_o^2(t) + \frac{L}{C}k^2(t)v_{in}^2(t) \quad (2)$$

Substituting this choice of state variable in (1) results in a state-space model that, although periodically-varying, is *linear* :

$$\dot{y}(t) = \frac{2v_{in}^2(t)k(t)}{C} - \frac{2P}{C} \quad (3)$$

The energy stored in the inductor is typically small compared to the energy stored in the capacitor. As a result, $y(t) \approx v_o^2(t)$, and we can make the approximation that the nominal or desired trajectory, $Y_d(t)$, for the quantity $y(t)$ can be expressed in terms of a desired output voltage waveform $v_{od}(t)$:

$$Y_d(t) \approx v_{od}^2(t) \quad (4)$$

If a constant average output voltage V_o is desired, it can be shown [6] that

$$Y_d(t) \approx V_o^2 - \frac{2P}{C\omega_2}\sin(\omega_2 t) \quad (5)$$

where ω_2 is the output ripple frequency (twice the line frequency) given by $2\pi/T_L$, with T_L denoting the period of the rectified line input. With the T_S-averaged model, therefore, the nominal output voltage is not just a DC term. Instead, the nominal output consists of a desired DC voltage, V_o, plus an unavoidable AC ripple due to the finite size of the bus capacitor.

One approach to the compensation of a time-dependent system is to choose feedback gains that vary with time, so that the overall closed-loop system is time-independent. For the UPF boost converter we propose the control law $k(t) = \tilde{k}(t) + K$. The term $\tilde{k}(t)$ serves to respond to deviations in the output voltage and to cancel out the time-varying term in (3):

$$\tilde{k}(t) = -\frac{C}{2v_{in}^2(t)}b\tilde{y}(t) \quad (6)$$

where $\tilde{y}(t) = y(t) - Y_d(t)$ and b is a constant selected by the designer to achieve a desired closed-loop transient response. The feedforward component K guarantees unity power factor in the steady state, and is given by

$$K = 2P/V^2 \quad (7)$$

where $V^2/2$ represents the RMS input voltage. Substituting this choice of $k(t) = \tilde{k}(t) + K$ into Eq.(3) yields a closed-loop system governed by the linear and time-invariant equation:

$$\dot{\tilde{y}}(t) = -b\tilde{y}(t) \quad (8)$$

Schemes in which (1) is averaged over the line cycle T_L and where $k(t)$ is assumed essentially constant over a cycle, [5], yield controllers that have inherently lower achievable closed-loop bandwidths than are possible with the fast controller. The fast controller, which incorporates a periodically varying feedback gain, can achieve orders of magnitude decreases in the transient response time.

4 System Overview

Figure 2 shows a block diagram of the UPF converter with the fast controller. Box 1 contains the blocks that represent the T_S-averaged state-space model (3) of the converter. The sequence of blocks in Box 2 takes as input the error $\tilde{y}(t)$ and computes $\tilde{k}(t)$, the periodically varying feedback gain that yields a time-invariant closed-loop system. Fast response to disturbances is achieved through careful selection of the constant b. In addition to $\tilde{k}(t)$, the controller computes the constant K of (7) from a feedforward estimate of the load power (Box 3) and a feedforward measurement of the RMS input voltage, making the controller insensitive to changes in both. The constant K is computed to guarantee UPF operation in the steady-state.

The fast controller employs active cancellation to prevent feedback of the ripple voltage on the bus capacitor. The computation indicated in Box 4 deter-

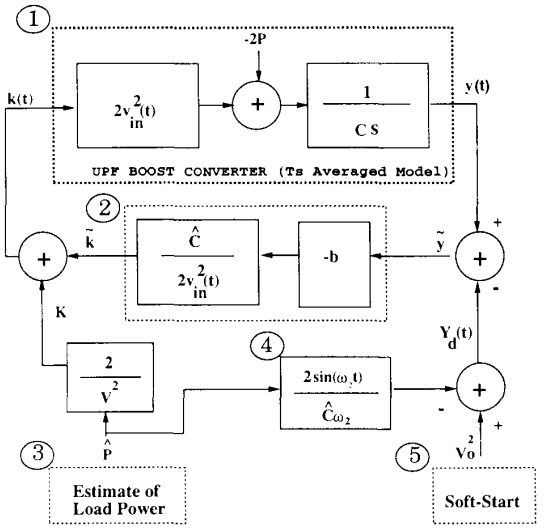

Figure 2: Block diagram.

mines the nominal trajectory for $y(t)$ according to Eq. (5).

Finally, the controller requires a DC reference, shown in Box 5, to set the DC component of the desired output voltage, i.e., V_o in Eq. (5). The hardware prototype, to be discussed in detail in the next section, incorporates a soft-start circuit to gradually build the DC component of the desired output voltage during the turn-on transient. This soft-start protects components in the boost converter from excessive stress during startup, when the controller is correcting for a large initial error.

5 Implementation Overview

A hardware prototype of the fast analog controller has been constructed and tested [7]. For convenience in developing the prototype, the inner current loop and parts of the outer voltage loop were implemented with a Unitrode integrated PFC controller chip (UC3854) [8]. While not intended to serve as a fast UPF controller, a UC3854 can be augmented with additional circuitry to implement a fast analog controller. Our prototype serves, therefore, not only to illustrate the performance of the fast controller in practice, but also to show how useful customizations may be made to off-the-shelf commercial components.

The hardware implementation of Block 1 in Figure 2, with $k(t)$ as input and $y(t)$ as output, is realized in the prototype with a UC3854 power factor correction IC and a 250 Watt boost converter circuit. On the input side, the UC3854 incorporates a multiplier block that computes the current reference $i_p(t)$ for the inner current loop from a scaled measure of the input voltage and the output of the fast controller, $k(t)$. The output of the IC directly controls the semiconductor switch in the boost converter.

As mentioned previously, the fast controller utilizes a periodically varying feedback gain to counteract the time-varying component of the T_S-averaged model of the UPF converter. This gain, shown as the output of Block 2 of Figure 2, is primarily calculated outside of the UC3854 by squaring a measure of the line voltage and using an analog divider to compute the reciprocal. Final scaling of this time varying term is completed inside the UC3854, which scales its input command by dividing by the square of the RMS input voltage.

Equation (1) assumes a constant-power load at the output of the converter. This assumption is reasonable with the UPF preregulator because a UPF converter is often employed in a system in which the load comprises one or more regulated switching power supplies. In testing the actual implementation, a resistive load was used for convenience. As noted earlier, a resistive load could have been incorporated into the analysis and design, but was not. The satisfactory performance of our controller reflects the robustness to load model assumptions, and is partly the result of the controller using a measured load power. In order to calculate the load power (Block 3 of Figure 2), the average load current was calculated by measuring the voltage across a current-sense resistor in series with the resistive load. The load power was then calculated by multiplying the load current with a scale factor representing the average load voltage.

The ripple on the output voltage is essentially sinusoidal with a frequency of 120Hz, corresponding to double the line frequency. The fast controller prototype uses a convenient estimate of this ripple to actively cancel out its distorting effect on the input current in the steady state. The sinusoid required to generate the ripple component of Y_d in (5), see Block 4 of Figure 2, is realized by squaring a measure of the 60Hz line voltage, eliminating the DC offset, and then using an all-pass filter to ensure the correct phase.

The fast controller also incorporates a soft-start mechanism during the initial startup transient, when the error between the desired voltage and the actual voltage is large. The key features of Block 5 in Figure 2 include:

- A voltage reference, derived from an internal precision reference available on the UC3854, that sets the desired steady-state bus voltage.
- An additive offset signal that accounts for the rectified line voltage present on the boost bus capacitor before boost operation can commence.
- An RC circuit with a gradually rising output voltage that sets the reference during the startup transient. The RC circuit is used in conjunction with a diode clamp that ultimately locks the reference at a steady-state value.

A simulation of the startup transient incorporating a soft-start mechanism and current limiting is shown in Figure 3. The initial distortion in the current is due to the periodically varying term in Block 2 in the feedback loop of the fast controller. During a transient, with a nonzero $\tilde{k}(t)$, the commanded current will contain a time varying term that distorts its shape. Empirical results from the hardware prototype are presented in the next section.

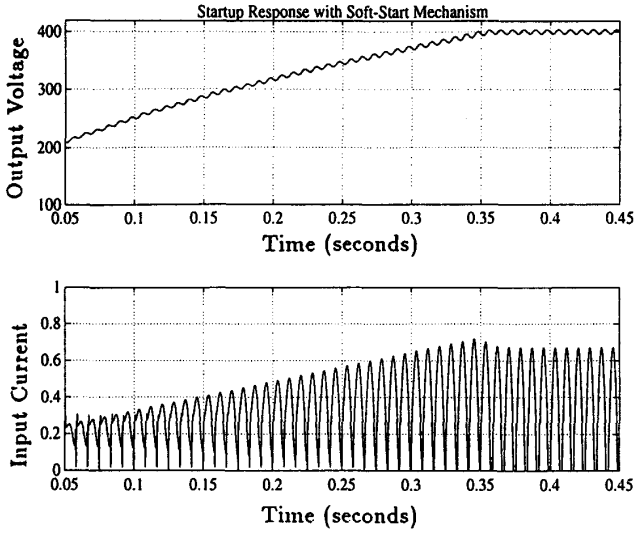

Figure 3: Simulated startup transient with soft-start and current limiting.

6 Experimental Results

The component values used in the boost converter in the prototype are $C = 47\mu F$, $L = 1mH$. The input voltage to the converter during the tests described in this section was $v_{in}(t) = 165 \mid \sin(\frac{\pi t}{T_L}) \mid$, with $T_L = 8.333ms$. The steady-state voltage reference was set to provide a nominal output voltage of $V_o = 350V$ to a resistive load. The performance of the prototype was examined during two different transient conditions: a startup transient and a doubling in load power.

The experimental UPF converter was activated in our experiments by first energizing the mains supply to the boost converter. With no active control, the output voltage rises to slightly under the peak input voltage, and the input current to the boost converter is, of course, noticeably distorted. The fast controller was then activated, and the output voltage regulated by the controller to the desired $350V$. As expected, the input current in steady-state is in phase and of the same shape as the input voltage. Figure 4 shows the startup response of the fast controller. The input current (lower signal) rises gradually to a steady-state value of approximately $.4A$ peak. The load voltage (top signal) rises to the desired steady-state voltage of $350V$.

Figure 5 shows the response of the controller to an approximate doubling of the load power. The voltage starts to dip while the controller commands more current to match the new output power requirement. The maximum current during this transient is approximately $.7A$ peak. As expected, the ripple on the output voltage is higher at the new power level.

The fast controller only ensures a distortion-free input current waveform during steady-state operation. This is better illustrated in Figure 6 which shows that, before and after the transient, the current is of the same shape as the input voltage, whereas during the transient, it is distorted. In the steady-state, $\tilde{k}(t)$ is zero and the input current is a scaled copy of the input voltage.

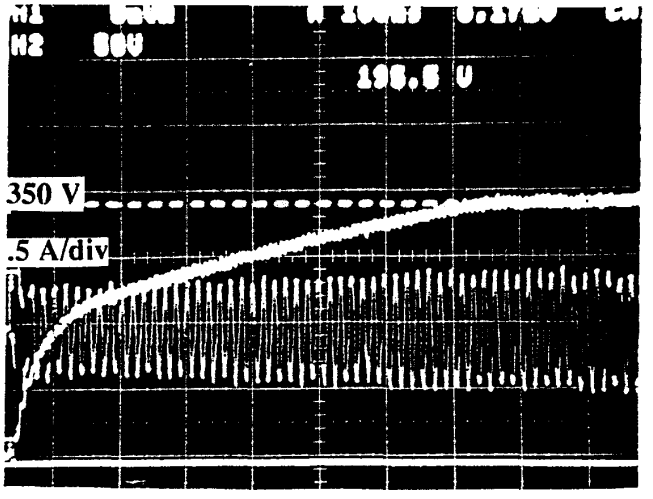

Figure 4: Startup transient in fast analog controller.

A point of interest in these experiments is the size of the bus capacitor. The relatively small bus capacitance incorporated in the prototype is not a problem for the fast controller because its active ripple feedback cancellation scheme allows the controller to prevent the feedback of the output voltage ripple. The insensitivity of the fast controller to output voltage ripple permits good regulation of the DC component of the output voltage even with very small bus capacitors. By enabling the use of a small bus capacitor, the fast controller can potentially reduce the overall cost of a UPF converter.

Unlike classical linear time-invariant (LTI) controllers, the fast controller employs a periodically varying feedback gain and a feedforward estimate of the load power. In principle, the fast controller can achieve zero steady-state error in the output state variable $y(t)$. However, the fast controller is sensitive to computation errors in the feedback gain and also to measurement errors in the feedforward estimate of the load power. Inaccurate measurements could re-

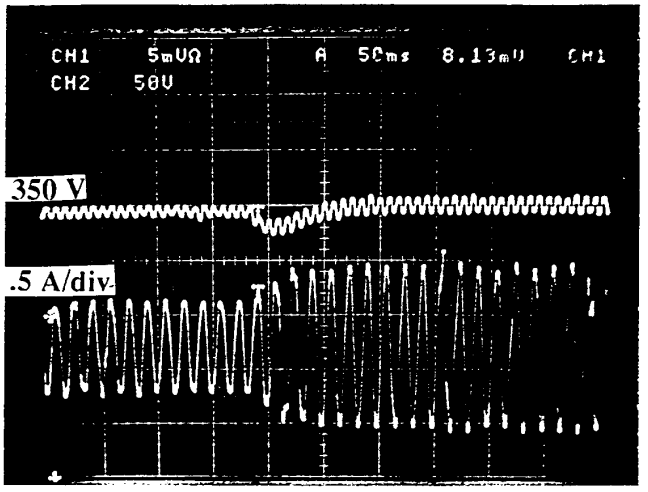

Figure 5: Response of fast controller to doubling of load power.

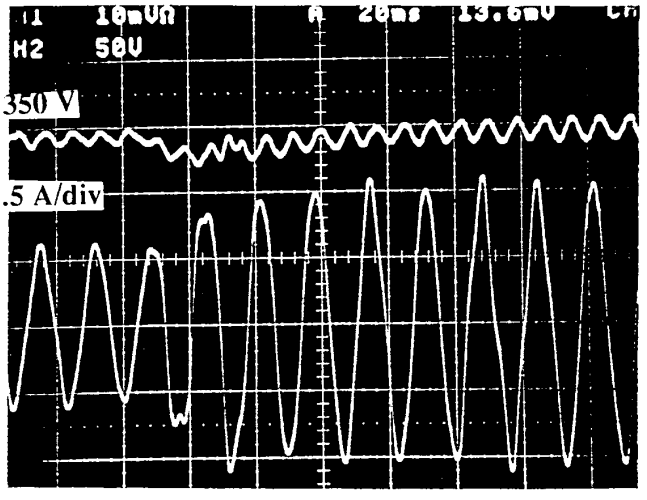

Figure 6: Distortion of input current during doubling of load power.

sult in an erroneous Y_d, since the ripple component will not match the ripple on the output voltage, causing the controller to regulate the output voltage to an incorrect "desired" trajectory. More importantly, this represents a transient state for the controller in which the input current is distorted due to the periodically varying gain. As a result, unity power factor would be compromised. An alternative solution would be to regulate the DC component of the output voltage with an appropriate LTI compensator, such as a proportional-integral controller, to guarantee zero steady-state error, and to use a second faster control loop to regulate the ripple on the output voltage.

7 Conclusion

In this paper, we have presented a novel control scheme designed on the basis of a periodically-varying, large-signal linear model of a unity-power-factor AC/DC converter. The prototype presented here employed a controller with a periodically varying feedback gain and a feedforward estimate of the load power, and demonstrated fast response to load disturbances. The fast controller's unique ability to reject the feedback of the bus capacitor ripple facilitates the reduction of the output bus capacitor. As a result, a cheaper, smaller UPF boost converter with superior transient response could replace many current designs.

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