A Systems Approach to Photovoltaic Energy Extraction

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***Abstract*—Per-panel photovoltaic energy extraction with integrated converters can increase overall array tracking efficiency. Also, switched-capacitor (SC) converters have been evaluated for many applications because of the possibility for on-chip integration; applications to solar arrays are no exception. This paper presents a comprehensive system-level look at solar installations, finding possibilities for optimization at and between all levels of operation in an array. Specifically, this paper examines new arrangements and options for applying switched-capacitor circuits at 3 levels: for the panel and sub-panel level, as part of the overall control strategy, and for ensuring stable and robust interface to the grid with the possibility of eliminating or reducing the use of electrolytic capacitors.**

Keywords- photovoltaic (PV) array, PV module, manufacturing I-V mismatch, MPPT, switched-capacitor (SC), multilevel, dc-dc power converters, common centroid, grid-tie inverter, stability

I. Introduction

Asymmetries in a PV string caused by temperature variation, dirt, panel aging, panel orientation, and other factors can negatively impact tracking efficiency. To maximize energy extraction, distributed power conversion is employed to enable per-panel or sub-panel maximum-power-point tracking (MPPT) [1-9]. There are essentially three common architectures deployed in residential and commercial PV installations for delivering power to the grid: string inverter, micro-inverter, and DC-DC series power supplies working in concert with a string inverter [1-3]. Each has limitations that can be overcome by the proposed approach presented here [12].

For example, these approaches are typically constructed with magnetic components, possibly purchased on a per-panel basis. Even at high switching frequencies where magnetic component size can be minimized or eliminated by using air core or parasitic wire inductance, these components constrain manufacturing cost. High frequency switching may also complicate electromagnetic interface created by the distributed converters, as the frequencies approach allocated FCC bands.

The drive to miniaturization has renewed interest in capacitor-based switching power conversion due to higher energy storage density of capacitors compared to inductors [10]-[11]. It was then proposed and shown in [12] that outstanding MPPT and overall system efficiency can be achieved using a modified version of the DC-DC module integrated converter, where the DC-DC converters are switched-capacitor converters that can only achieve integer or rational multiples of the input voltage from a photovoltaic module. This approach may be cost-attractive and physically rugged because it requires no per-panel magnetic components. A system level overview of this approach is shown in Figure 1, where each PV element can represent either a PV cell, sub-module PV string, or a PV module.

Switched-capacitor MICs may not be most efficiently deployed as current sources contributing to the string. However, in contrast to the typical DC-DC MICs that operate with local autonomous MPPT control, the proposed system shares the responsibility of MPPT with one centralized inverter. Specifically, the central inverter can be input-current-controlled so that it appears as a current sink to all the MICs in the string. The load current can then be scaled by the module-level converter to become a scaled current sink at the sub-module levels.

This paper explores the efficacy and examines the enhancements of applying this system architecture at all levels in the array: for the panels, for the overall control, and for the interface to the utility. Measurement results of an experimental MIC prototype built from the analysis in [12] are presented in Section III. Finally, stability analysis, additional considerations and optimizations in the grid-tie inverter interface with SC DC-DC MICs are discussed in Section IV.

II. Sources of Variation in a PV String

The different types of variations that cause asymmetries in a PV string can be broadly classified into two categories: process variation and external operating condition.

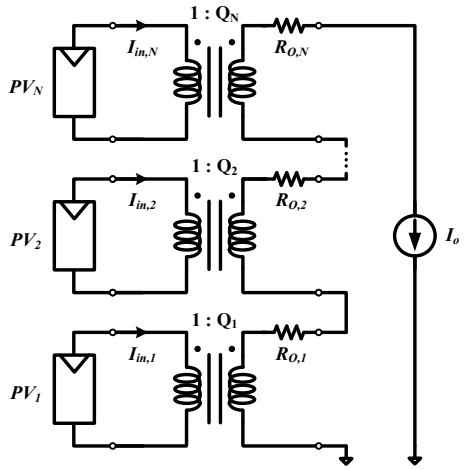


Figure 1. Linearized discrete conversion ratio integrated converter model.

Process variation in the solar industry typically refers to manufacturing I-V mismatch between solar cells. Low-level solar module construction faces similar tracking efficiency challenges as high-level solar array assembly. Solar cells that are connected in series must all carry the same current. Thus, they do not perform at their individual maximum power points. Instead, they operate at a collective maximum that is limited by the mismatch between cells within the module. The tracking efficiency at the cell level, also known as the mismatch factor, can be defined as

$$\eta_{p,cell} = \frac{P_{collective,max}}{\sum P_{i,cell,max}}. \quad (1)$$

In order to reduce the amount of cell-to-cell variation and increase the cell tracking efficiency, the solar panel manufacturers have invested greatly in improving their manufacturing process as well as evaluating different cell binning algorithms [13]-[14]. In the past ten years, the manufacturers have refined their production process and reduced the power tolerance from ±10% down to ±3% [15]. However, it is worth noting that current and voltage parameters can have higher tolerance in the case of sorting by maximum power as manufacturers typically sort the cells into different power bins to sell at different price points. Finally, recent work has also investigated optimal series-parallel layout configuration to maximize the output power of PV modules at a given confidence level [16].

External operating conditions consist of environmental factors including irradiance level, shading, temperature variation, dirt collection, panel aging, and panel orientation. Unlike process variation, which is tightly controlled in the manufacturing process, environmental factors can introduce large systematic imbalance (panel aging, panel orientation) or can unpredictably change the individual solar module's maximum power point substantially (irradiance level, shading). For example, shading of a solar module can change a module's maximum power by as much as 100%. In addition, in a residential installation, panels may be placed on both sides of the roof, meaning that panels have two distinct orientations and thus a systematic irradiance level difference throughout the day. Finally, panel age and dirt collection may cause asymmetry between existing and newly-installed panels. These factors are particularly relevant to residential installations where owners only purchase a portion of the panels upfront and plan on acquiring additional panels to increase the power output in the future.

A. Cell-Level Integrated Converters

At the sub-module cell level, the solar cells are closely spaced such that their external operating conditions are highly correlated and can be approximated as being nearly identical. Thus, the dominant source of asymmetry arises from the process variation between the cells in a sub-module string. Even though power tolerance can be limited down to ±3%, I-V mismatch can have higher tolerance when cells are sorted by maximum power. To study the effectiveness of a switched-capacitor DC-DC integrated converter at the cell level, a conservative maximum-power current variation of ±5% is assumed for the following discussion.

A first-order approximation for maximum power point tracking assumes that the cell output is step-wise linear when its output current is slightly perturbed around the maximum-power current. That is, if the current deviates from the maximum-power current by a small percentage ϵ, the output power is reduced from the maximum power by the same percentage.

$$I_{cell} = (1 - \epsilon) \cdot I_{mp} \quad (2)$$

$$P_{cell} \simeq (1 - |\epsilon|) \cdot P_{max} \quad (3)$$

In the case where the cell maximum-power current varies by up to ±5%, an overall tracking efficiency above 95% is expected; that is, the sub-module string current can be set to the average maximum-power current so that it is always within 5% of each cell's individual maximum-power current.

To increase tracking efficiency, finer conversion levels must be added to tune individual cells' current closer to their maximum-power current. Since cell-level variations are typically tightly constrained and voltage level is low, a relatively simple fully-integrated SC circuit can be used to provide a fractional step in both positive and negative directions. At the cell-level, simplicity is a benefit in minimizing integrated converter cost. The choice of the tuning step-size is illustrated in Figure 2 assuming uniform distribution and maximum allowable maximum-power current variation of δ around the norm. The entire space is quantized into 3 equally sized intervals of size $2\delta/3$ and the discrete tuning steps can be found as the center of each interval $\{1 - 2\delta/3\,, 1, 1 + 2\delta/3\,\}$.

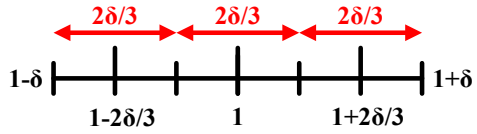
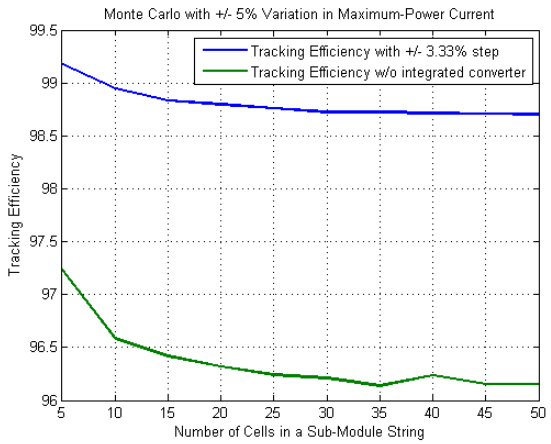


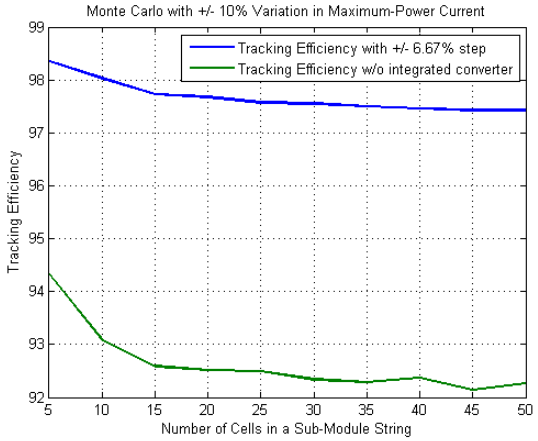
Figure 2. Cell-level integrated converter quantization steps.

Monte Carlo simulation results using the methods presented in [12] are shown in Figure 3a. As expected from our approximation, the tracking efficiency with no integrated converter is slightly above 96%. With the introduction of integrated converters with discrete ±3.33% steps, an overall tracking efficiency greater than 98.33% is expected. The simulation results again agree with the intuitive model, and the tracking efficiency improves to above 98.7%. Potentially the greatest value in integrating converters at the cell-level lies in the fact that the added degrees of freedom allow the currently extensive and stringent binning process to be relaxed during manufacturing. Therefore, it is possible to lower the production cost of the solar panel itself and may open doors for a paradigm shift in the manufacturing process.

Consider the following example with the maximum allowable maximum-power current variation doubled from the previous case to ±10%. The simulation is repeated with a new optimal step-size of ±6.67% and the results are shown in Figure 3b. The tracking efficiency of the relaxed binning process with integrated converters (97.5%) is shown to exceed that of the stringent binning process without integrated converters (96.2%). Furthermore, assuming a 98% conversion efficiency for the switched-capacitor circuit, the overall efficiency of the relaxed binning process with integrated converters becomes 95.6%. Thus, even when taking into account conversion



(a) ±5% variation in maximum-power current



(b) ±10% variation in maximum-power current

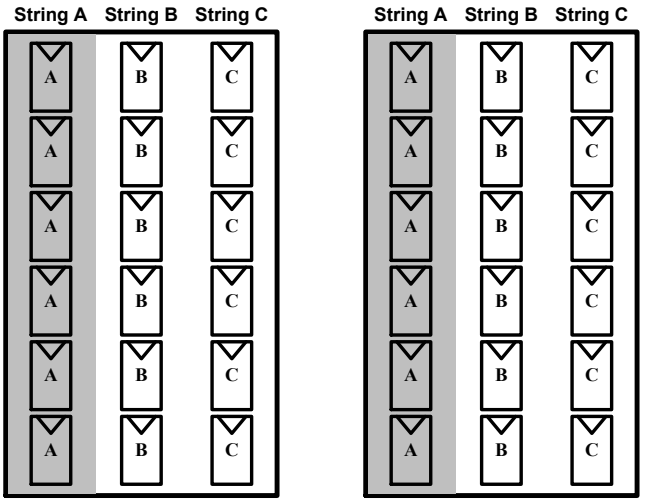
Figure 3. Cell tracking efficiency with and without integrated converters using different binning tolerance.

efficiency, the cost effective switched-capacitor integrated converters approach presents minimal power loss compared to stringent binning process while offering a great opportunities in reducing the manufacturing cost of the solar panels.

B. Sub-Module String Level Integrated Converters

A group of solar cells are connected in series to form a sub-module string. Given small variations among each cell's maximum-power current, the overall maximum-power current of the sub-module string can be well-approximated as the arithmetic mean of the individual cells' maximum-power currents. Assuming the maximum-power current for the cells are *i.i.d.* with mean μ and variance σ^2, the overall maximum-power current of the sub-module string will roughly have a mean μ and a variance σ^2/N, where N is the number of solar cells in the sub-module string. Therefore, for reasonably sized sub-module strings, the asymmetries can be attributed entirely to the external operating conditions.

Since the sub-module strings are closely spaced, their statistical variations must be correlated. In particular, external operating conditions such as temperature, dirt collection, aging, and orientation are for all intents and purposes identical



(a) Typical sub-module string layout (b) Common centroid string layout

Figure 4. Imbalance between sub-module strings caused by partial shading.

because the strings occupy the same solar panel. Thus, the variability of the maximum-power current is expected to be constrained, which would limit the required tuning range of the SC integrated converter for a target tracking efficiency and thereby reduce cost. However, given the current sub-module string layout employed by the manufacturers, partial shading can cause substantial mismatch between sub-module strings. Such a situation is illustrated in Figure 4a, where a panel with typical sub-module string layout is affected by partial shading, or a 1-D "hard" gradient, in the direction orthogonal to the string orientations.

Common centroid layout is effective in reducing gradient-induced mismatches [17]. Utilizing such a technique in a solar panel layout would help substantially reduce the amount of mismatch caused by an imbalance in solar irradiance between the sub-module strings. Note that a custom layout requiring stringent parasitic control is not necessary; instead a simple PCB with the common centroid routing pattern is sufficient. An example of such layout is shown in Figure 4b. In the common centroid case, the power between the sub-module strings will remain symmetric with the same partial shading as before and will remain relatively balanced given other linear shading patterns as well.

A statistical evaluation method was adopted to simulate the effect of linear irradiance gradient. For each iteration in the simulation, a random linear shading pattern is generated. Each string's respective power is computed and the standard deviation of the string's maximum power is recorded. As shown in Figure 5, the common centroid layout is very effective in compressing the standard deviation to below the power of a single solar cell. Furthermore, since the standard deviation is kept below the power of a single solar cell, the power variation between strings is expected to decrease inversely proportional to the number of power generating cells per string. To verify this hypothesis, additional simulations of 3 strings with 6 cells are performed to characterize the percentage power variation between the maximum and minimum power strings vs. the output power of the maximum power string. As shown in Figure 6, while the normal string

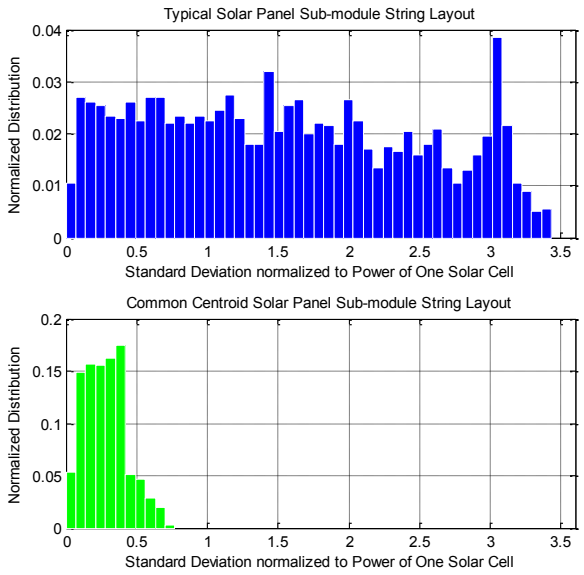


Figure 5. MATLAB simulation results comparing the two layout schemes shown in Figure 4. Simulated standard deviation distribution (normalized to the maximum power of one solar cell) of maximum power for 3 strings of 6 cells.

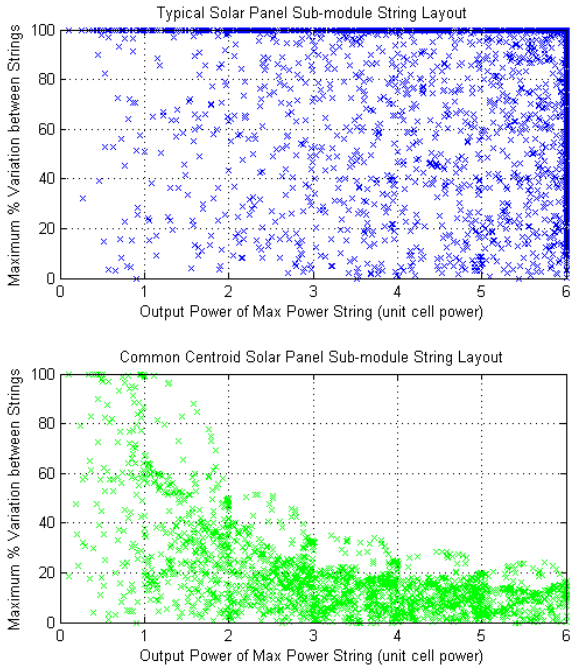


Figure 6. Statistical percentage power variation vs. output power of maximum power string.

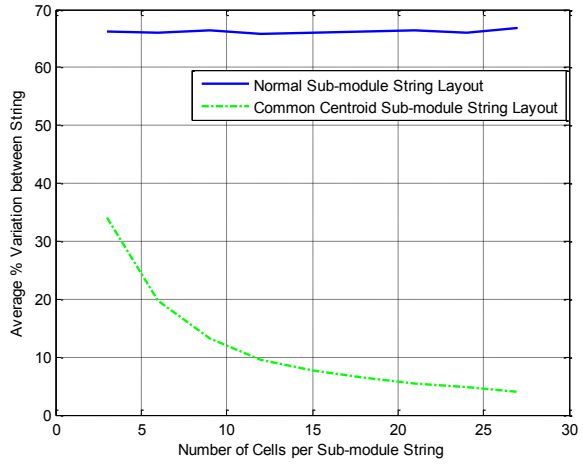


Figure 7. Expected percentage power variation vs. number of cells per sub-module string.

layout results in very high percentage variation in power between strings across all power levels, the common centroid layout significantly limits the percentage variation in power between strings at reasonable power levels.

The number of cells per string can be used as a design variable to limit variation between sub-module strings. By increasing the number of cells per string N, the expected percentage power variation should scale as $\propto 1/N$. To provide design guidelines regarding the number of cells per string needed for a certain expected percentage power variation between strings, statistical simulations are repeated for a variety of sub-module string sizes. The result is shown in Figure 7. While the expected power variation between strings for a normal sub-module string layout remains constant at approximately 65% as the number of cells per sub-module string varies, the expected power variation between strings for a common centroid layout decreases inverse proportional to the number of cells per sub-module string. Approximate 15 cells per sub-modules string can limit the expected percentage variation between strings to less than 10%. This results in 45 cells total and is comparable to current industry offerings. For example, the Mitsubishi PV-MF170EB4 has 50 cells in series. Once the variations are compressed, a highly efficient converter with limited conversion ratio can be used to perform MPPT at the sub-module string level.

C. Module Level Integrated Converters

By following a similar argument in the sub-module string section, process variation can be neglected at the even higher module level. For a large array of solar panels, there exist panels with relatively large spatial separations such that their maximum-power current variations become only weakly correlated. Consequently, at the module level, the SC DC-DC converters must have a wide tuning range to recover losses from the potentially large asymmetries in the maximum-power currents.

To optimally cover the possible range of maximum-power currents $[0, I_{mp}]$, the converter tuning range can again be broken up into uniformly-spaced discrete intervals where the centers of the intervals represent the relative conversion ratio. The system design guidelines regarding the choice of level granularity has been discussed in [12]. Monte Carlo simulation assuming the worst-case uniformly distributed maximum-power currents was used to examine tracking efficiency tradeoffs at the module level. The result suggested good

tracking efficiency improvement from 65% to 90% using a 5-level SC DC-DC converter in a 3-module system.

D. Maximum Power Point Tracking (MPPT)

The switched capacitor integrated converter MPPT algorithm must find the optimal conversion ratio such that the PV element is outputting the maximum power given the desired output current I_o. In other words, the converter must find conversion ratio Q_i to minimize the difference between PV element's current $Q_i I_o$ and the PV element's maximum-power current $I_{mp,i}$, where $I_{mp,i}$ can be estimated by measuring the short-circuit current of the PV element [18]-[19]. Furthermore, it is noted in [12] that a perturb-and-observe step may be necessary for good accuracy following the initial I_{mp} estimate. In a discrete conversion system, this requires at most two additional measurements of both current and voltage.

While the above control strategy is viable, it can be further simplified since there are only a small number of conversion levels available. Instead of using the maximum-power current estimate from short-circuit current measurement followed by a perturb-and-observe step, the local MPPT algorithm can simply loop through all the conversion levels to search for the maximum-power conversion ratio. This translates to only two additional observations in the 5-level converter discussed at the module level. At sub-module string and cell levels, only one additional observation is required. Furthermore, there is no longer a need to measure the output current I_o if the brute-force search method is employed.

Even more simplification can be performed at the sub-module cell level. As discussed in section II-A, the converters at the sub-module cell level are added mainly to reduce process variation induced mismatch. Since asymmetries caused by process variation are unlikely to change significantly over the lifetime of the solar panel, there is no need to run the optimization algorithm continuously during normal operation. The conversion ratio can be hard programmed at panel assembly time, or be self-calibrated on a regular basis.

III. Module Level Converter Experimental Results

A. Overall Experimental Setup

An experimental prototype of the Marx Multilevel converter proposed in [12] was constructed and characterized. Summaries of the circuit components and parameters for each of the implemented conversion ratios are shown in Table I.

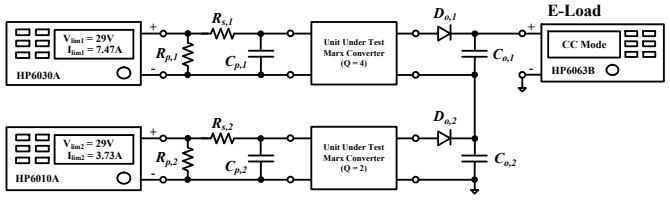


Figure 8. Connection diagram depicting the experimental setup for the series connection of MICs and PV circuit models.

Table I
Experimental Prototype Parameter Summary

Parameter	Symbol	Value
Switched-capacitor	C_i	$12.5\mu F$
Switching Device	M_i	$IRF8721$
Panel Capacitor	$C_{p,i}$	$25\mu F$
Local Output Capacitor	$C_{o,i}$	$12.5\mu F$
Switching Frequency (Q = 2)	$f_{sw,Q2}$	$100kHz$
Switching Frequency (Q = 3)	$f_{sw,Q3}$	$88kHz$
Switching Frequency (Q = 4)	$f_{sw,Q4}$	$127kHz$
Panel 1 MP	P_{MP1}	$170W$
Panel 1 MP Voltage	V_{MP1}	$24.6V$
Panel 1 MP Current	I_{MP1}	$6.93A$
Panel 1 Series Resistance	$R_{s,1}$	0.635Ω
Panel 1 Shunt Resistance	$R_{p,1}$	54Ω
Panel 2 MP	P_{MP2}	$85W$
Panel 2 MP Voltage	V_{MP2}	$24.6V$
Panel 2 MP Current	I_{MP2}	$3.47A$
Panel 2 Series Resistance	$R_{s,2}$	1.27Ω
Panel 2 Shunt Resistance	$R_{p,2}$	108.1Ω

Figure 8 shows the connection diagram of the experimental setup consisting of two series connected modules and the constructed PV circuit models. In this experiment, $Q = 2$ and $Q = 4$ modules were constructed to perform MPPT on two unbalanced PV circuit models. Conversion efficiency was measured using HP34401A digital multimeters. Input and output voltages for each converter were measured at the PCB terminals. Current sense resistors with nominal resistance of $10m\Omega$ were used to measure input and output currents. The precise values for each current sense resistor were measured separately to within $0.01m\Omega$ using current-mode and voltage mode digital multimeters simultaneously.

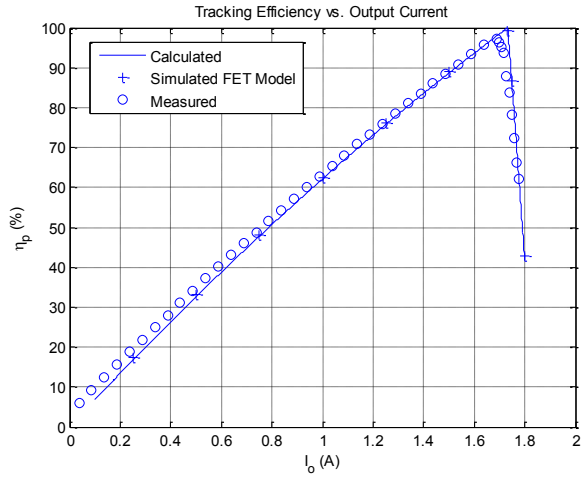
B. Experimental Prototype Performance

The plots in Figure 9 show measured efficiency data compared to simulated and calculated values. Peak conversion efficiency of 92.2% was measured and an optimized conversion efficiency of 95.2% is projected. The added loss in the conversion efficiency plot is due to standby power dissipation not included in simulation and calculation. These additional sources of losses will be characterized and optimized in section III-C.

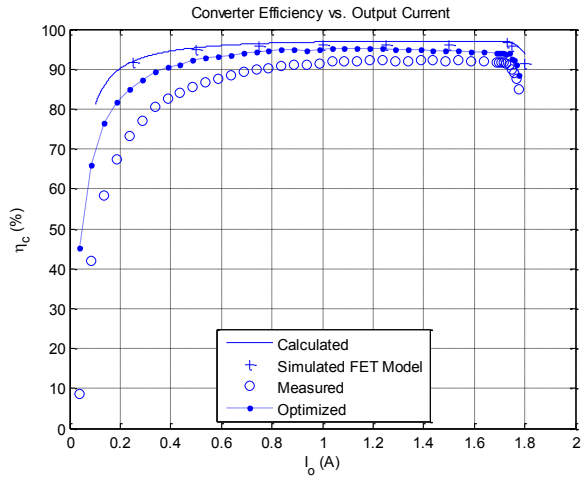
The switching frequencies for the experimental prototype were chosen based on the measured data. Since the most efficient switching frequency generally depends on conversion ratio, in order to maximize the overall system efficiency, the switching frequency showing the maximum conversion efficiency must be chosen for each conversion ratio.

C. Standby Power Dissipation

After constructing and characterizing the experimental prototype, several conversion efficiency optimizations are immediately clear. Several sources of power dissipation that can be optimized will be computed and reasonable values in an optimized prototype will be speculated. These will serve as design guidelines for future iterations of the switched-capacitor converter design.



(a) Tracking Efficiency



(b) Conversion efficiency

Figure 9. Experimental data: single $\boldsymbol{I_o}$ sweep, 2 sources and 2 converters, $Q = [2,4]$, $I_{mp,vec} = [3.465, 6.93]A$, $C = 12.5\mu F$.

The largest contributor to the discrepancy in efficiency between the simulated and the measured systems is the standby power dissipation. One significant portion of the standby power dissipation originates from biasing the zener diodes in the gate drive charge pump circuits shown in Figure 10. The biasing resistor sets the current through the zener diode and should be optimized to provide just sufficient bias current without dissipating excessive power. Thus, appropriate values for the zener bias resistors should be chosen based on the time-averaged voltage across them. The time-average voltage across the bias resistor is the time-averaged MOSFET source voltage minus the zener voltage. Therefore, the bias resistor value is related to both the associated MOSFET and the conversion ratio. Table II indicates the MOSFET source voltages normalized by the input voltage across possible conversion ratios.

In the experimental system, the only MOSFETS that require charge-sustaining gate drives are M3, M6, M9 and M10. To compute the upper limit of the biasing resistor, the minimum zener bias current and the minimum input voltage

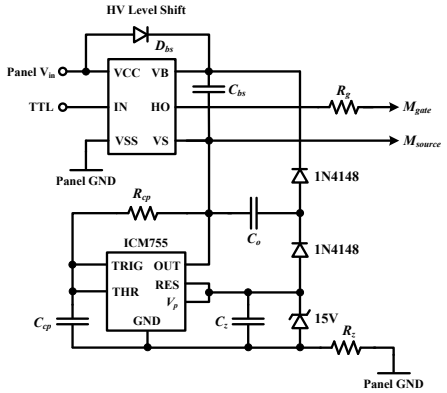


Figure 10. Recommended gate drive adapted from IR AN-978 [20]

Table II
MOSFET SOURCE VOLTAGES NORMALIZED TO INPUT VOLTAGE

	Recharge	$Q=0$	$Q=1$	$Q=2$	$Q=3$	$Q=4$
M1	0	0	0	1	1	1
M2	0	0	0	0	0	0
M3	1	1	1	1	1	1
M4	0	0	0	1	1	2
M5	0	0	0	1	1	1
M6	1	1	1	2	2	2
M7	0	0	0	1	2	3
M8	0	0	0	1	1	2
M9	1	1	1	2	2	3
M10	≈1/2	0	1	2	3	4
M11	0	0	0	1	2	3

must be considered. For instance, with $V_{in,\min} = 24V$ and $I_{z,min} = 18mA$, the time-averaged bias voltage for the MOSFET M6 in the $Q = 2$ operation is

$$\langle V_{z6,Q2} \rangle = 24 \cdot \frac{1+2}{2} - 15 = 21V. \quad (4)$$

The maximum zener bias resistor value for the M6 in the $Q = 2$ switching pattern is then

$$R_{z6,Q2} \leq \frac{\langle V_{z6,Q2} \rangle}{I_{z,min}} \quad (5)$$

$$= 1.17k\Omega. \quad (6)$$

The time-averaged power in the resistor can be calculated to be

$$P_{R6,Q2} = \frac{\langle V_{z6,Q2}^2 \rangle}{R_{z6,Q2}} \quad (7)$$

$$= \frac{\langle V_{z6,Q2} \rangle^2 + \left(0.707 \cdot \Delta V_{M6,Q2}\right)^2}{R_{z6,Q2}} \quad (8)$$

$$= \frac{21^2 + (0.707 \cdot 12)^2}{1.17 \cdot 10^3} = 440mW. \quad (9)$$

where a square wave of bias voltage and the maximum allowable bias resistance are assumed. In addition to the power

dissipated in the resistor, the zener diode itself dissipates power. The zener power dissipation can be approximated as

$$P_{z,i} \approx I_z \cdot V_{z,i} \tag{10}$$

$$= 18mA \cdot 15V = 270mW. \tag{11}$$

Since both sources of loss depend heavily on the zener bias current, the zener diode bias should be minimized to reduce the standby power required for biasing. Note that this optimization is valid to the extent that the zener bias current is larger than the current demanded by the charge pump circuit.

A third source of standby power dissipation originates from charging and discharging the timing capacitor in the charge pump circuit. This loss can be calculated as

$$P_{cp,timing} = C_{cp} \cdot V_{z,i}^2 \cdot f_{cp}. \tag{12}$$

where the timing capacitor is assumed to fully charge to the zener voltage and fully discharged each switching cycle. Therefore, reducing the timing capacitance value may constitute a significant optimization. The charge pump switching frequency can remain unchanged by increasing the timing resistor by the same factor.

These un-optimized standby power dissipation sources are characterized and tabulated. Reasonable optimized values for the fully discrete implementation of the Marx experimental prototype are calculated as well. The optimized standby power dissipation numbers are assumed in the conversion efficiency data from section III. The results are summarized in Table III for the $Q = 2$ module.

The experiments demonstrate the value and approach to loss minimization for a particular MIC design. Different gate drive architectures may be employed in a practical switched-capacitor MIC integrated circuit. While the specific details of the appropriate optimizations will vary with the MIC topology, the possibilities and approach for developing a high efficiency converter are illustrated here.

Table III
STANDBY POWER OPTIMIZATION RESULTS FOR $Q = 2$ MODULE

Source	Un-optimized	Optimized
Charge Pump Zener M3	432mW	48mW
Charge Pump Zener M6	710mW	72mW
Charge Pump Zener M9	710mW	72mW
Charge Pump Zener M10	502mW	60mW
Charge Pump Timing Cap × 4	130mW	26mW
HV Level Shift × 11	158mW	100mW
ICM7555 × 5	6mW	6mW
LM7812	158mW	100mW
LM7805	6mW	6mW
Total	2.8W	500mW

D. Run-Time Zener Biasing Optimization

As shown in the previous section, the optimal zener bias resistance value depends on the conversion ratio, it should be chosen at run-time to minimize standby power. One approach could be to implement a switched set of fixed resistors for each gate drive, and the converter could choose the resistor based on the conversion ratio. One such scheme could be implemented using ground-referenced MOSFETs and TTL level control signals.

However, the optimal zener bias resistance value also depends on the input voltage. As the input voltage increase beyond the minimum value of 24V, excessive power dissipation is introduced in the passive biasing circuit. Thus, an even more efficient solution employs active current sources to provide the zener bias current. In this case, the power dissipation in the biasing circuit is simply

$$P_{z,i} = \langle V_{MOSFET,s,i} \rangle \cdot I_{z,i}. \tag{13}$$

For instance, to minimize the standby power dissipation, a zener diode with a low bias current of $2mA$ is selected. Then, the power dissipation of M6 zener biasing would be

$$P_{z,6} = 24 \cdot \frac{1+2}{2} \cdot 0.002 = 72mW. \tag{14}$$

E. Run-Time Frequency Scaling

Based on Table I, the switching frequency yielding the highest conversion efficiency is dependent of the conversion ratio. Therefore, the switching frequency should also be selected at run-time to ensure the highest overall conversion efficiency is achieved. This selection may be based on a pre-determined set of optimal switching frequencies for a specific load current.

IV. GRID-TIE INVERTER INTERFACE

The proposed centralized inverter consists of three components illustrated in block schematics in Figure 11. Unlike conventional string inverters and microinverters that close a single feedback loop on the current injected to the grid to control both maximum power point tracking and power delivery to the grid, the propose architecture uses two separate controllers to achieve maximum power point tracking and energy balance.

The input current sink serves as the MPPT tracking control by demanding a current from the PV array that maximizes the product of the demanded current and the PV array voltage. Functionally, the input current sink could be implemented as a canonical cell converter such as a boost or a SEPIC converter. The input power from the PV array can then be monitored by measuring the PV array input voltage. An energy balance control loop can then be designed to use this information to control the power injected to the grid. That is, the input power can be fed forward to improve grid-tie inverter response time and controller stability.

A. Grid-Tie Inverter Stability

It was shown in [21] that the stability of a grid-tie inverter can be derived by a small-signal equivalent circuit model shown in Figure 12, where the grid-tie inverter is modeled as a Norton equivalent current source and the utility grid is modeled as a Thevenin equivalent voltage source. Using the equivalent circuit model, the output current of the inverter can be solved by superposition to be

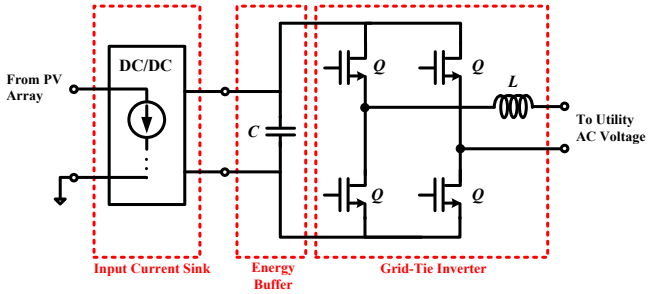


Figure 11. Grid-tie inverter interface.

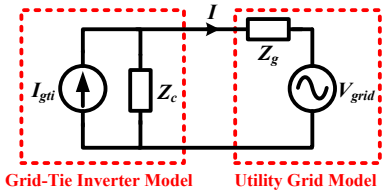


Figure 12. Grid-tie inverter model from [21]

$$I(s) = \frac{I_{gti}(s) \cdot Z_c(s)}{Z_c(s) + Z_g(s)} - \frac{V_{grid}(s)}{Z_c(s) + Z_g(s)} \tag{15}$$

$$= \left(I_{gti}(s) - \frac{V_{grid}(s)}{Z_c(s)} \right) \cdot \frac{1}{1 + \frac{Z_g(s)}{Z_c(s)}}. \tag{16}$$

From (16), the stability criterion can be derived. Specifically, the impedance ratio $Z_g(s)/Z_c(s)$ is required to satisfy the Nyquist criterion. This implies that the grid-tie inverters should be designed to have output impedance $Z_c(s)$ significantly higher than the grid impedance in order to operate with stability when connected to the grid. That is, the following condition should be satisfied.

$$\left| \frac{Z_g(s)}{Z_c(s)} \right| < 1 \tag{17}$$

Furthermore, the control strategy for the grid-tie inverter has strong effects on the inverter's output impedance. Thus, separating the controls into two separate loops simplifies the inverter output impedance derivation and provides additional insights for design. In the following section, the control strategy will be outlined and the output impedance will be derived.

B. Energy Balance Control

The power P_{in} flows into the grid-tie inverter via the input current sink and is delivered to the utility grid by controlling the magnitude of the output current. The energy buffer capacitor would store any energy difference between the input energy and the energy delivered to the grid.

A sampled-data approach is adopted where the input power P_{in} and the energy stored on the buffer capacitor $e[n]$ are sampled at twice the line frequency. Using the sampled data, the controller specifies the scale factor of the reference current waveform for the next cycle. Note that the reference current waveform is assumed to be a scaled version of the grid voltage for unity power factor operation. In addition, a fast inner current hysteresis loop is assumed to shape the current injected to the grid. The energy balance equation can then be written as

$$e[n+1] = e[n] + P_{in} \cdot T - \int_{nT}^{(n+1)T} c[n] \cdot v_{grid}^2(t) dt \tag{18}$$

where $e[n]$ is the energy stored in the capacitor C at the n-th sampling instant, T is the sampling period of $1/(120Hz)$, and $v_{grid}(t)$ is the voltage of the grid. For the following analysis, assume that the grid voltage has nominal amplitude of V_s.

Given ideal components, the grid-tie inverter can be controlled without any feedback. By selecting $c[n] = 2P_{in}/V_s^2$, the integral term cancels the $P_{in}T$ term exactly, so the energy stored on the buffer capacitor will be in steady-state. However, practically there are always errors in the computation of power due to losses and model deviation so the current amplitude control $c[n]$ will be implemented with a feedforward term plus a feedback term.

$$c[n] = c_0 + \tilde{c}[n] \tag{19}$$

$$= \frac{2 \cdot P_{in}}{V_s^2} + k \cdot \frac{2}{V_s^2 \cdot T} \cdot \tilde{e}[n] \tag{20}$$

where $\tilde{e}[n] = e[n] - e_{ref}$.

A model for computing the incremental output impedance is shown in Figure 13. This analysis was first presented in [22] for the nonzero input source impedance in a unity power factor converter. In the grid-tie inverter case, the analysis can be applied in the "reverse" direction. Let v_i represent a small voltage source perturbation used to probe the output impedance of the inverter as presented to the grid. This voltage can be expressed as a perturbation to the steady-state grid voltage $v_{grid}(t) = V_s \cdot cos(\omega_0 t)$ such that

$$v_{grid}(t) + v_i(t) = V_s \cdot \cos(\omega_0 t) \cdot \{1 + \epsilon \cdot \cos(\omega_1 t)\} \tag{21}$$

where ω_0 is the line frequency, $\omega_1 < \omega_0$ and $\epsilon \ll 1$. That is, v_i corresponds to an additive perturbation in a frequency range near ω_0. In order to solve for the output impedance, the corresponding perturbation in the input current needs to be solved. Assuming small enough ϵ and ω_1, the integral term in (18) can first be approximated as

$$c[n] \cdot \frac{TV_s^2}{2} + c[n] \cdot \epsilon \cdot TV_s^2 \cdot \cos\left(\omega_1 T \cdot \left(n + \frac{1}{2} \right) \right). \tag{22}$$

And the difference equation can then be approximated as

$$e[n+1] \approx e[n] + P_{in}T - c[n] \cdot \frac{TV_s^2}{2} - c[n] \cdot \epsilon \cdot TV_s^2 \cdot \cos\left(\omega_1 T \cdot \left(n + \frac{1}{2} \right) \right). \tag{23}$$

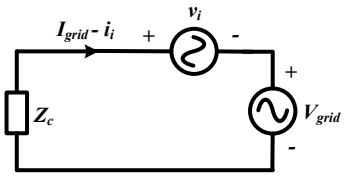


Figure 14. Model for calculating the output impedance of a constant power grid-tie inverter.

Simplifying the expression further by cancelling the $P_{in}T$ term and the $c_0 \cdot TV_s^2/2$ term, and assuming the product of two small signal terms is negligible, the following difference equation can be written.

$$\tilde{e}[n+1] \approx \tilde{e}[n] \cdot (1-k) - c[n] \cdot \epsilon \cdot TV_s^2 \cdot \cos\left(\omega_1 T \cdot \left(n+\frac{1}{2}\right)\right). \quad (24)$$

Equivalently, the difference equation can be expressed in terms of the feedback term in the control variable using (20).

$$\frac{\tilde{c}[n+1]}{2k} \approx \tilde{c}[n] \cdot \frac{1-k}{2k} - c[n] \cdot \epsilon \cdot \cos\left(\omega_1 T \cdot \left(n+\frac{1}{2}\right)\right) \quad (25)$$

Finally, the total current delivered to the grid from the converter output can be written as

$$I_{grid}(t) - i_i(t) = c[n] \cdot \left(v_{grid}(t) + v_i(t)\right) \quad (26)$$

$$\approx c_0 \cdot v_{grid}(t) + \tilde{c}(t) \cdot v_{grid}(t) + c_0 \cdot v_i(t). \quad (27)$$

where $\tilde{c}(t)$ is the result of passing the discrete sequence $\tilde{c}[n]$ through a zero-order hold. The incremental current due to the voltage perturbation can then be approximated as

$$i_i(t) \approx -\epsilon \cdot c_0 \cdot v_{grid}(t) \cdot \cos(\omega_1 t) - \tilde{c}(t) \cdot v_{grid}(t) \quad (28)$$

$$\approx -\epsilon \cdot c_0 \cdot v_{grid}(t) \cdot cos(\omega_1 t) \cdot \{1 + H(\omega_1)\} \quad (29)$$

where $H(\omega_1)$ is the response of the product of the transfer function in (25) and a sampler at rate $1/T$. Making the same approximation as in [22], the approximate expression for the incremental output impedance be solved in terms of ω_1 and re-expressed in terms of ω by using substituting $\omega_1 = \omega - \omega_0$.

$$Z_c(\omega) = \frac{-1}{c_0} \cdot \frac{1}{1 + sinc\left(\frac{(\omega-\omega_0)T}{2}\right)\frac{-2k}{e^{j(\omega-\omega_0)T} - (1-k)}} \quad (30)$$

Figure 14 shows the magnitude and phase of the grid-tie inverter's incremental output impedance. Note that the

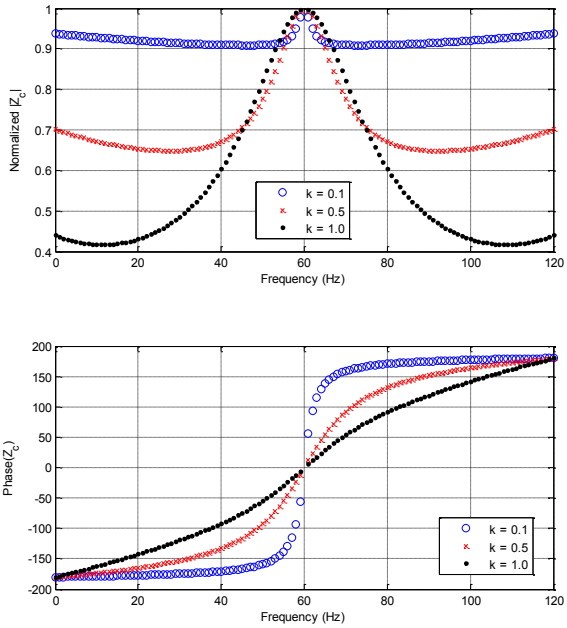


Figure 13. Approximate Output Impedance normalized to $\frac{1}{c_0} = \frac{V_s^2}{2P_{in}}$ for different feedback gain k.

expression in (30) is only valid for frequencies near $60Hz$, specifically, $|\omega - \omega_0| < \pi/T$. Due to the sample and hold operations, perturbations with frequency content outside of this range will alias into this range. As shown in the figure, the incremental output impedance looks real and positive with value $V_s^2/(2P_{in})$ at $60Hz$. However, the magnitude of the incremental output impedance decreases as the perturbation frequency deviates from $60Hz$. In particular, the decrease in margnitude of the incremental output impedance is more significant for larger values of the feedback gain parameter k. Note that the phase of the incremental output impedance quickly changes 180^o as the perturbation frequency deviates from $60Hz$ as well. Therefore, referring back to the stability criterion derived in (17), larger feedback gain values make the grid-tie inverter more susceptible to stability problems due to decreasing impedance magnitude.

The benefit of the proposed system architecture now becomes evident. By decoupling the MPPT tracking and the energy balance control loops, the system can potentially operate more stably by relying more heavily on the feedforward term than the feedback term. In addition, since the MPPT tracking is controlled by an input current sink, the change in power from the PV array can be accurately monitored by measuring the PV array voltage only. Even if the feedback loop is not fast enough to track input power transients, the feedforward path can force a resample mid-cycle (at the price of non-unity power factor for one cycle) to prevent the energy buffer capacitor voltage from running out of range. The forced resample may be triggered by passing the PV array voltage through a high-pass filter and level detectors to check for sudden large steps in input power. Note that the frequency of occurrence of such event is expected to be low.

C. Bus Capacitor Utilization

A DC-to-AC converter needs an energy buffer stage to store the instantaneous power difference between the input and the output ports. Such an energy buffer is typically implemented with a single large capacitor. As the system reaches periodic steady state, the instantaneous power difference manifests itself in a ripple voltage on the capacitor at twice the line frequency. The exact expression for the magnitude of the voltage ripple can be derived. Assume the grid-tie is in period steady state so that

$$v_{in} \cdot i_{in} = \frac{1}{2} \cdot v_{grid} \cdot i_{grid}. \tag{31}$$

where v_{in} and i_{in} are DC values, and v_{grid} and i_{grid} are AC amplitudes. The factor of $1/2$ arises from the RMS conversion. The instantaneous power on the buffer capacitor can be written as

$$P_{cap} = P_{in} - P_{grid} \tag{32}$$

$$= P_{in} - 2 \cdot P_{in} \cdot \cos^2(\omega_0 t) \tag{33}$$

$$= -P_{in} \cdot \cos(2\omega_0 t). \tag{34}$$

If the power is integrated over the positive half capacitor ripple cycle, or a quarter of the line cycle, the peak to peak energy change in the storage capacitor can be calculated as

$$\Delta E_{cap} = \int_{\substack{positive\ half \\ ripple\ cycle}} P_{in} \cdot \cos(2\omega_0 t)\, dt = \frac{P_{in}}{\omega_0}. \tag{35}$$

Finally, the peak-to-peak energy change can be translated into peak-to-peak voltage ripple on the energy buffer capacitor.

$$\Delta E_{cap} = \frac{1}{2} \cdot C \cdot \left(V_c + \frac{1}{2}\Delta V_{r,pp}\right)^2 - \frac{1}{2} \cdot C \cdot \left(V_c - \frac{1}{2}\Delta V_{r,pp}\right)^2 \tag{36}$$

Combining (35) and (36) gives the expression for the voltage ripple on the energy buffer capacitor.

$$\Delta V_{r,pp} = \frac{P_{in}}{\omega_0 \cdot C \cdot V_c} \tag{37}$$

Equation (37) provides clear guidelines for grid-tie inverter bus capacitor sizing. For instance, given a $1kW$ power system with nominal bus capacitor voltage of $V_c = 400V$ and maximum allowable peak-to-peak voltage ripple $\Delta V_{r,pp} = 20V$, the energy buffer capacitor must be at least $332\mu F$.

Now consider the energy utilization of the capacitor in this case. The capacitor stores a maximum of $27.9J$ but only $2.65J$ is used to buffer the instantaneous power difference between the input and output ports. Thus, the energy utilization of a single bus capacitor implementation allowing 5% ripple voltage is

$$\frac{\Delta E_{cap}}{E_{cap,max}} = 9.5\%. \tag{38}$$

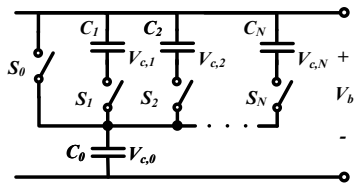


Figure 15. Switched-capacitor energy buffer implementation.

The capacitor shift topologies [23] are known to achieve higher energy utilization and lower voltage ripple. Using such a topology for the energy buffer capacitor would lead to more effective capacitor utilization and smaller capacitor volume for the same allowable voltage ripple.

As an illustration, consider the capacitor shift topology in Figure 15, where only one switch can be turned at any given time. For simplicity consider the base example with only C_0, C_1, S_0, and S_1 are present. Assume unit capacitance, arbitrary initial conditions and that the bus experiences discharging by a unit current source for 1 second then charging by a unit current for 1 second. Furthermore, assume that switch S_0 is turned on the moment discharge cycle begins.

In order to minimize the ripple seen at the top of the bus, it must be true that after C_0 is discharged through S_0 for some time, S_0 will turn off and S_1 will turn on to add the initial voltage of C_1 back onto the bus. Thus, the initial condition for capacitor C_1 must be a positive and equal to the initial voltage drop in C_0. After S_1 turns on, the bus voltage now decreases twice as fast as before.

The optimal case is when the two sub-cycles exhibit the same drop in bus voltage, i.e. S_0 turns off after $2/3$ seconds. Thus, the optimum ripple magnitude now becomes $2/3$ of that of the single bus capacitor case. During the charge cycle, the switching sequence is the mirror sequence of the discharge cycle. That is, the capacitors will end up same charge they started with before the discharge cycle.

This method can be extended to the energy buffer bus capacitor, where the charge and discharge current waveforms are sinusoidal. The corresponding waveforms are shown in Figure 16. The two waveforms show the same reduction in ripple magnitude but with different timing for the switches. The switch timing can be solved by taking the inverse of the sinusoidal function at the corresponding ripple magnitudes.

The initial condition for C_1 only depend on the ripple size, which leads to very low voltage ratings. On the other hand, the initial condition for C_0 cannot be determined by using the ripple size alone. In the case of an inverter energy buffer, the initial voltage on C_0 instead depend on the nominal bus voltage, which requires high voltage rating.

Consider the previous example with maximum allowable peak-to-peak voltage ripple reduced by 33%. Assume electrolytic capacitors are used and their volume scales [24] with

$$Vol \propto C \cdot V_{rating}^{1.5}. \tag{39}$$

In the conventional case, the energy buffer capacitance would need to increase by 50%, which translates 50% more volume. However, in the switched-capacitor implementation, even though the same capacitance is added, the required voltage

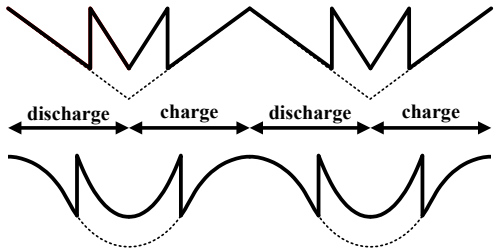


Figure 16. Switched-capacitor charge and discharge waveforms.

rating is only 13.3V. Therefore, the total increase in capacitor volume from the estimate in (39) is less than 0.6%.

The theory can be generalized to any number of switches and capacitors. Using N equally sized capacitors in the switching configuration, the ripple size is reduced to

$$\Delta V_{r,pp} = \frac{2}{N+1} \cdot \left(\frac{P_{in}}{\omega_0 \cdot C \cdot V_c} \right). \tag{40}$$

Furthermore, each capacitor in the array must be charged to some initial voltage before the discharging cycles begin.

$$V_{i,max} = \begin{cases} V_{bus} + \frac{1}{2} \cdot \left(\frac{P_{in}}{\omega_0 \cdot C \cdot V_c} \right), & i = 0 \\ \frac{i+1}{N+1} \cdot \frac{P_{in}}{\omega_0 \cdot C \cdot V_c}, & 1 \le i \le N-1 \end{cases} \tag{41}$$

In the proposed architecture, all the values in (40) and (41) are readily measured. Thus, the capacitor voltages can be tightly monitored and robustly controlled. Note that evaluating (41) using the maximum input power from the PV array would yield the voltage ratings for the capacitors.

To illustrate the potential application of this switched-bus-capacitor approach for a grid-tie inverter, consider the results of a basic control algorithm implemented in a SPICE simulation. The circuit block diagram and the controller overview are shown in Figure 17. The switched-bus-capacitor energy storage is implemented with just two capacitors for illustration purposes. The system is designed to maintain a bus voltage of $250V$ and deliver a maximum of $500W$ to the grid. The preliminary control strategy developed here pre-computes the optimal cycle timings to switch in C_1 while maintaining the voltage $V_{c,1}$ within the bounds calculated from (40) and (41). That is, whenever the voltage $V_{c,1}$ is about to exceed the calculated bounds, $Q_{c,0}$ is switched on so C_0 absorbs the rest of the charge or discharge current alone. The voltage on C_0 is then regulated by the energy balance control loop.

Note that in a sampled system, the worst-case behavior occurs if a large transient occurs directly after sampling has taken place. Thus, this is the case chosen for the simulation. However, by forcing the system to resample, the inverter output current settles to the final value almost immediately as shown in Figure 18. Furthermore, the bus capacitor control is shown to keep the voltage $V_{c,1}$ within the calculated bounds in real-time.

Finally, it is noteworthy that using the switched-capacitor implementation, smaller capacitors with lower voltage ratings can be used to replace a single large capacitor with high voltage rating. Thus, it is possible to construct an inverter potentially free of electrolytic capacitors in order to enable long-life operation.

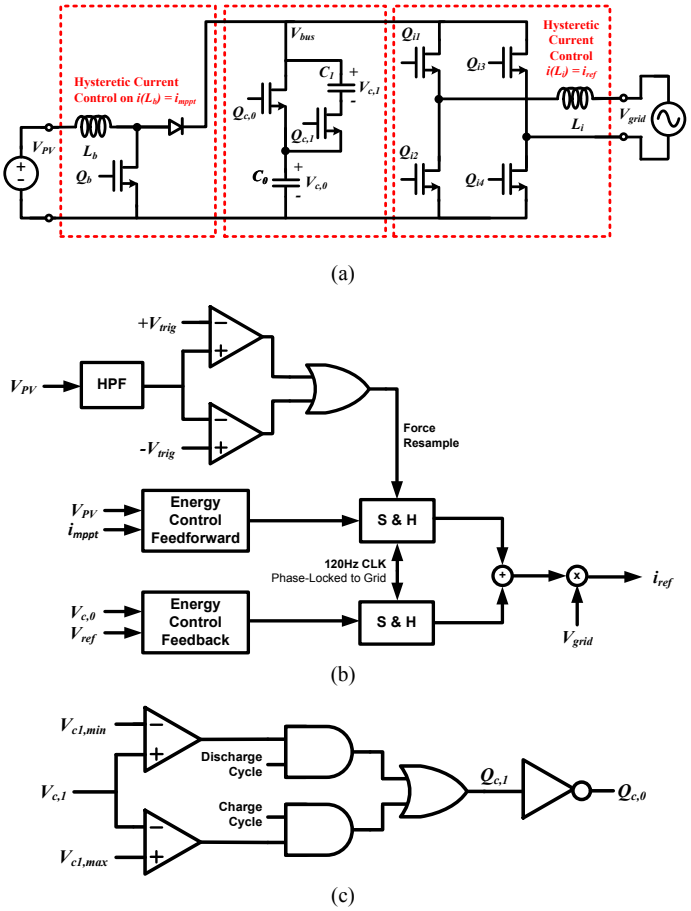


Figure 17. Overall system-level block diagram and control schemes implemented in SPICE simulation. (a) system overview of the simulated circuit. (b) energy balance controller with feedforward forced resampling. (c) preliminary switched-bus-capacitor control logic.

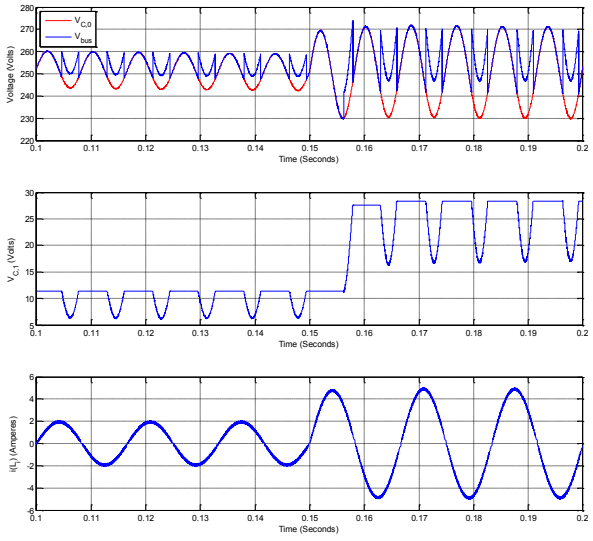


Figure 18. Simulated step response. Input voltage step from 40V to 100V and $i_{mppt} = 4A$. The input step occurs after $150ms$.

V. Conclusion and Future WOrks

This paper offers a different approach to the distribution of energy conversion and control throughout a solar array. The architecture choices presented here affect the power electronics implemented at the module. These choices afford new opportunities for the control and processing of energy that may enhance system and grid-interaction stability. They also offer the possibility of removing certain types of components from troublesome areas of the system, e.g., magnetics behind panels and electrolytic capacitors in the inverter. This paper presents a "system" view of a solar array, and explores potential optimizations that maximize energy extraction to the grid with the improved stability while potentially minimizing expense and maximizing field life.

Switched-capacitor DC-DC converters have been shown to be beneficial at all levels of solar energy extraction. Notably, utilizing these converters at the cell level may lead to reduction in production cost or different opportunities for the manufacturer of solar panels. Common centroid layout can potentially keep MPPT converters away from extreme conversion ratios where their conversion efficiencies may degrade.

As generation on the utility grid becomes increasingly distributed due to the influx of renewable energy sources, the uncertainty of local grid impedance will increase. Thus, stability of the electrical power network is becoming a growing concern. The proposed architecture can potentially minimize the possibility of unstable interactions with the grid by exploiting the utility of feedforward information from the PV array current sink. The technologies in this architecture could be applied in other areas as well, including power-factor correcting converters.

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