Per Panel Photovoltaic Energy Extraction with Multilevel Output DC-DC Switched Capacitor Converters

John J. Cooley, *Student Member, IEEE*, and Steven B. Leeb, *Fellow, IEEE*
Massachusetts Institute of Technology
Dept. of Electrical Engineering and Computer Science
Cambridge, MA, USA

***Abstract*—Switched capacitor multilevel output DC-DC converters are evaluated as panel integrated modules in a solar maximum power point tracking system. The recommended system includes a central input current-controlled ripple port inverter. Potential benefits include per panel MPPT without inter-panel communication, electrolytic capacitors or per panel magnetics. Statistical methods are used to predict average tracking and conversion efficiencies. A particular implementation of the switched capacitor module is studied - the Marx converter. Average total efficiencies (tracking $\times$ conversion) greater than 93% are predicted for a simulated 510 W, 3 panel, DC-DC system.**

***Index Terms*—Switched Capacitor, Multilevel, Marx, Module Integrated Converter, Photovoltaic, Ripple Port Inverter**

I. Introduction

The total installed cost ($/W) and total cost of ownership ($/Wh) have been well-studied as the key metrics controlling the grid penetration of solar power [1]–[4]. Among the factors impacting installed cost (per Watt) are power converter cost and total (tracking $\times$ conversion) efficiency, both of which share strong relations to converter and system complexity. A critical factor impacting the cost of ownership is the lifetime of the power converter (and implied replacement costs). Cost-effective solutions for solar energy extraction should address system cost and complexity, conversion and tracking efficiencies and converter lifetime simultaneously.

The need for suitable tracking efficiency is normally addressed with a maximum power point tracking (MPPT) algorithm embedded in the control of the converter or inverter [5], [6]. In the important grid-tied case, 120 Hz power ripple at the panel terminals negatively impacts the MPPT function, but this may be addressed by augmenting the source with a large electrolytic capacitor [7]–[15]. However, the limited lifetime of electrolytic capacitors contends directly with the long-life characteristic of cost-effective solar conversion. To reconcile this, [1] proposed the "ripple port" inverter, which still directly interfaces the PV cell, but directs the 120 Hz ripple power to a transformer coupled ripple port and away from the cell.

There is a growing need to implement per panel MPPT to contend with varying light levels, temperatures, panel ages, etc. across physically widespread solar arrays [7]–[15]. There are advantages of a DC-DC MIC + central DC-AC approach over a DC-AC MIC approach. These include the availability of a single DC bus for an entire array and intermediate power ripple filtering, as well as added degrees of freedom for MPPT control [7], [8], [16]. With per-panel MPPT, global tracking efficiency can be significantly improved over simple series or parallel connections of those panels (see Section II-D), but the installation of per-panel converters impacts the important cost metrics above. Converter lifetime and replacement costs become even more critical with per panel conversion.

Many inductor based converters and inverters have been proposed as module integrated converter (MIC) topologies, but they require magnetic components to be either purchased per panel or to be integrated into the converter IC [7]–[11]. Multilevel converters have been proposed as per panel DC-AC converters, but they suffer from either 120 Hz power ripple at the panel terminals or the need for cost-prohibitive and / or electrolytic energy storage [12]–[15].

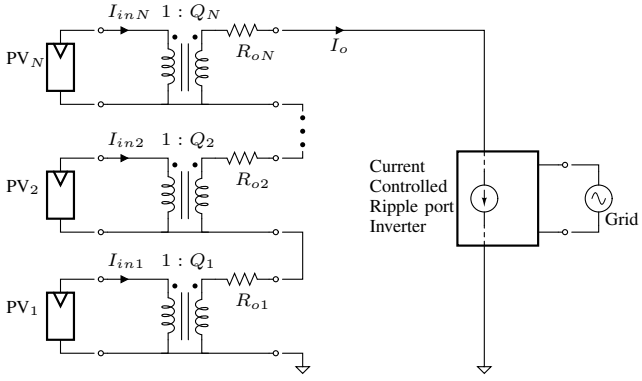


Fig. 1: A DC linearized model with an N-panel PV string illustrates the system-level approach. The ideal transformers model the function of the DC-DC MICs.

A. System Overview

The system level approach in this paper is illustrated by the DC linearized circuit model in Figure 1. This system shares some key features with other systems employing DC-DC MICs and a central inverter but differs in at least one key way [7]. The DC-DC MICs typically operate with local autonomous MPPT control. In the system proposed here, the

responsibility of MPPT is shared among the DC-DC modules and the central inverter. As a result, the required complexity of the DC-DC MICs is simplified. Significantly, the system can be implemented with switched capacitor multilevel DC-DC converters and a central ripple-port inverter. Per panel magnetics are eliminated as are electrolytic capacitors. Any magnetics that are required for the ripple port inverter need only be purchased once per string. The DC-DC module conversion ratios are selectable, but discrete. A central question that is addressed in this work concerns the tracking efficiency that is possible with this system.

B. Switched Capacitor Benefits

Switched capacitor converters achieve current and voltage conversion without magnetic energy storage. Figure 2 shows the cost and volume per energy storage (μJ) for a sample of discrete capacitors and inductors suitable for power applications. These data imply *a-priori* expected cost and volume benefits of switched capacitor converters when compared to inductor-based converters. A detailed discussion can be found in [17].

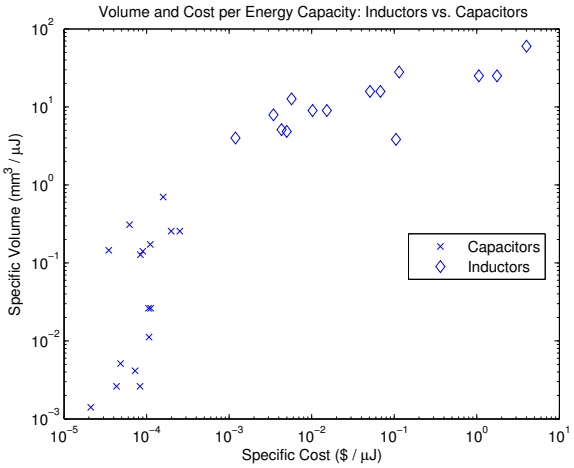


Fig. 2: Specific cost and volume: Discrete inductors (10 μH-1 mH/100 mA-1 A) and capacitors (Ceramic and Film 1-10 μF/10-100 V) sampled from Digikey. Energy was calculated as $\frac{1}{2}CV^2$ or $\frac{1}{2}LI^2$ for maximum rated voltages and currents.

C. Total Efficiency

Total efficiency is central to the design and evaluation of the systems in this work. Here we define total efficiency, η, as the product of tracking efficiency, η_p, and conversion efficiency, η_c:

$$\boxed{\eta = \eta_p \times \eta_c}. \tag{1}$$

Figure 3 depicts a sample of reported tracking and conversion efficiencies in MPPT algorithms and DC-DC MICs respectively. The two ranges are multiplied yielding a third range corresponding to total efficiency, η.

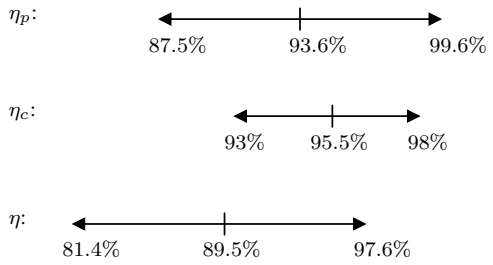


Fig. 3: A literature survey of total energy extraction efficiency, DC-DC MICs: [7], [8], [18]–[23] and MPPT algorithms: [6], [23]–[27]

II. Maximum Power Point Tracking

Maximum power point tracking in the system of Figure 1 is simplified by the input current control of the central inverter and the series connection of the MICs. The selectable conversion ratios, Q_i, allow the DC-DC modules to track local MPP's as the string current varies. The central inverter tracks the global MPP by adjusting its input current.

The run-time global MPPT can be implemented by exploiting time-scale separation. Here, we take the local MPPT control to operate fast, and the global MPPT control to operate relatively slowly. Specifically, on the time-scale of local MPPT control, the string current, I_o, may be taken to be static or "quasi-static." Because the maximum power point of each panel is defined by a unique maximum power current, $I_{mp,i}$, the quasi-static string current naturally decouples MPPT control among the modules.

A. PV Model

Before discussing system performance further, we establish a model of the photovoltaic panel and its parameters. The circuit model used here (Figure 4) is common in the literature, e.g. [16]. Given the parameters quoted in a typical datasheet,

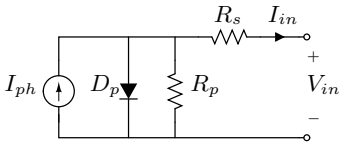


Fig. 4: PV circuit model

V_{oc}, I_{sc}, and the maximum power voltage and current, V_{mp}, and I_{mp}, analysis of the circuit in Figure 4 yields

$$V_{dp} = V_{oc} \tag{2}$$

$$R_s = \frac{V_{oc} - V_{mp}}{I_{mp}} \tag{3}$$

$$R_p = \frac{I_{sc}R_s - V_{oc}}{I_{mp} - I_{sc}} \tag{4}$$

$$I_{ph} = I_{mp} + \frac{V_{fwd}}{R_p}, \tag{5}$$

where V_{dp} is the forward voltage of the diode, D_p, in the model. In Figure 4, when $I_{in} < I_{mp}$, the diode, D_p, is

forward-biased and it is reverse-biased otherwise. The resulting panel voltages are

$$\begin{aligned} V_{in} &= V_{dp} - I_{in}R_s, & I_{in} < I_{mp} \\ V_{in} &= R_p I_{ph} - (R_s + R_p)I_{in}, & I_{in} \geq I_{mp} \end{aligned} \quad (6)$$

and the panel power is simply

$$P_{in} = I_{in}V_{in}. \quad (7)$$

For simplicity, the rest of this work assumes the following nominal datasheet values adapted from a Mitsubishi PV-MF170EB4 [28]:

$$\begin{aligned} I_{mp} &= 6.93 \text{ A} \\ V_{mp} &= 24.6 \text{ V} \\ I_{sc} &= 7.38 \text{ A} \\ V_{oc} &= 29 \text{ V} \end{aligned} \quad (8)$$

B. Local Maximum Power Point Tracking

Local MPPT control consists of matching the string current, to the panel's own $I_{mp,i}$'s. From Figure 1, the i^{th} panel current is

$$I_{in,i} = Q_i I_o. \quad (9)$$

Given a quasi-static string current, I_o, the modules each choose a Q_i to maximize their panel power. This maximization step can be performed a number of ways. For instance, the modules may estimate their $I_{mp,i}$'s via short-circuit current measurements. References [29]–[33] discuss MPPT control by this method. A perturb and observe step may be necessary for good accuracy following the initial I_{mp} guess. In our system, having discrete conversion ratios, a maximum of two additional observations should be required to determine the actual optimal conversion ratio.

In the simulations that follow, the local algorithm for choosing conversion ratios was implemented as follows. Given $I_{mp,i}$ either by the short-circuit method described above or otherwise, the modules attempt to minimize the error $|I_{in,i} - I_{mp,i}|$. This minimization is constrained according to the nonlinear behavior of the PV indicated in Figure 4. Combining equations (6) and (7), the panel power for the i^{th} panel can be written:

$$\begin{aligned} P_{in,i} &= I_{in,i}V_{dp,i} - I_{in,i}^2 R_{s,i}, & I_{in,i} < I_{mp,i} \\ P_{in,i} &= I_{in,i}R_{p,i}I_{ph,i} - (R_{s,i} + R_{p,i})I_{in,i}^2, & I_{in,i} \geq I_{mp,i}. \end{aligned} \quad (10)$$

Taking the derivative of (10) with respect to I_{in} yields

$$\begin{aligned} \frac{\partial P_{in,i}}{\partial I_{in,i}} &= V_{dp,i} - 2I_{in,i}R_{s,i}, & I_{in,i} < I_{mp,i} \\ \frac{\partial P_{in,i}}{\partial I_{in,i}} &= R_{p,i}I_{ph,i} - 2(R_{s,i} + R_{p,i})I_{in,i}, & I_{in,i} \geq I_{mp,i}. \end{aligned} \quad (11)$$

The term, $-2(R_{s,i} + R_{p,i})I_{in,i}$, in the derivative typically leads to a steep decrease in panel power for $I_{in} \geq I_{mp}$. Absolute errors $|I_{in,i} - I_{mp,i}|$ impact the panel power less for $I_{in,i} < I_{mp,i}$. Accordingly, the algorithm adopted in this work attempts to minimize the error $|I_{in,i} - I_{mp,i}|$ with the following order of preference:

1) $I_{in,i} = I_{mp,i}$
2) $I_{in,i} < I_{mp,i}$
3) $I_{in,i} > I_{mp,i}$.

In the examples presented here, the DC-DC modules each continuously attempt to match the string current to their own MP currents according to the above algorithm. Generally, the modules can choose from a set of integral conversion ratios [0,1...Q_{max}]. The Q = 0 module configuration is important for good average tracking efficiency. It is equivalent to the pass-through mode discussed in reference [7] and represents the option for a panel to "sit out" when its maximum power is so low that including it in the string would have a negative impact on the global MPP.

C. Global Maximum Power Point Tracking

The string inverter can track the global MPP by adjusting its input current. Figure 5 depicts an example of the tracking efficiency achieved as I_o is swept, while the DC-DC modules adjust their conversion ratios. For this example, and for the rest of this section, tracking efficiency is considered in an otherwise lossless system ($\eta_c = 100\%$). Section IV addresses the effect of converter efficiency on MPPT control. The I_o

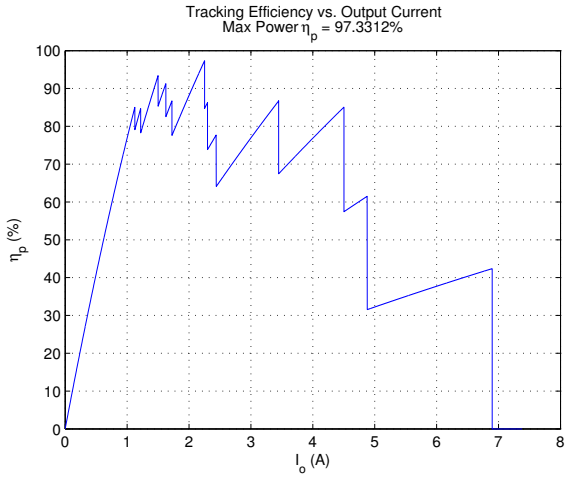


Fig. 5: A single I_o sweep: 3 panels, Q_{avail} = [0,1,2,3,4], $I_{mp,vec}$ = [6.898, 4.503, 4.878] A, $\Delta I_o = 1$ mA

sweeps, like the one depicted in Figure 5, may be performed on a scheduled basis. Alternatively, I_o may be varied continuously according to a particular runtime MPPT algorithm. Section IV-E presents a simulation of a likely input current-controlled inverter.

D. Statistical Performance Evaluation

A statistical performance evaluation method was adopted to account for variations in panel MPP's. Monte Carlo simulations were performed by allowing MATLAB® to choose random (normalized) $I_{mp,i}$'s for each panel. For each simulation, the string current, I_o, was swept as in Figure 5 and

the maximum efficiencies (tracking, converter, and total) were recorded. Repeating this many times and averaging the results yielded a prediction of average performance. An example output plot is shown in Figure 6. The plot in Figure 6 reveals

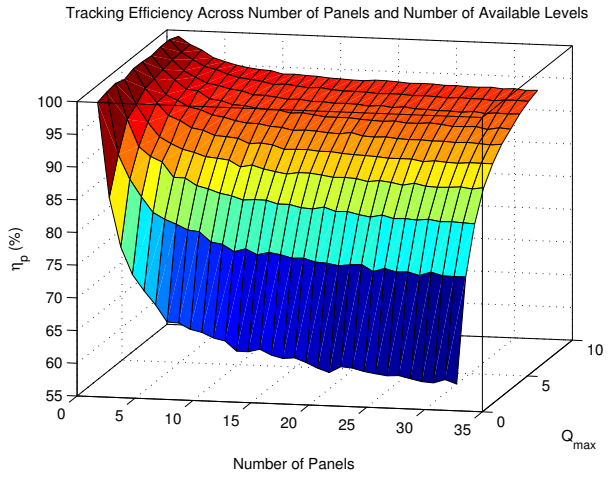


Fig. 6: Monte Carlo performance prediction: $Q_{avail} = [0 : 1 : Q_{max}]$, Monte Carlo Length = 200, $I_{o,sweep} = [0.01 : 0.02 : 6.93]$ A

that tracking efficiency can be very high for only a few panels. As panels are added, η_p diminishes to a limited extent. The local MPPT algorithm implemented impacts this behavior significantly. For instance, if the order of preferences listed in Section II-B is reversed, the tracking efficiency diminishes steadily as panels are added rather than flattening as it does in Figure 6. The Monte Carlo simulation results also show how average tracking efficiency improves as the number of available levels increases. The tracking efficiency predicted for a 3-panel, 5-level system is approximately 90%. Increasing the number of available levels to 8 increases the predicted tracking efficiency to 95%.

Finally, it should be noted that the $Q_{max} = 1$ case (i.e. $Q_{avail} = [0, 1]$) is somewhat representative of a simple series string of panels with bypass diodes. The statistical data predict roughly 65% average tracking efficiency while a 5-level MIC would improve that efficiency to roughly 90%

E. Effect of spatial panel separation

In the above example, the panels are assumed to have a random and uncorrelated distribution of MPP's. Intuitively, this model becomes inappropriate as panels become closely spaced. To model the effect of statistical correlation between MPP's for panels arranged in a non-infinite area, the randomly assigned panel MPP's can be constrained to a fraction of the full range. The simulation above was repeated having forced the MPP's to lie within 50% of the full range for each Monte Carlo iteration. The results show universally higher average tracking efficiencies. For instance, the tracking efficiency predicted for a 3-panel, 5-level system is approximately 95.5% and for a 3-panel, 8-level system, 97.4%.

F. Non-integral level selections

So far, we have considered only switched capacitor multilevel converters having integral, boosting sets of conversion ratios. There are many switched capacitor topologies that can achieve rational and bucking conversion ratios as well. Such a topology choice may be beneficial when considering upper bounds on DC bus voltages or other practical issues. A more thorough investigation will be the subject of future work.

III. Switched Capacitor Implementation

One particular realization of the switched capacitor MICs in Figure 1 is the Marx Multilevel converter. By forming series and parallel combinations of the the input source and the switched capacitors, the 5-level Marx converter shown in Figure 7 can achieve conversion ratios $Q_{avail} = [0, 1, 2, 3, 4]$.

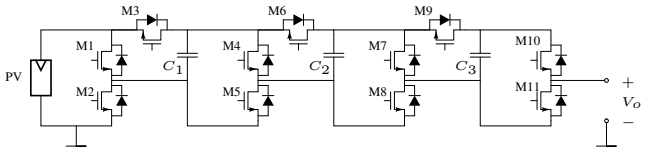
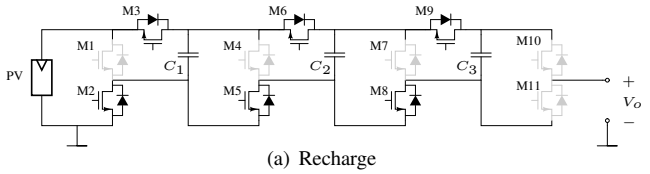


Fig. 7: A 5-Level Marx converter

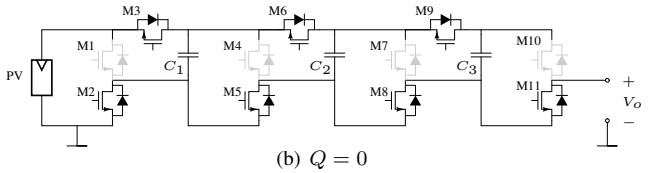
A. Efficient Switching Patterns

Switching cycles consist of a recharge phase, ϕ_1, and an output phase, ϕ_2. During ϕ_1, the switched capacitors are disconnected from the load and charged in parallel with the source. During ϕ_2, one of several series-parallel configurations of the switched capacitors and input source is chosen to achieve the desired conversion ratio. Many redundant switching configurations are possible. The switching configurations shown in Figure 8 were chosen for the 5-level Marx to minimize the conduction losses that will be quantified shortly. Generally, the switching configurations were chosen to minimize capacitor droop and the number of switches in the output current path, both of which lead to loss and load regulation. Rules of thumb to minimize capacitor droop include 1) utilize the input source to drive the output during ϕ_2 when possible and 2) utilize all of the switched capacitors when driving the output, e.g. parallel-connect redundant capacitors when possible.

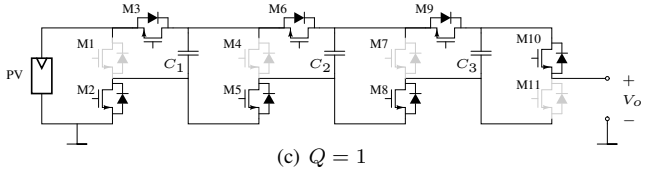
Switched capacitor circuits can achieve very high conversion efficiency by minimizing the instantaneous current flow through their effective output resistance, $R_{out,i}$. In a DC-DC switched capacitor circuit, the output is slowly-varying on the time-scale of one switching period. These facts guide us to particular modes of operation. In particular, efficient operation can be achieved when the same output phase (ϕ_2) configuration is repeated every cycle. In contrast, modulation of the ϕ_2 configuration on a per cycle basis, e.g. to achieve intermediate conversion ratios, would be ill-advised as it would lead to continuously varying open circuit converter voltages resulting in high instantaneous currents (high AC rms currents) through $R_{out,i}$. This observation leads directly to the constraint



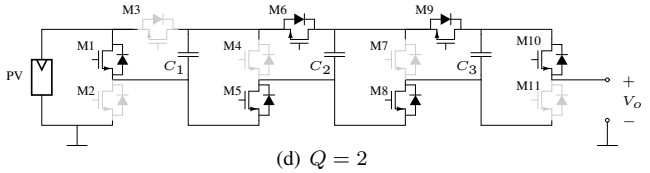
(a) Recharge



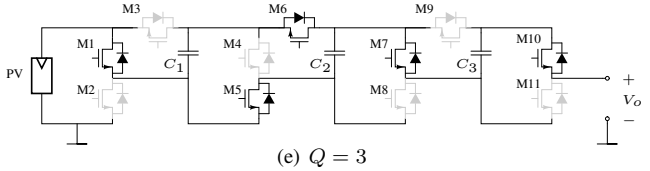
(b) $Q = 0$



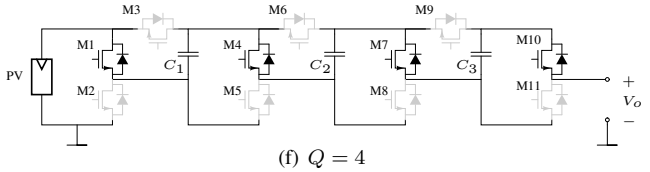
(c) $Q = 1$



(d) $Q = 2$



(e) $Q = 3$



(f) $Q = 4$

Fig. 8: Switching configurations

that the Marx Multilevel converter can (efficiently) achieve a discrete set of conversion ratios.

B. Linear Modeling

A linear modeling approach was adapted from the work in [34]. This linear modeling effort yielded quantitative support for the linear circuit models shown in Figure 1 including the output resistances, $R_{out,i}$ which represent both loss and load regulation in the switched capacitor circuits [34].

C. Switching Speed Limit Definitions

According to [34], loss and load regulation mechanisms can be differentiated among two switching speed limiting cases. In the slow-switching-limit (SSL), the switched capacitors fully equilibrate yielding impulsive capacitor currents. In the fast-switching-limit (FSL), the switched capacitors maintain fixed voltages while capacitor currents during each switching state are constant [34]. The two switching speed limits can be understood by considering the classic capacitor charging loss

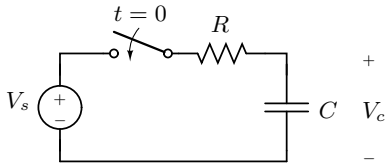


Fig. 9: The canonical circuit for studying the fundamental loss associated with charging a capacitor.

problem depicted in Figure 9. The total energy lost in charging the capacitor is the time-integral of $I_C(t)^2 R$:

$$E_{tot} = -\frac{(V_s - V_C(0))^2}{2R} RC \left(e^{-2t/RC} \right) \Big|_0^t . \tag{12}$$

In the SSL, the exponential term is allowed to collapse to -1 and the energy lost becomes

$$E_{tot,SSL} = \frac{1}{2} C \Delta V_C^2, \tag{13}$$

independent of R, and in agreement with the classical result. In the FSL, (12) can be viewed near $t = 0$ with the Taylor series approximation to the exponential term. This leads to

$$E_{tot,FSL}(t) = \frac{(V_s - V_C(0))^2 t}{R}, \tag{14}$$

i.e. the loss we would expect for two fixed voltages connected across the resistor. Reference [34] shows how these two loss mechanisms yield asymptotic limits to the output resistance with proportionalities

$$\begin{aligned} R_{SSL} &\propto \frac{1}{C f_{sw}} \\ R_{FSL} &\propto R_{ds,on}. \end{aligned} \tag{15}$$

The method developed in [34] for computing the multipliers to quantify R_{SSL} and R_{FSL} was adapted to the Marx Multilevel converter here. The results are summarized in Tables I and II for Marx converters having between two and eight available levels. Note that the multipliers in the tables need to be computed for each conversion ratio (switching pattern) for each number of available levels (topology). Also note that R_{FSL} depends on the duty ratio between ϕ_1 and ϕ_2, which was taken as $D = 0.5$ for all switching patterns here. Given the asymptotic limits, the actual output resistance for any combination of topology, C, f_{sw}, and $R_{ds,on}$ is generally

$$\boxed{R_{out} = \max(R_{FSL}, R_{SSL})} \tag{16}$$

and the conduction loss per module is simply

$$P_{rloss} = I_o^2 R_{out}. \tag{17}$$

D. Switching Loss

The linearized model above captures loss due to output current conduction. When evaluating the design in Section IV, it will also be important to include switching loss, a loss mechanism not explicitly contained in the linearized circuit

TABLE I: R_{SSL} Multipliers: ($\times 1/Cf_{sw}$)

Levels Available:	2	3	4	5	6	7	8
Q = 0	0	0	0	0	0	0	0
Q = 1	0	0	0	0	0	0	0
Q = 2	0	1	1/2	1/3	1/4	1/5	1
Q = 3	0	0	2	3/2	1	5/6	2/3
Q = 4	0	0	0	3	5/2	2	3/2
Q = 5	0	0	0	0	4	7/2	3
Q = 6	0	0	0	0	0	5	9/2
Q = 7	0	0	0	0	0	0	6

TABLE II: R_{FSL} Multipliers: ($\times R_{ds,on}$)

Levels Available:	2	3	4	5	6	7	8
Q = 0	2	4	6	8	10	12	14
Q = 1	2	4	6	8	10	12	14
Q = 2	0	8	10	12.4	8.2	17.6	32.4
Q = 3	0	0	26	24	38	48.4	50.8
Q = 4	0	0	0	64	90	100	100
Q = 5	0	0	0	0	130	180	206
Q = 6	0	0	0	0	0	232	307
Q = 7	0	0	0	0	0	0	378

model of Figure 1. The switching loss for any active switch (one that changes state between the two switching phases) can be quantified by considering the circuit shown in Figure 10. All MOSFETs in the Marx converter reside in at least one loop

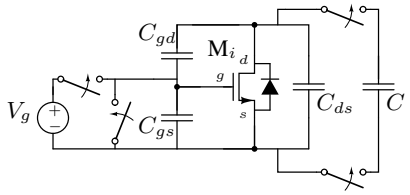


Fig. 10: Switching loss evaluation in the Marx converter for active MOSFETs

consisting only of one or two other MOSFETs and a switched capacitor. In the Marx converter, the switched capacitor, C, in Figure 10 will nominally exhibit a voltage equal to the panel voltage, V_{in}, because it is recharged to that potential each cycle. The total switching loss was estimated in terms of typical data sheet values using [35] for N active devices as

$$P_{swloss} = N\left(Q_g V_g + \frac{1}{2}Q_{oss}|V_{in}| + Q_{rr}|V_{in}|\right) f_{sw}. \quad (18)$$

Examining the switching patterns shown in Figure 8, one can extract the following pattern generalizing the number of active switches according to conversion ratio:

$$\begin{aligned} N &= 1, & Q &= 0 \\ N &= 3Q - 2, & Q &> 0. \end{aligned} \quad (19)$$

E. Inherent Features

Inherent to the topology of the Marx converter are a few interesting features that may add significant value to a solar power system. As mentioned previously, the Marx converter has a natural pass-through feature, replicating the function of bypass diodes and also the pass-through mode presented in [7].

The ability to disconnect each module from the load may be beneficial when implementing safety disconnect features. Reference [36] discusses the need for a disconnect in the event of a fire to prevent electrocution hazards that would otherwise result from the high voltage string output. This disconnect feature may also be particularly beneficial in implementing an anti-islanding mode. A good discussion of anti-islanding control and solutions for solar power systems can be found in [37].

The run-time local MPPT algorithm described above can be designed to automatically prevent under-voltage conditions at the panel output. Because the DC-DC modules continuously choose Q_i to closely match $I_{in,i}$ to $I_{mp,i}$, they automatically adjust to over current conditions, choosing $Q_i = 0$ in the limiting case. This feature is advantageous when the local control circuitry is powered by the panel itself.

F. Gate Drive

The gate drive for the Marx converter needs to operate with a continuous floating gate drive voltage. The converter itself does not guarantee a periodic charging path to recharge a bootstrap capacitor. A level shift circuit is also required to translate ground-referenced logic signals to the gate drive output. The recommended topology (not necessarily the specific parts), adapted from [38], is shown in Figure 11.

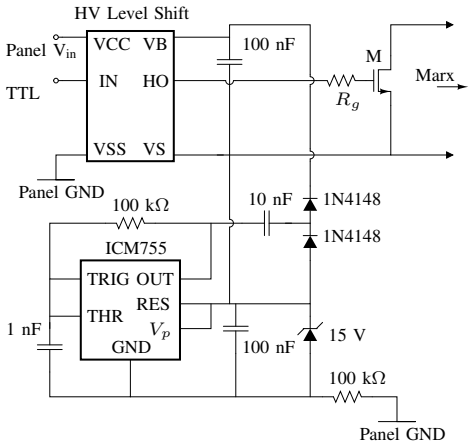


Fig. 11: The recommended gate drive adapted from IR AN-978 [38].

The 555 timer IC, 1N4148 diodes and floating capacitor form a charge pump circuit. The 100 kΩ resistor between the 555 timer GND and Panel GND and the 15 V zener allows the timer IC to float 15 V below the source of the driven MOSFET. The low power version of the 555 timer IC (ICM755) is needed in this circuit to achieve low power dissipation in the part itself and to achieve sufficient quiescent current despite the 100 kΩ resistor to ground. The charge pump drives the V_B node to twice its supply voltage referenced to its own floating GND leading to a 15 V floating drive referenced to the MOSFET source. This voltage can be adjusted by choosing the voltage of

the Zener diode. The "HV Level Shift" could be a commercial high side driver IC such as the IR2125. However, the high voltage rating of such a part would be under-utilized for a typical implementation of the system in this work. Therefore, a more cost-effective gate drive would include a custom level shift circuit.

IV. Design Example

A 3-panel 510 W system was designed and simulated in SPICE and in MATLAB®. Among the key topological considerations for implementing a practical Marx DC-DC MIC is the need for a power diode in series with the output of each module. This diode is required to block current from conducting backwards through the body diode of the upper MOSFET in the output stage during ϕ_1. In order to alleviate any need to synchronize switching action among modules, a local output non-electrolytic capacitor was placed across each module to create a local DC bus.

A. Number of Levels

The number of levels was chosen using the same Monte Carlo prediction methods described in Section II-D. Having enumerated loss mechanisms, total efficiency was used to determine performance. To choose an appropriate number of levels, an unoptimized but lossy system was simulated using nominal circuit parameters and MOSFET device characteristics. The predicted performance is plotted in Figure 12. The data show diminishing returns in total efficiency beyond 5 levels. Therefore a 5-level Marx converter was chosen as the MIC.

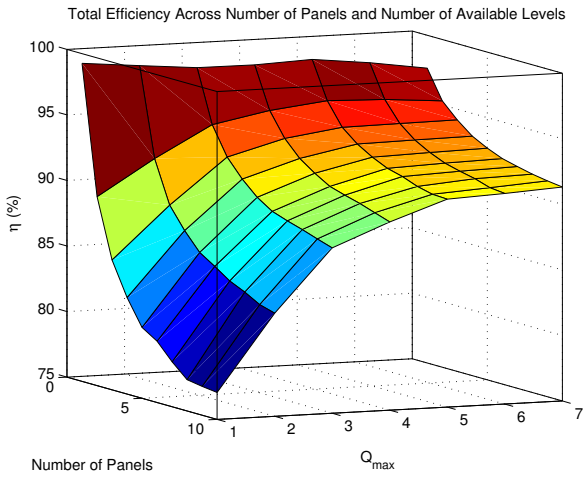


Fig. 12: Unoptimized system performance prediction: $Q_{avail} = [0 : 1 : Q_{max}]$, Monte Carlo Length = 400, $I_{o,sweep} = [0.01 : 0.02 : 6.93]$ A, C = 12.5 μF, f_{sw} = 250 kHz, $R_{dson} = 10$ mΩ, Q_g = 10 nC, Q_{oss} = 5 nC, Q_{rr} = 25 nC,V_g = 15 V, V_{oc} = 29 V, V_{mp} = 24.6 V, I_{sc} = 7.38 A, I_{mp} = 6.93 A, Distribution Compression = 50%

B. MOSFET Choice and Switching Frequency Optimization

Having chosen a reasonable value for the non-electrolytic (metal film) switched capacitors in the 5-level marx, the choice of MOSFET and switching frequency were optimized together. It is significant that all MOSFETs in the Marx converter reside in loops containing a switched capacitor and other MOSFETs only. MOSFET drain-source voltages are therefore upper bound by the maximum panel voltage. Accordingly, it is particularly advantageous to choose a panel whose open-circuit voltage is just below a standard value for V_{dss}. Oversizing the MOSFET beyond the required V_{ds} rating would lead to unneeded switching or conduction loss and a suboptimal design. A number of likely MOSFETs were identified having $V_{dss} = 30$ V for the panel open-circuit voltage of 29 V. The likely MOSFETs were chosen based on their on-resistance, $R_{ds,on}$, and gate capacitance, C_g. With the losses derived in (17) and (18), the performance was plotted for each MOSFET across switching frequency and conversion ratios. Figure 13 shows such a plot for the selected MOSFET. A maximum average converter efficiency (across all conversion ratios) of $> 98\%$ was predicted at a switching frequency of 360 kHz. Note that the gate drive voltage was decreased from 15 V

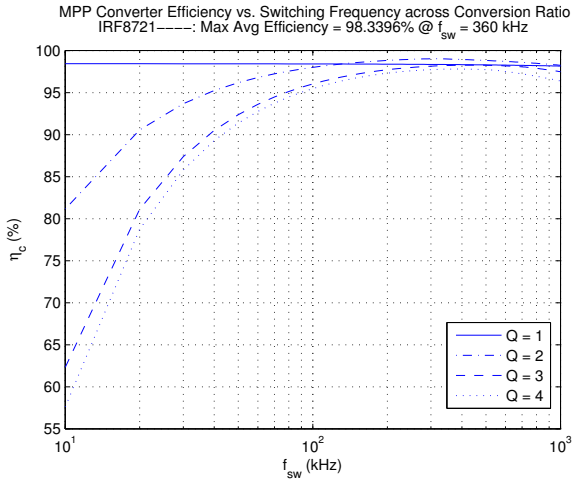


Fig. 13: MOSFET and switching frequency evaluation at peak power: IRF8721, C = 12.5 μF, V_{mp} = 24.6 V, I_{mp} = 6.93 A, MP = 170 W, V_g = 10 V

in the unoptimized system to 10 V in the optimized system. Adjusting the gate drive voltage trades off conduction loss (on-resistance) for switching loss.

C. Power Diode

The power diode was chosen primarily to support the peak output current and to block the peak reverse voltage safely. Secondly, it was chosen for low capacitance, forward voltage, and ESR. Having added output diodes to the implemented

system, the additional losses can be estimated as follows:

$$V_{fwd,i} = \ln\left(\frac{I_o}{I_s+1}\right) n\frac{kT}{q} + ESR_{diode} I_o \quad (20)$$

$$P_{diode} = I_o \sum_i V_{fwd,i} + f_{sw} C_{j,i} V_{rr,i}^2, \quad (21)$$

where V_{rr} is the reverse voltage during ϕ_1 and C_j is the junction capacitance of the diode. This expression can be used to improve the accuracy of the Monte Carlo performance predictions. The power diode chosen for this example was the Motorola MBR20100C Shottky [39]

D. Simulated Prototype

The optimized system was simulated using SPICE and MATLAB®. The performance of this system was predicted with Monte Carlo methods having incorporated the losses derived in (17), (18) and (21). The results are shown in Table III. A summary of circuit elements selected for the simulated prototype is shown in Table IV.

TABLE III: Simulated statistical performance: 5-level, 3 Panel optimized system: Monte Carlo Length = 100, Distribution Compression = 50%, $\Delta I_o = 1$ mA, Diode Loss = [on]

efficiency	symbol	simulated result
tracking	η_p	95.43%
conversion	η_c	97.56%
total	η	93.10%

TABLE IV: Circuit component summary

Component	Part No. / Value	Note
Switched Capacitors, Output Capacitor	12.5 μF	Metal Film 1 $\parallel$ 4.7 $\parallel$ 6.8 μF
Panel Capacitor	25 μ F	12.5 $\parallel$ 12.5 μF
MOSFET	IRF8721	
Output Diode	MBR20100C	

It is important to realize that the central inverter cannot track panel power, corresponding to η_p, directly. Instead it tracks its input power, corresponding to η. Having incorporated the loss mechanisms from Section III and in equation (21), this observation was accounted for in simulation by allowing the inverter to choose the I_o that maximized its input power. Tracking efficiency was recorded for comparison to total efficiency.

A single experiment was performed in simulation to validate the linear modeling effort and loss calculations above. A fixed set of conversion ratios and MPPs was chosen for the three panels. Tracking, conversion, and total efficiencies were plotted for a single I_o sweep. Figure 14 compares the results for calculated data based on Section III and equation (21), a SPICE simulation of the linearized model and a SPICE simulation of the MOSFET system. The difference in η_c between the linearized model and the other two data sets represents switching and output diode loss. Errors between the calculated model and FET simulation are likely due to estimation errors in computing diode and switching losses. Note that in the plots of Figure 14, the maximum in total efficiency lines up closely with the maximum in tracking efficiency.

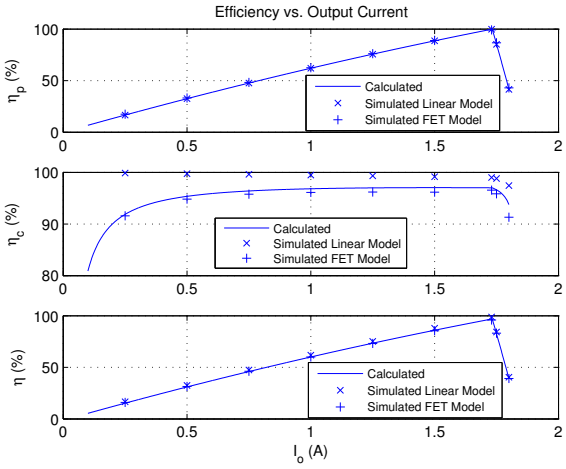


Fig. 14: Model Validation: Single I_o sweep, 3 sources, Q = [0, 2, 4], $I_{mp,vec}$ = [0.007 3.465 6.93] A, $C = 12.5$ μF, $f_{sw} = 360$ kHz, MOSFET: IRF8721, $V_g = 10$ V, deadtime = 100 ns, $R_g = 4\ \Omega$

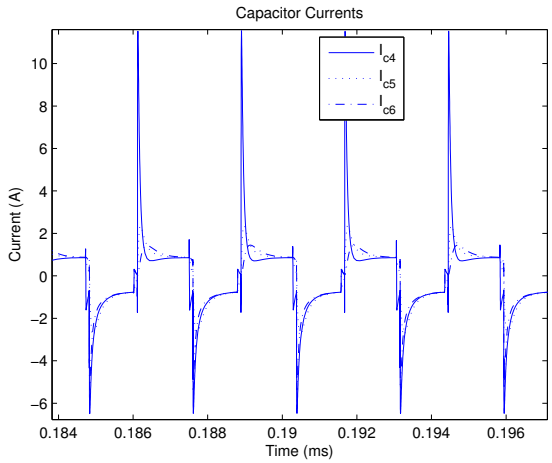
Time domain waveforms from the simulated system are shown in Figure 15. Figure 15(a) shows a zoom-in of the capacitor currents. The shape of those currents indicates operation between the slow and fast switching limits defined in Section III-C. This result is a natural outcome of the MOSFET choice and switching frequency optimization step above. Figure 15(b) shows panel input currents during a step change in the load current from 90% to 100% of the predicted maximum power current. In this example, Panel 1 is bypassed ($Q_1 = 0$) because its MPP is quite low; $I_{in1} = 0$ in the plots. The other two panels initially settle close to their respective $I_{mp,i}$'s - Panel 2 exhibits half of the photovoltaic current that Panel 3 does. When the load current steps to its maximum power value, I_{in2} and I_{in3} settle on their respective $I_{mp,i}$'s.

E. DC AC Dynamics

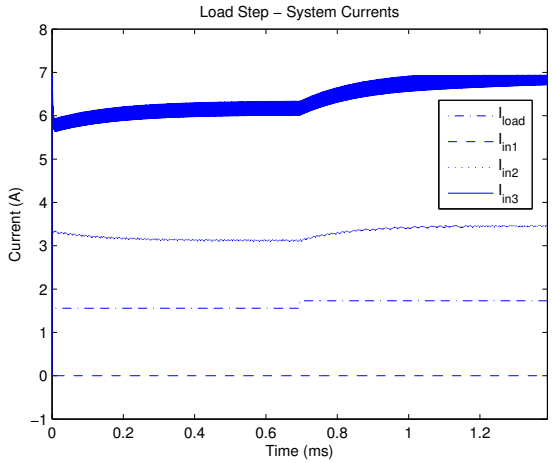
A linearized model of the central input current-controlled inverter is shown in Figure 16. The closed-loop transfer functions of particular interest can be derived from that circuit. They are

$$\frac{\hat{i}_{in}}{\hat{v}_{in}}(s) = \frac{M^2(D)}{sL_e + R_e + R \parallel \frac{1}{sC}} \left(\frac{1}{1+T(s)}\right) \quad (22)$$

$$\frac{\hat{i}_{in}}{\hat{v}_{ref}}(s) = \frac{A(s)}{1+A(s)F(s)}, \quad (23)$$



(a) Capacitor Currents



(b) Load Step - Currents

Fig. 15: Time-domain waveforms.

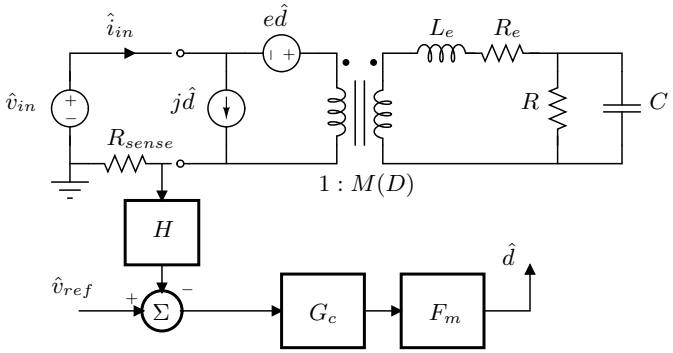


Fig. 16: A linearized model of an input current-controlled inverter front-end.

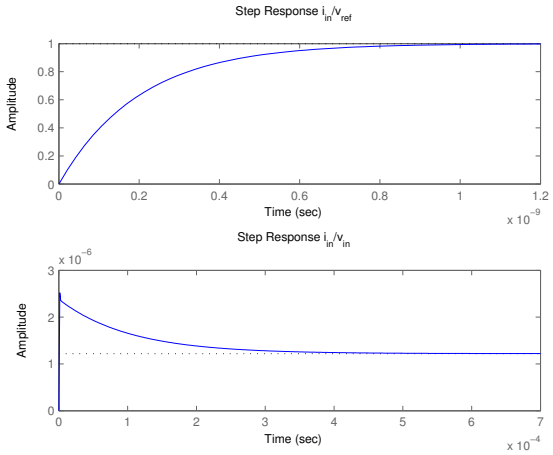


Fig. 17: Inverter closed-loop step responses

where

$$A(s) = G_c(s)F_m\left(j(s) + e(s)\frac{M^2(D)}{sL_e + R_e + R \parallel \frac{1}{sC}}\right) \quad (24)$$

$$F(s) = HR_{sense} \quad (25)$$

$$T(s) = AF. \quad (26)$$

The linear model parameters, e, j, $M(D)$, L_e, and R_e were chosen for a 500 W buck-derived inverter topology.[1] Figure 17 shows step responses of the closed-loop transfer functions in (22) and (23). They show relatively fast settling times in the input current upon step transients in the input voltage (corresponding to the string DC bus voltage) and the reference voltage (corresponding to the control for the sweepable input current). The lower plot also indicates a significant attenuation of the input current response to changes in the input voltage. This attenuation is largely dependent on the low-frequency magnitude of the loop gain $T(s)$ as indicated by equation (22).

[1]See reference [40] Chapter 8 for a supporting discussion.

V. Conclusions and Further Work

Widespread grid penetration of PV will rely on the reduction of capital cost and total cost of ownership for solar power systems. It is critical that these factors guide the design of photovoltaic power circuits and system architectures. This work has presented a full system approach utilizing switched capacitor multilevel DC-DC converters. Substantial cost reductions may be possible by providing per panel MPPT without the need for per panel magnetics. Coupling the DC-DC modules with a ripple port inverter eliminates the need for electrolytic capacitors, enabling long-life operation.

Topics of ongoing research include investigation of MPPT algorithms and related system level tradeoffs for control of the central inverter. There exist necessary tradeoffs among switching frequency, converter efficiency, and global tracking efficiency (I_o step size) when considering the dynamics and runtime MPPT approaches for the full system. Not addressed in this work was the dual case of paralleled strings of panels. This will also be a topic of ongoing investigation.

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