VAMPIRE: A Magnetically Self-powered Sensor Node Capable of Wireless Transmission

Jinyeong Moon, John Donnal, Jim Paris, Steven B. Leeb
Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA 02139, USA

***Abstract*—This paper presents a power electronic topology for providing a vibration monitor with in-situ magnetic energy harvesting. The energy harvesting circuit uses low voltage MOSFETs and a nano-crystalline magnetic core to extract energy from an operating electrical load like a motor. This topology can be used to power sensors and wireless circuitry for diagnostics with no need for battery or special power wiring. Harvesting energy from a 90 W-60 Hz load, a Vibration Assessment Monitoring Point with Integrated Recovery of Energy (VAMPIRE) produces 7.5 mW with the core volume of 2.9 cm^3, and powers up a 6.5 mW electrical monitor that provides sampling, signal processing, and periodic wireless data transmission through an RF channel. The system samples the vibration data at 125 Hz, and enables wireless burst transfer every 160 ms.**

***Index Terms*—Magnetic Coupling, Energy Harvesting, Magnetic Saturation, Transformer, Vibration Assessment**

I. Introduction

In sensor-monitoring applications, there is a great attraction to a "dual-use" design philosophy. Dual-use seeks to piggyback or squeeze extra functions from existing systems and structure. For example, we are developing a vibration monitor we call VAMPIRE that can be designed or retrofit into equipment to be monitored [1]. This nonintrusive vibration monitor requires no ohmic electrical connections to the existing system. This vibration monitor is built around a magnetic core much like a current-sense transformer. The toroidal transformer of VAMPIRE self-powers from the magnetic fields around a wire feeding an electromechanical load of interest, e.g., a motor. This monitor could store data for later retrieval, or communicate wirelessly, or potentially communicate with a nonintrusive load monitor (NILM) collating data via a power line carrier modem [2]-[4]. The system is maintenance-free and easily installed as part of a new or retrofit motor enclosure cover. It could also measure temperature and other important diagnostic indicators.

A prototype of our VAMPIRE sensor node is shown in Fig. 1. This is similar to a current transformer, but it differs in that it has a goal of extracting power from the monitored line in useful amounts. The current-driven transformer is limited for power delivery by magnetic saturation of the core, which, along with the distortion in rectification, restricts power transfer to the secondary side.

Design constraints for the necessary power electronics can be explored in the context of a specific example. For vibration monitoring of utility-frequency electromechanical actuators

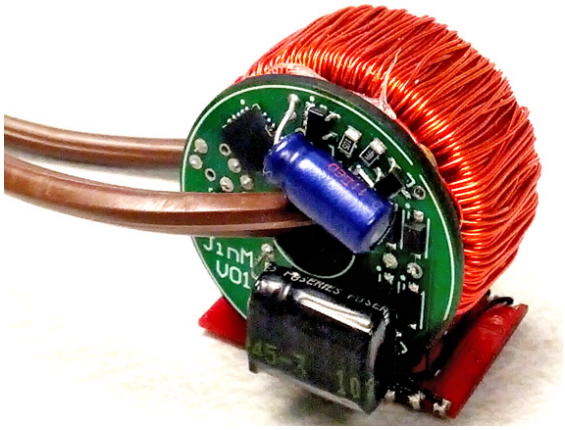


Fig. 1. Physically Built and Operational VAMPIRE

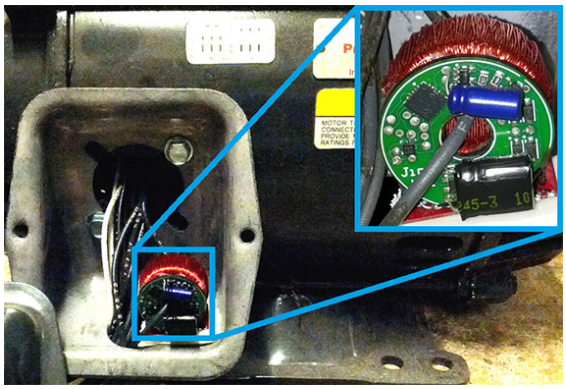


Fig. 2. Notional VAMPIRE installation in a NEMA enclosure

like motors, VAMPIRE needs to be conveniently attached to (or enclosed in) the equipment to be monitored. An illustration of a typical VAMPIRE installation is shown in Fig. 2. For this example, a reasonable target size of the core is shown in Fig. 3, limited by the physical dimensions of the terminal box of a typical motor NEMA enclosure. The design discussion in this paper will focus on this example and the physical dimensions as given in Fig. 3, with the understanding that the analysis can be extended to other situations and core dimensions.

Power requirements for VAMPIRE are determined by the needs of the sensors, digital monitoring package, and wireless communicator necessary for in-situ vibration monitoring for

978-1-4673-4355-8/13/$31.00 ©2013 IEEE

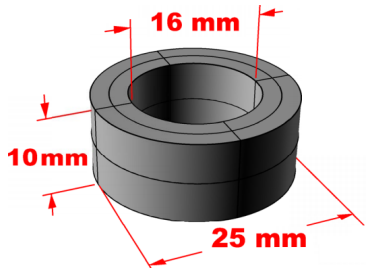


Fig. 3. Physical Dimensions $\left(A_{\text{FLUX}} = 0.36\,\text{cm}^2, l_{\text{FLUX}} = 6.44\,\text{cm}\right)$

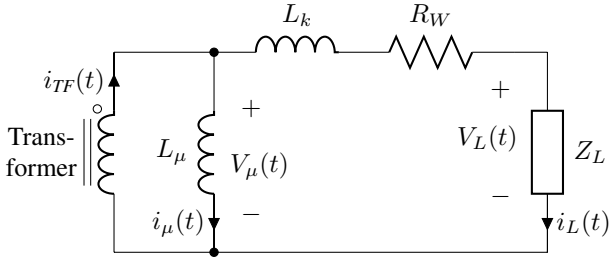


Fig. 4. Secondary Side Circuit Model

condition-based maintenance applications. For our prototype, sensing, signal processing, and communicating require an average power consumption of 6.5 mW at 125 Hz data sampling rate with a 2 V supply rail. This considers the minimum supply voltage of 1.8 V for the VAMPIRE monitoring package and 200 mV headroom. Therefore, a core and associated power electronic circuit should be designed in accordance with these constraints.

Fig. 4 shows a model of the secondary side of the magnetic core in VAMPIRE. To get a first cut at predicting the power capability of the core, assume ideal inductors, hence no magnetic saturation, for the transformer. Also, assume initially that wire resistance and leakage inductance are negligible ($R_W = 0$, and $L_k = 0$). With an ideal core without the magnetic saturation, the magnetizing inductance is

$$L_\mu = \mu_r \mu_0 \cdot N^2 \cdot \frac{A_{\text{FLUX}}}{l_{\text{FLUX}}} \tag{1}$$

The idealized peak voltage at the load, $V_L(t)|_{\text{MAX}}$, which is an upper bound of the load voltage in Fig. 4, can be calculated by a voltage divider. This peak voltage must be larger than $\sqrt{2} \cdot V_{\text{RMS}} = \sqrt{2} \cdot 2\,\text{V} = 2.828\,\text{V}$.

$$\begin{aligned} V_L(t)|_{\text{MAX}} &= \frac{I_{PRIMARY}}{N} \cdot |R_L \;//\; j\omega L_\mu| \\ &= \frac{I_{PRIMARY}}{N} \cdot \frac{R_L \cdot \omega L_\mu}{\sqrt{R_L^2 + \omega^2 L_\mu^2}} > 2.828\,\text{V} \end{aligned} \tag{2}$$

The equations, (1) and (2), indicate that, in this idealized design process, there are two key design variables: μ_r and N. Given the equipment to be monitored is fixed, for example, a 90 W-60 Hz desk lamp in our case, I_{PRIMARY} and ω are fixed. Also, modeling the VAMPIRE power consumption as a resistive load, R_L is a fixed value as well, which can

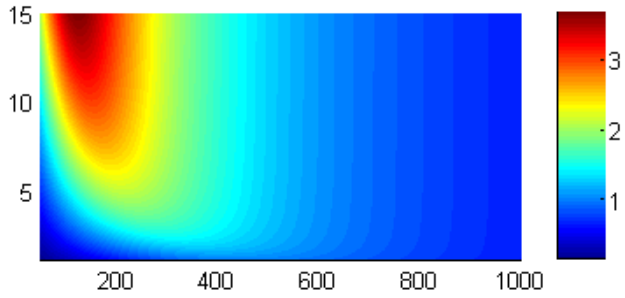


Fig. 5. $V_L(t)|_{\text{MAX}}$ with ideal components
(Color Gradient: Peak Voltage [V], Y-axis: μ_r [in 10k], X-axis: N [#])

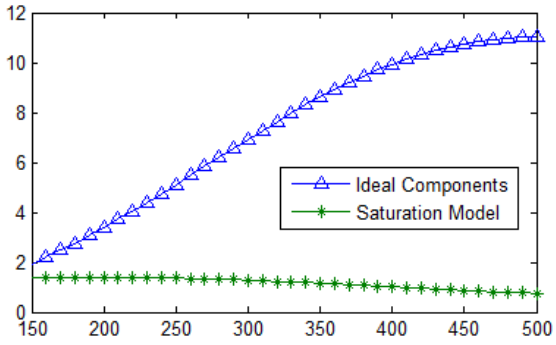


Fig. 6. Harvested Power Comparison with MAX $(\mu_r) = 150,000$
(Y-axis: Power [mW], X-axis: N [#], in Saturated Condition)

be substituted with $615\,\Omega$ in our VAMPIRE case. With the two key variables, we might imagine, for example, using a known core material with μ_r of $10,000$, an easily obtainable permeability at utility-frequencies, and the core dimensions as in Fig. 3. Unfortunately, Fig. 5, which is a space spanned by all possible design points, reveals that such a choice with μ_r of $10,000$ will provide an output voltage less than 1 V regardless of N, the number of turns in the secondary side. Furthermore, the output voltage will be even lower if we take into account other nonidealities, such as magnetic saturation and voltage drop in a rectifier.

Even with ideal components, VAMPIRE is not viable with widely available cores. When we consider magnetic core saturation, it becomes much harder to make VAMPIRE work. As an example, Fig. 6 illustrates these difficulties, where the harvested power of the saturation case is poor compared to the ideal case, harvesting less power with larger N. A more sophisticated design is necessary to create a successful VAMPIRE energy harvester. However, designing a core requires a considerate analysis of the effects of subsequent power electronic circuits. As will be explored in the follwing sections, the core's load is a supercapacitor through a rectifier, which can be considered as a constant voltage source. Exploiting it along with the core being a current-driven transformer, we can design the core independently, with this voltage as a variable.

In this paper, we will explain the limits induced by saturation, develop a core design strategy to achieve maximum power extraction, and design circuit topologies for harvesting maximum practical power from the VAMPIRE transformer.

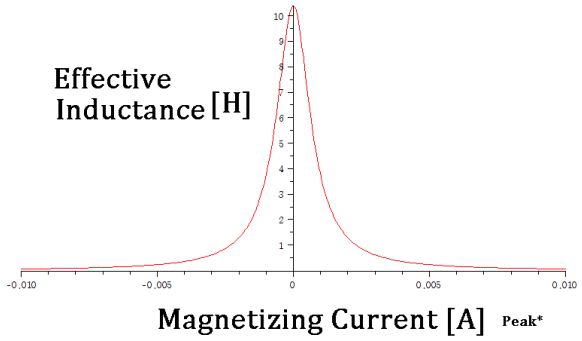


Fig. 7. Effective Magnetizing Inductance vs. Magnetizing Current

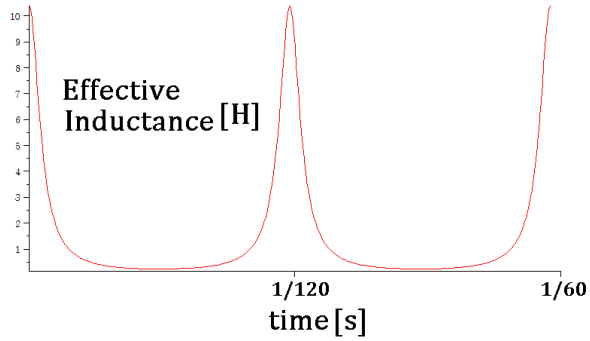


Fig. 8. Effective Magnetizing Inductance over Time (60 Hz Current Injection)

II. Core Modeling and Saturation Analysis

A. Mathematical Modeling of Magnetic Core Saturation

1) Amorphous Nanocrystalline Core:

As illustrated in Fig. 5, even with the ideal components, a magnetic core with μ_r larger than $100,000$ is required to achieve reasonable output voltage level. Most commercially available cores have maximum permeability of less than $30,000$ while amorphous nanocrystalline cores are capable of providing maximum permeabilities larger than $150,000$ at $60\,\text{Hz}$ [5]. We chose this type of core for our design considering sufficient maximum permeability at utility-frequency. With high permeability core materials, saturation occurs at relatively low winding currents. There are two approaches to model this nonlinear behavior.

2) Modeling from Maxwell's Equations:

One way to model the saturation behavior of the magnetic core is to create a nonideal transformer with ideal inductors associated with it. We can calculate the magnetic field, H, inside the core, given the core shape and dimensions, and relate it to the magnetic flux density, B, according to the nonlinear B-H curve of the material. Plugging this B into Maxwell's equations, and combining it with KVL of the secondary side, we get a nonlinear differential equation. When solved, we can get a distorted saturation current coming out of the transformer if the core is indeed in the saturation regime. This is a physical modeling, based on the most fundamental principle of physics. However, the differential equation tends to be extremely nonlinear and complex, and hardly provides us with any insight. Furthermore, it is even harder to solve the system if the core is connected to other nonlinear components, for example, a rectifier.

3) Circuit-based Modeling:

A more tractable approach is to create an ideal transformer with nonideal inductors associated with it. The new model can be represented by the same secondary side circuit as given in Fig. 4. Since the transformer is now ideal, we can use a circuit model for the transformer and avoid the higher order derivatives introduced by Maxwell's equations in the previous model. By definition, a nonideal inductor can arbitrarily change its inductance over time regardless of a fixed frequency. Therefore,

$$V_\mu(t) = \frac{\mathrm{d}\mathit{Flux}(t)}{\mathrm{d}t} = \frac{\mathrm{d}\left[L_\mu(t) i_\mu(t)\right]}{\mathrm{d}t} \neq L_\mu(t)\frac{\mathrm{d}i_\mu(t)}{\mathrm{d}t} \tag{3}$$

In order to express the relationship between voltage and current of such a nonideal inductor, we need to consider a magnetic flux equation, and this is where the core saturation is modeled. The inverse tangent function is chosen to describe the saturation behavior when the current through the magnetizing inductor becomes large.

$$\mathit{Flux}(t) = \Lambda(t) = \Lambda_{\text{MAX}} \cdot \frac{2}{\pi}\arctan\left(\frac{N}{\alpha} i_\mu(t)\right) \tag{4}$$

For the equation (4), we need to estimate two material-related parameters, B_{SAT} (in Λ_{MAX}) and α, where B_{SAT} is the saturated magnetic flux density, and $1/\alpha$ is the sensitivity to the current in a non-saturated region (similar to μ_r). Combining (3) and (4), we finally get the relationship between voltage and current of a nonideal inductor.

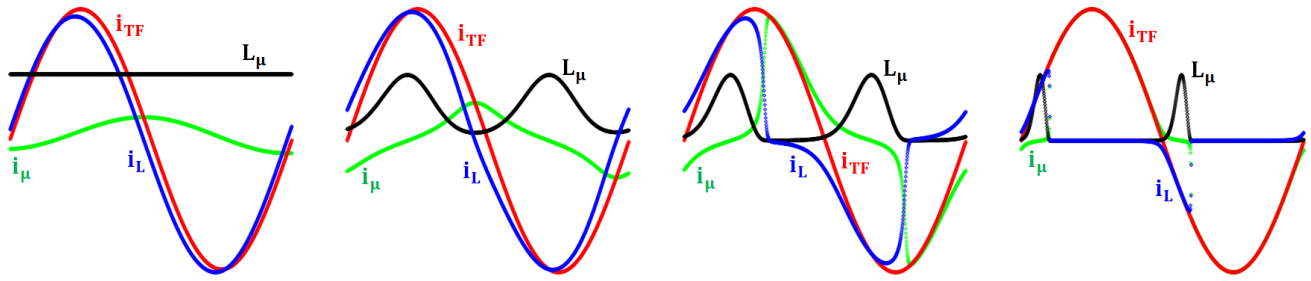
$$\begin{aligned} V_\mu(t) &= \frac{\mathrm{d}}{\mathrm{d}t}\left[\Lambda_{\text{MAX}} \cdot \frac{2}{\pi}\arctan\left(\frac{N}{\alpha} i_\mu(t)\right)\right] \\ &= \Lambda_{\text{MAX}} \cdot \frac{2}{\pi} \cdot \left(\frac{\alpha N}{\alpha^2 + N^2\, i_\mu(t)^2}\right) \cdot \frac{\mathrm{d}i_\mu(t)}{\mathrm{d}t} \end{aligned} \tag{5}$$

In this modeling, we will consider the transformer in Fig. 4 as ideal with the equation (5) for the magnetizing inductor. Leakage inductance has been ignored in this analysis because experimental measurements show that leakage is less than 1% of the magnetizing inductance.

If we define the effective inductance as $\mathrm{d}\mathit{Flux}(t)/\mathrm{d}i_\mu(t)$,

$$L_{\mu,\text{eff}}(t) = \Lambda_{\text{MAX}} \cdot \frac{2}{\pi} \cdot \left(\frac{\alpha N}{\alpha^2 + N^2\, i_\mu(t)^2}\right) \tag{6}$$

We can verify that $L_{\mu,\text{eff}}(t)$ indeed depends on the current through it, as in Fig. 7, and changes over time even at the fixed frequency, as illustrated in Fig. 8. The transformer is no longer a 'good current source' since the parallel impedance periodically becomes near-zero, and most of the power is flowing through the source impedance rather than the load.



(a) No Saturation (b) Soft Saturation (c) Saturation (d) Hard Saturation

Fig. 9. Simulation of the Core Saturation with Increasing Current Amplitude (scaled accordingly)

Only a small fraction of the power is transferred when the magnetizing inductance is maintained well above zero around the peaks.

If we apply KVL around a load, we get

$$V_\mu(t) = [i_{TF}(t) - i_\mu(t)] \cdot R_W + V_L(t) \tag{7}$$

Since we modeled all the nonidealities in the magnetizing inductance, $i_{\mathrm{TF}}(t)$ is a perfect sinusoid. Then, by combining this perfect sinusoid with (5) and (7), we get the model below.

$$\begin{aligned} &\left[\frac{I_{PRIMARY}}{N}\sin(2\pi f t) - i_\mu(t)\right] \cdot R_W + V_L(t) \\ &= \Lambda_{\mathrm{MAX}} \cdot \frac{2}{\pi} \cdot \left(\frac{\alpha N}{\alpha^2 + N^2\, i_\mu(t)^2}\right) \cdot \frac{\mathrm{d}i_\mu(t)}{\mathrm{d}t} \end{aligned} \tag{8}$$

B. Saturation Analysis

The circuit-based modeling, given in (8), also becomes complicated if we insert rectification circuitry with general impedance as a load (for example, a large capacitor with parasitics). However, unlike the model developed with Maxwell's equations, we can still develop an insight since everything is a circuit element. For the purpose of developing an insight, we will first use a simple resistor as a load, and provide a qualitative analysis of magnetic saturation from a circuit designer's perspective.

1) Back-of-the-Envelope Analysis with Resistive Load:

Let us first consider the circuit, Fig. 4, without solving (8). Since the impedance of the magnetizing inductor is not infinite, there must be a finite current through it, and the current changes with a certain phase delay with respect to the transformer's sinusoidal current. While the transformer current changes, if the magnetizing current increases and is large enough, the flux will start to saturate and its time derivative, $V_\mu(t)$, will drop to zero, which means the impedance of the path will decrease to zero (becoming a short path). As a result, L_μ draws more current from the transformer, and the increased current will expedite the saturation in turn, eventually rerouting all the transformer current to the magnetizing inductor. This positive feedback is the essence of the core saturation analysis, and drastically lowers power transfer to the load.

2) Numerical Simulation with Resistive Load:

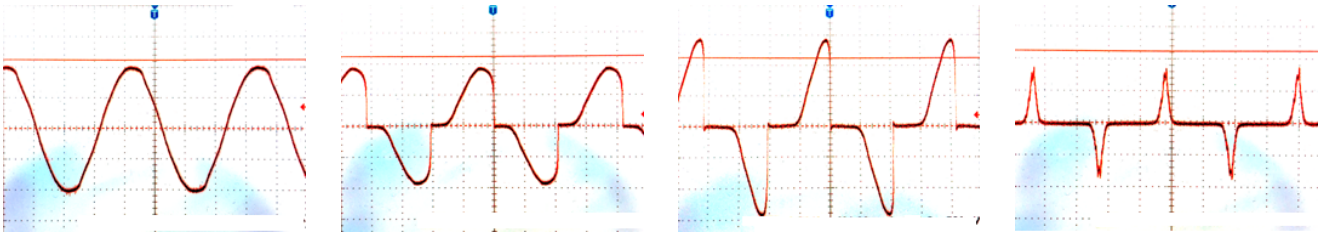
By solving the suggested model, four cases with different levels of the core saturation are presented in Fig. 9. Please note that, in order to compare four cases with ease, the waveforms in each case are normalized by the maximum value of i_{TF}, and L_μ is scaled to half the height of the maximum value of i_{TF}.

In Fig. 9(a), which has a low transformer current, hence a non-saturated core, i_μ is proportional to i_L with 90° lag as in an ideal RL circuit. Since the core is not saturated, the magnetizing inductance is approximately constant over the cycle.

In Fig. 9(b), where the transformer current is significantly increased compared to (a), the phase difference between i_μ and i_L is still close to 90°. However, the difference is that the magnetizing current is rapidly amplified as it increases toward the plot center. The rapid amplification goes on until it meets i_{TF} and generates the peaking. (This is done by the aforementioned positive feedback of the saturation.) Due to this peaking, the load current starts to get a distortion by the same amount. And, as expected, the effective magnetizing inductance, L_μ, is very low around where i_μ peaks. One thing to note is that even though the left and right side of the i_μ with respect to the center of the plot look symmetric, they are not. The qualitative reason is that, when i_μ was increasing, L_μ was falling, and smaller inductance allows faster current change. This is the same positive feedback again, and the same thing can be said for the case of decreasing i_μ. As a consequence, L_μ hits zero faster than it recovers from it. This asymmetry is also reflected in i_L.

In Fig. 9(c), the magnetizing current is even more rapidly increasing to i_{TF}. After the peaking, decreasing i_μ eventually gets the core out of the saturation, and L_μ is again restored. We can also see that rising L_μ results in much slower current drop compared to current rise in falling L_μ, as explained in (b). In this case, i_μ's zero crossing point happened with around 90° lag with respect to i_{TF}'s, but the peaking point does not keep the same phase difference anymore due to the saturation.

In the extreme case of hard saturation, Fig. 9(d), the phase difference between i_{TF} and i_μ is meaningless because i_μ is mostly identical to i_{TF} except where i_{TF} itself is around 0. This is because the core is almost always saturated due to the large transformer current, and L_μ is rather a short circuit for



(a) No Saturation (b) Saturation (c) More Saturation (d) Hard Saturation

Fig. 10. Scope Measurements of i_L (magnitude not scaled)

the time being. Power is transferred to the load only in the 'cat ear' region, where i_L is not 0.

3) Core Saturation Measurement with Resistive Load:

Since $i_L = V_L/R_L$, the shape of the voltage across the load resistor will be the same as that of the load current except for a scale factor. The scope measurement screenshots of the load current are presented in Fig. 10. Although the magnitudes are not scaled, we can verify that the core saturation in the measurements develops in a similar fashion to the explanation. Therefore, we can conclude that the core saturation can be described with the suggested modeling on which we will simulate our circuit. Please note that the settings of the level of the core saturation for four cases are not exactly the same as Fig. 9.

III. Core Design Process

In order to facilitate the maximum power extraction from the VAMPIRE core, there are several variables we should consider in the core design stage, including variables from the power electronic circuits that are connected to the core. These variables are for manipulating flux parameters, which affect the level of the core saturation. One important thing to note is that, though we used a resistive load in the previous section, a supercapacitor and a rectifier are used in the real system to deal with surge currents, such as initialization and RF transmission bursts.

A. Design Variables

1) Core Compensating Capacitance:

Even with a rectifier and a capacitive load, we can still consider Fig. 4 for a piece-wise time segment where we assume the rectifier is turned on and providing zero impedance. For that time segment, no matter what the load impedance is, we can calculate the equivalent source impedance using a Thévenin equivalent circuit. Since the main impedance is provided by the magnetizing inductance and the wire resistance, the equivalent series source impedance would be inductive, though it is dynamically changing over time. Even so, we can still insert capacitance to (at least partially) cancel the inductive impedance of the core, so as to deliver the most power in a non-saturated region. (In a saturated region, regardless of canceling, delivered power due to the core is zero.) In order to get the best capacitance, we need to solve the differential equation. However, we can estimate the value explicitly if we take the instantaneous complex power of the load, integrate it over a half cycle, and find the extrema. This is a straightforward process, and we get

$$C = \frac{1}{(2\pi f)^2} \cdot \frac{1}{\frac{1}{T}\int_{-0.5T}^{+0.5T} \frac{\mathrm{d}\mathit{Flux}}{\mathrm{d}i_\mu}\mathrm{d}t} \tag{9}$$

If we examine the integral term in (9), we can see that it is equivalent to the average of the instantaneous effective inductance over a cycle. (Even in a constant L_μ case, this gives the correct estimation for the best canceling.) Using this estimation as a first guess, we swept the capacitance and found the best result by solving the differential equation of the real system. Please note that the optimal C estimated depends on flux parameters, such as target output voltage, primary current amplitude, and the number of turns in a transformer. Therefore, C must be adjusted when the configuration changes.

2) The Number of Turns:

If N is getting smaller, the injected secondary side current is getting larger, since it is proportional to $I_{PRIMARY}/N$. However, the magnetizing inductance is getting smaller much faster since it is proportional to N^2, so the power delivery is getting worse. On the other hand, if N is getting larger, we get more of the secondary side current going toward the load branch, but we have less secondary side current to begin with. So, in the extreme, there are two zeros at $N = 0$ and $N = \infty$. Therefore, there has to be a peak value in between, and we can conclude that more N does not always guarantee higher power delivery. Furthermore, there is a saturation effect. Since N is a flux parameter, C from the previous section should be adjusted accordingly. Higher N, which means less secondary side current, is less prone to the core saturation, and this gives higher average inductance. Therefore, in this case, the matching capacitance should go down. Similarly, lower N means larger matching capacitance.

3) Output Load Voltage Level:

As calculated in the feasibility section, the intention of VAMPIRE is delivering the output voltage directly from the core, using a capacitor as a buffer. This means we are not going to use another power converter between the core and the load. Therefore, the load voltage should be higher than the absolute minimum digital supply voltage of 1.8 V. We could have had

sufficient headroom, making the output voltage far higher than 1.8 V to allow much safer monitoring operations. We could have also said that we could pick a certain (higher) output voltage that gives us the maximum power extraction. All these can be true, but we should note that the maximum power extraction point is not necessarily the sufficient current point for the digital load. Even if it is indeed the maximum power extraction, due to the high voltage, the average current that the core supplies can be far less than the average load current. Furthermore, since the power dissipation of the digital circuits tends to decrease with lower supply voltage, we can make the power constraint more loose as we set the output voltage lower. Therefore, in order to make VAMPIRE work, it will be good for us to be around the maximum power extraction point, but only if the minimum steady-state load current is satisfied.

The output voltage will be held constant by the supercapacitor, and this periodically forces a square voltage wave across the core through the rectifier (because this is a current transformer, not a voltage one). Since the flux is the voltage integrated over time, the output voltage is definitely a flux parameter. Therefore, we need to adjust the matching capacitance in accordance with the target output voltage as well.

B. The Effect of Higher Primary Current

Though this is not a core design variable, this is the main flux parameter for the core. Therefore, we need to recalculate the matching capacitance if VAMPIRE harvests energy from different instruments. If we increase the primary side current, the secondary side current will automatically increase, and more power will be delivered to the load. However, we can expect that after a certain point the core will be almost entirely saturated, and it will not allow the core to transfer more power than a normal air-core transformer would. In order to avoid this hard limit, we can make the core physically larger, or find a core with higher B_{SAT} and similar μ_r. Currently such a material is not commercially available.

In the hard saturation regime, one could argue for lower μ_r. However, a quick analysis shows that this will not improve the amount of energy harvested. The area under a B-H curve is the magnetic energy density in the core, and the slope of the curve is the magnetic permeability. As the current increases, a range of H field is getting wider, and the magnetic energy density increases. However, the increased area does not mean an increase in the energy harvested by the core. Assume H is linearly increasing with time, which is a good approximation when the amplitude of the current is large and the core is in hard saturation. Then, the B-H curve can be seen as 'B vs. time' as well. We can see multiple meanings at the same time in the B-H curve. Since the harvested power is proportional to $\partial B/\partial t$, the harvested energy, which is stored in the supercapacitor, is proportional to B, which has an asymptote of B_{SAT} in the B-H curve. Now, assume that μ_r is halved, but B_{SAT} stays the same. We have twice the time to reach the saturation, however, energy harvested in the nonsaturation region is still the same since the slope is halved.

Meanwhile, the higher μ_r has saved a little bit more of power

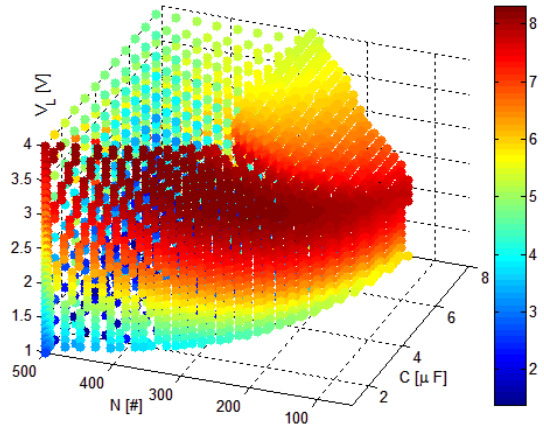


Fig. 11. Illustration of a 3-D Variable Space - Color: Power [mW] (Z-axis: Load Voltage [V], Y-axis: N [#], X-axis: C [μF])

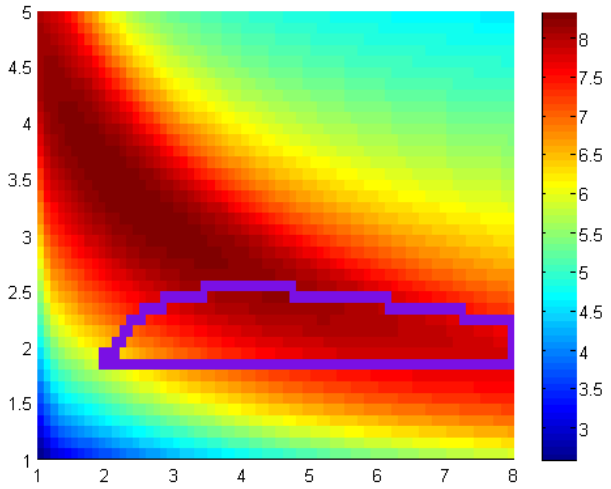


Fig. 12. Maximally Extractable Power from the Core with Proper N (Color: Power [mW], Y-axis: Load Voltage [V], X-axis: C [μF]) (Purple Loop: Power Constraint of the Monitoring Package)

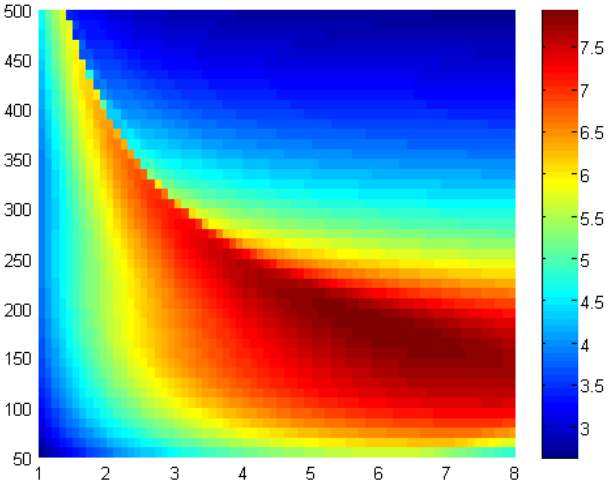


Fig. 13. Maximally Extractable Power from the Core at $V_L = 2\,\mathrm{V}$ (Color: Power [mW], Y-axis: N [#], X-axis: C [μF])

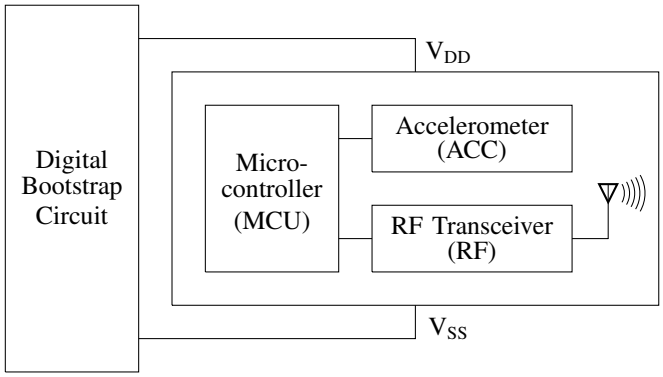
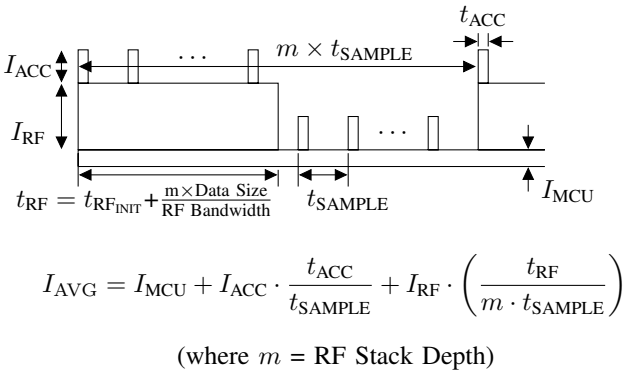


Fig. 14. Digital Block Architecture



$$I_{AVG} = I_{MCU} + I_{ACC} \cdot \frac{t_{ACC}}{t_{SAMPLE}} + I_{RF} \cdot \left(\frac{t_{RF}}{m \cdot t_{SAMPLE}} \right)$$

(where m = RF Stack Depth)

Fig. 15. Digital Current Profile
(The magnitude of the currents are not proportional to the scale above)

in the saturated region, though it may be tiny. Therefore, unless we find a different core with higher B_{SAT}, lower μ_r always harvests less energy.

C. Final Core Design Values

Given the fixed primary current, there are three control variables: matching capacitance, a number of turns, and target load voltage. Since a 4-D plot (3 variables with 1 result), as illustrated in Fig. 11 as a notional example, is hard to explore, we have drawn two surface cuts of such a 3-D variable space fixing one variable at a certain value. In Fig. 12, N is selected (but omitted in the figure) for each C and V combination such that the power is maximized at the given C and V pair. The purple loop inside the plot means the constraints of the digital circuits, such as minimum supply voltage and average current of the monitoring package. We decided to choose 2 V as the target output voltage for the core, and this is used to plot Fig. 13, which is N vs. C. The final values we have chosen are, $N = 230$, $C = 5.6\mu$F, and $V_L = 2$ V, targeting 7.5 mW. If the primary current or the target output voltage is subject to change during the operation, a compensator, which is a multiplexer controlled by a microcontroller, can be designed to select the most power beneficial N and C combination. We can provide multiple values of N by using a multi-tapped core. By shorting across different taps the effective number of turns can be adjusted at runtime.

IV. Circuit Topology

A. Monitoring Package

The digital block architecture for VAMPIRE is drawn in Fig. 14, and its current profile, when in operation, is illustrated in Fig. 15. After optimizing associated variables in the current profile, such as RF stack depth, sampling frequency, RF bandwidth, data size, and data resolution, we achieved load power consumption of 6.5 mW at V_{DD} of 2 V with the sampling frequency of 125 Hz. Each sampling contains 3-axis acceleration data with each axis in 10-bit resolution. Although we omitted the explicit temperature sensor in Fig. 14, VAMPIRE samples additional 8-bit temperature information from the temperature sensor every 160 ms. The RF channel

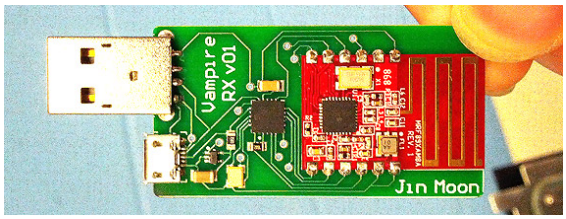


Fig. 16. VAMPIRE Receiver

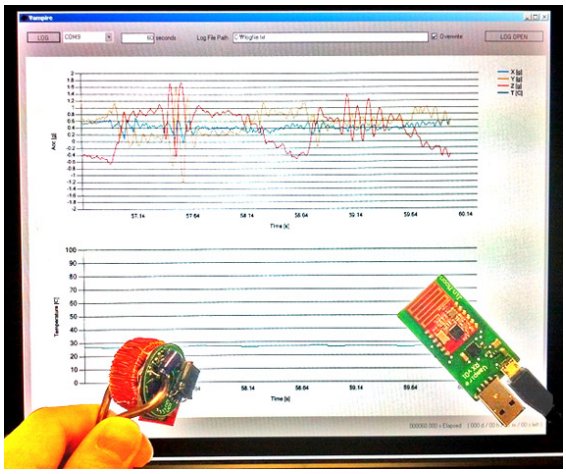


Fig. 17. Real-time Demonstration with a 90 W-60 Hz Desk Lamp

frequency that VAMPIRE uses is 868 MHz, and the receiver module, which uses USB to connect to a PC, is presented in Fig. 16. By assigning a different network address to each device, multiple VAMPIREs can be simultaneously supported using one receiver. Fig. 17 shows the real-time demonstration of VAMPIRE and the software we developed (a 90 W-60 Hz desk lamp is used as a primary side).

B. Overall Arhitecture of VAMPIRE

VAMPIRE's overall block diagram is given in Fig. 18. The first stage is the magnetic core and the matching capacitor. (We have implemented two compensation paths in Fig. 1, though it can be increased to as many as we need.) After the first stage,

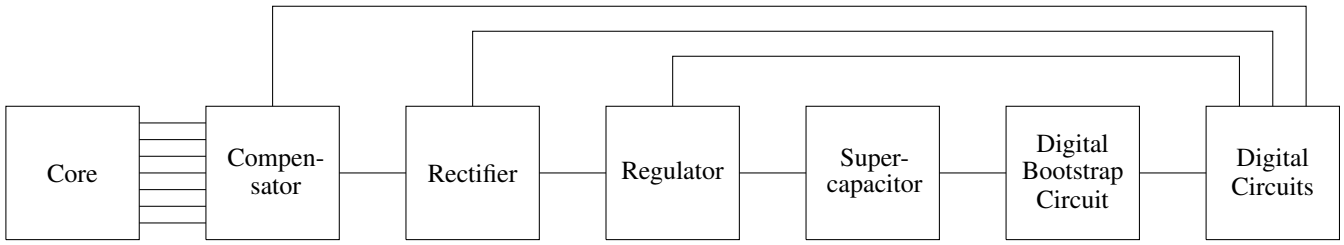


Fig. 18. VAMPIRE Block Diagram

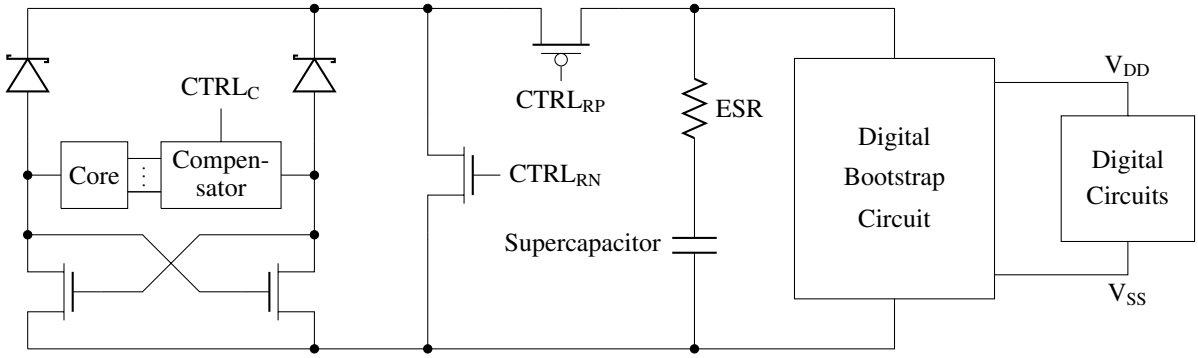


Fig. 19. Power Block Architecture

the current from the core is rectified and stored in a $50\,\mathrm{mF}$ supercapacitor through a voltage regulator, which can provide a short circuit path for the transformer for an appropriate amount of time if the current is larger than what is required for the digital load. This is to prevent the supercapacitor from getting indefinitely charged up. This is especially important since supercapacitors usually have a very low voltage rating. After a certain time, when the supercapacitor has enough voltage, the digital bootstrap circuit is triggered, and provides the power supply paths to the digital load. The digital load becomes operational after that point, and will be so as long as the voltage in the supercapacitor does not go below the minimum voltage we set.

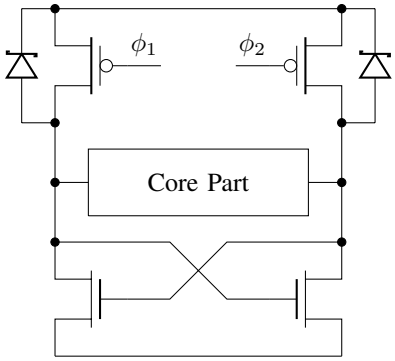


Fig. 20. Rectifier with the Active Gate-control

C. Power Electronic Circuits

1) Rectifier - Passive:

Fig. 19 is the power block architecture used in Fig. 1. Rectification is done by two Schottky diodes in top and two MOSFETs cross-coupled in bottom. This is a passive rectification circuit, which requires no additional control power, but it has one diode voltage drop along the current path when the circuit is operating. The corresponding power loss is $V_{\mathrm{DIODE}} \times I_{\mathrm{AVG}} = 0.15\,\mathrm{V} \times 3.25\,\mathrm{mA} = 0.5\,\mathrm{mW}$. Since the core is a current-driven transformer, one of the two cross-coupled MOSFETs is automatically selected in accordance with the current direction, and corresponding voltage is automatically developed across two terminals of the core part (the core and the compensator). When enough voltage is developed in the supercapacitor, we can actually see that the voltage polarity of the core part, hence the selected MOSFET, is consistent with the voltage forced by the supercapacitor, provided the voltage regulator is connecting the rectifier to the supercapacitor.

2) Rectifier - Active:

We can avoid the diode power loss by adding a MOSFET in parallel with each diode, as given in Fig. 20, and applying the active gate-control, ϕ_1 and ϕ_2, to the newly placed MOSFETs. The basic concept is that when the current path is well switched by diodes, we turn a MOSFET on and reroute most of the current from the diode to the MOSFET, which has substantially lower on-resistance (hence much lower voltage drop across the device). The complications are that the MCU is busier, taking care of additional computations for phase alignment, and more I/O ports are occupied for feedback and control purposes. This is a direct increase in digital power consumption, but the increase is relatively lower than the diode

loss. In the end, we achieved $0.3\,\mathrm{mW}$ better power transfer with 95% MOSFET on-time. The rest (5%) of the cycle is used to charge up and discharge gate capacitances, and this duration can not be zero. (During this time, the diode carries the current, so current direction switchings are automatic.)

One might suggest that we may use cross-coupled MOSFETs for both top and bottom to eliminate the control power. Such a method is described in [6] and [7]. However, the explanations given in [6] and [7] are only applicable to voltage-driven transformers, whereas the core in VAMPIRE is a current-driven transformer. The specific problem is that, without an active gate-control, the current path will not automatically switch even if the current goes negative, because a MOSFET is a bidirectional device. It is turned off when $|\mathrm{V_{GS_P}}|$ becomes lower than the threshold voltage, and this is not a function of the current direction. Any one of the two MOSFETs will try to discharge the output voltage until it reaches the cut off region every cycle. Therefore, in this case, the output voltage of the rectifier will be settled around $|\mathrm{V_{GS_P}}|$.

Although the active gate-control method, Fig. 20, is not implemented in a neat construction like Fig. 1, we built this version separately and measured the improved power transfer by $0.3\,\mathrm{mW}$. Please note that the cross-coupled pair can be either PMOS or NMOS, provided that the gate-control is adjusted accordingly.

3) Voltage Regulator and Supercapacitor:

In Fig. 19, two MOSFETs after the rectification stage are for the voltage regulation. In a normal operation, the PMOS is turned on, providing a current path to the later stages. However, if the average core current is higher than the average load current, $\mathrm{CTRL_{RN}}$ is asserted (and the PMOS is turned off) for an appropriate amount of time in each cycle, and the NMOS is providing a short circuit path for the core. One complication is that, if we use the active gate-control, we monitor the voltage across the core part as a feedback, and it is near zero when the core is short-circuited. In this case, we turn off the active gate-control for easier MCU manipulation despite the power loss due to the diode voltage drop.

4) Digital Bootstrap Circuit:

A hysteresis driven amplifier is used for the digital bootstrap circuit with a voltage level detector to set up a start-up condition for the digital load as well as to limit the lower bound of the digital circuit voltage in case of an insufficient current supply. Also included in this circuit are the initialization paths for control signals when the MCU is not powered on. For example, $\mathrm{CTRL_C}$ = DEFAULT, $\mathrm{CTRL_{RP}} = 0$, and $\mathrm{CTRL_{RN}} = 0$ until the MCU comes alive. Please note that if there are more than 2 compensation paths, $\mathrm{CTRL_C}$ becomes a multi-bit control signal.

5) Power Factor:

Simulated power factor of Fig. 19 is 0.95, and it increases to 0.97 with the active gate-control. Achieving this value is aided by the fact that the matching capacitance is also a power factor corrector, and another important point is that the core is a current-driven transformer. Since one of the two possible paths should be always turned on due to the transformer current, the supercapacitor is directly connected to the core as a constant voltage source, and more importantly, it is connected to the core in a way that it always takes in the currents (because all the current switchings are done by the diodes).

V. Conclusion

The VAMPIRE prototype is successfully built, harvesting $7.5\,\mathrm{mW}$ from a $90\,\mathrm{W}$-$60\,\mathrm{Hz}$ desk lamp. The core volume is $2.9\,\mathrm{cm}^3$, and the small dimensions of VAMPIRE open up the possibility of being enclosed in or retrofit into a wide range of equipment to be monitored. Despite the magnetic core saturation, which restricts power transfer to the monitoring package, a careful analysis and design process led to a successful VAMPIRE energy harvester. A sufficient amount of power is harvested to sample the 3-axis vibration data at $125\,\mathrm{Hz}$ and periodically enable wireless burst transmissions through an RF channel. With this self-powered standalone sensor node, we can monitor equipment of interest without any special power wiring or external battery. In addition, since there is no downtime in VAMPIRE, it is capable of providing continuous monitoring information for an indefinite amount of time.

Acknowledgment

The authors would like to thank ONR Structural Acoustics Program, and The Grainger Foundation.

References

[1] J. Donnal, U. Orji, C. Schantz, J. Moon, S. Leeb, "VAMPIRE: Accessing a Life-Blood of Information for Maintenance and Damage Assessment," in *Proc. American Society of Naval Engineers*, Feb. 2012.

[2] S. B. Leeb, S. R. Shaw, and J. L. Kirtley Jr., "Transient Event Detection in Spectral Envelope Estimates For Nonintrusive Load Monitoring," *IEEE Trans. Power Del.*, vol. 10, no. 3, pp. 1200-1210, Jul. 1995.

[3] S. B. Leeb, "A Conjoint Pattern Recognition Approach to Nonintrusive Load Monitoring," Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, Feb. 1993.

[4] S. R. Shaw, "System identi?cation techniques and modeling for nonintrusive load diagnostics," Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, Feb. 2000.

[5] G. Herzer, "Amorphous and Nanocrystalline Soft Magnets," in *Proc. NATO Advanced Study Institute*, vol. 338, pp. 711-730, , Jul. 1996.

[6] A. Facen, A. Boni, "Power supply generation in CMOS passive UHF RFID tags," *Proc. 2nd Conf. Ph.D. Research Microelectronics and Electronics*, pp. 33-36, Jun. 2006.

[7] J. Wardlaw, A. Karsilayan, "Self-Powered Rectifier for Energy Harvesting Applications," *IEEE J. Emerging and Selected Topics in Circuits and Systems*, vol. 1, pp. 308-320, Sept. 2011.