Power Flow Control and Regulation Circuits for Magnetic Energy Harvesters

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***Abstract*—This paper presents control schemes for power flow and voltage regulation for magnetic energy harvesters, using unique operating properties set by a current-driven harvester core. An active rectification circuit and a voltage regulation circuit are introduced based on assumptions of a supercapacitor and a MHz microcontroller that is already accompanied in the sensor node. Detailed analyses on circuits, control methods, and state transitions are provided from an implementational viewpoint. In the experiment, fine regulation of 48 mV is achieved at the nominal voltage of 4.5 V with increased power dissipation in μW range, and the active rectification method boosts power harvest by more than 10% compared to a conventional full-bridge diode rectifier. An overall architecture of the power processing circuits are first introduced, and circuit and control analyses are proposed. Simulation and experimental verification subsequently follow to demonstrate effectiveness of the proposed circuits and control methods.**

I. Introduction

An energy harvester provides great flexibility to sensors and monitoring applications, allowing them to operate from parasitic or symbiotic energy flows without custom power wiring or inconvenient battery installation. There are many symbiotic energy sources, e.g., mechanical vibration [2], [3], [7], thermal gradients [4], [5], acoustic vibrations [6], and light [8], etc., and magnetic field also can be an energy source by utilizing a magnetic core to harvest the energy. A magnetically self-powered sensor node called VAMPIRE (Vibration Assessment Monitoring Point with Integrated Recovery of Energy), based on a magnetic energy harvester, has been built and verified operational in [1]. Once the energy harvester is capable of sustaining the load, the sensors and monitoring devices are powered on, assessing operating signatures, such as vibration, thermal profile, etc. The sensor node can indicate diagnostic conditions, or affirm proper operations by trasmitting appropriate information through wireless channels. Though it is beyond the scope of this paper, magnetic energy harvesters have additional benefit of allowing the associated sensors to measure the electrical consumption of the operating electromechanical equipment.

The notional illustration of VAMPIRE is drawn in Fig. 1. A single winding of the primary side goes through the center of the magnetic core of the harvester, and induce the secondary side current. This is similar to a configuration of a conventional current transformer, but is different in that the energy is actively harvested by subjecting the generated current to an internally built-up and regulated voltage. More differently, since the magnetic core is continuously stressed by a constant

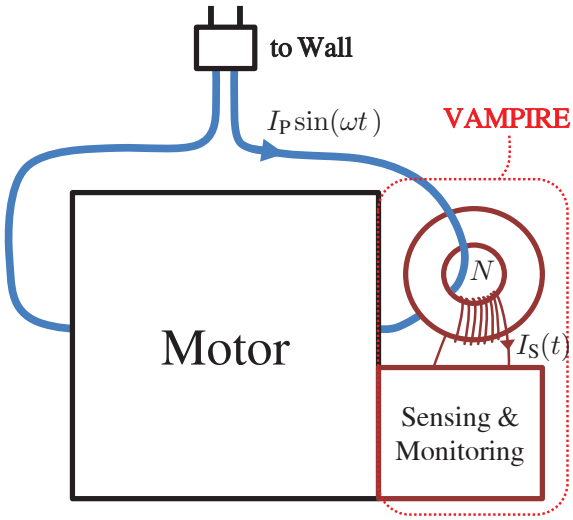

Fig. 1. Illustration of VAMPIRE

voltage, the core is periodically saturated, whereas conventional magnetic cores always avoid such magnetic nonlinearity.

A current-driven transformer is more appropriate for harvesting purposes than a voltage transformer, because it imposes negligible insertion impedance on the primary side. Also, since the current, instead of the voltage, is forced on the harvester side, a rectifier does not see any dead time during polarity switchings of the current, which results in longer harvesting opportunities. Also, a magnetic energy harvester can supply power in mW order very reliably with relatively small dimensions from a low primary side current, for example, 7.5 mW with 2.9 cm^3 from sub-1 A_{RMS} [1]. However, there are still issues to be addressed. The harvester must be self-powered, therefore, it must have passive ways of harvesting energy starting from the zero energy state. Also, initializations of the devices that are not used until active controls are enabled, proper transitions from the passive control to the active control, and actual generation of control signals in a power efficient way are required. Moreover, the voltage of a supercapacitor, which acts as an energy storage, always increases since the core serves as a current transformer. Therefore, a proper regulation must be designed in the harvester as well.

In this paper, such issues are addressed and solutions are proposed. Detailed analyses on power flow, active rectification and voltage regulation circuits, and control methods are pre-

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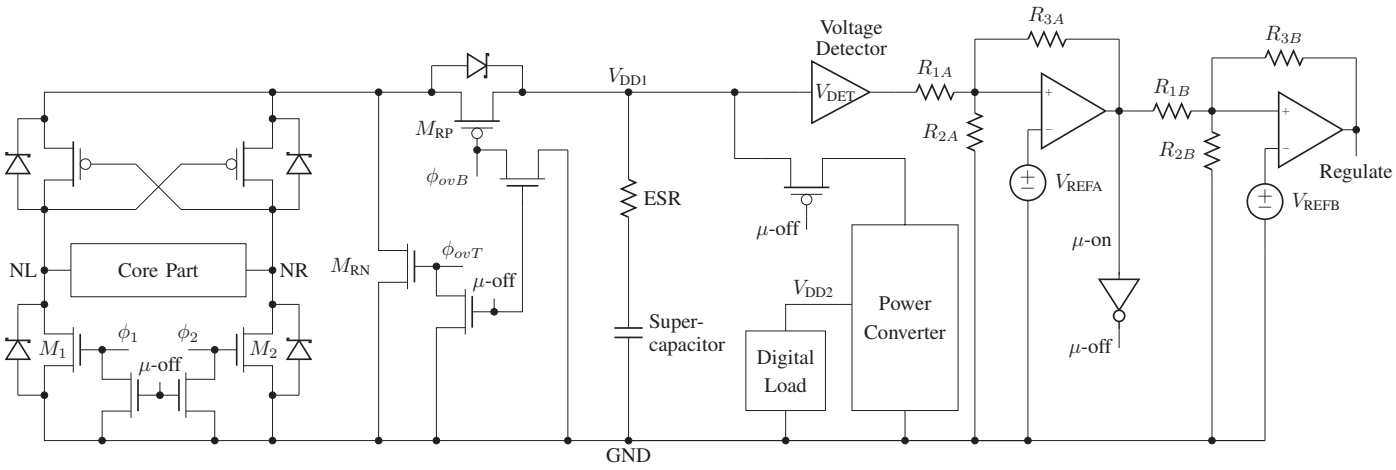


Fig. 2. Overall Power Processing Circuits

sented. Circuit simulation and experiment results are presented as verification. Throughout the paper, a sustainable operation is assumed: the average power harvested from the core is always equal to or greater than the average power dissipation of the load.

II. Power Processing Circuits

A. Overall Architecture

The overall architecture of the power processing circuit given in Fig. 2 includes a rectifier, regulation switches, a supercapacitor, hysteresis amplifiers, and a digital load, including a microcontroller. The rectifier is implemented with active gate control, requiring two gate signals from the microcontroller. Regulation switches are placed between the rectifier and the supercapacitor, requiring another two gate signals from the microcontroller. The supercapacitor serves as an energy storage, and its voltage is regulated by hysteresis amplifiers, regulation switches, and the microcontroller. The digital load is treated as a constant current load, and is not described in this paper, except for the microcontroller for control purposes. Since the magnetic energy harvester has no external power source, the boot-up process from the zero energy state requires the entire circuit to rely on passive components only. Once the energy stored in the supercapacitor is sufficient, i.e., the voltage across the supercapacitor reaches a predefined level, the microcontroller is powered on, and starts controlling all the actively controlled devices. The voltage level of the supercapacitor is determined based on core saturation and initial power surge of the digital load. Until then, all the actively controlled switching devices must be initially turned off or bypassed explicitly because microcontroller's outputs are in high-impedance states. In order to handle initializations, additional FETs with direct gate controls from one of the hysteresis amplifiers, not from the microcontroller, are employed in the design.

B. Rectifier

A full-bridge diode rectifier is an effortless way to implement AC-DC rectification. However, it always imposes two diode voltage drops in current paths, causing power loss. One of the effective methods to reduce this loss is to use Schottky diodes that have low threshold voltage, though it does not completely remove the loss. A better way is described in [1]. One diode pair, either top or bottom, can be replaced with cross-coupled FETs. The top pair can be substituted by PFETs, and the bottom pair can be substituted by NFETs. The cross-coupled FETs completely eliminate one diode loss without any side effect and control effort because the magnetic core of the harvester is a current-driven transformer. However, the remaining diode pair cannot be replaced with cross-coupled FETs due to the backward conduction [1]. Instead, actively controlled FETs can be used. While doing so, Schottky diodes can be left in parallel with the FETs, or eliminated with the intention of using the body diodes of the FETs. In the latter, the circuit implementation becomes simpler in the expense of power efficiency.

As suggested in [1], diodes are used during zero crossings of the harvester current, and the FETs are used for the remaining portion of the cycle, where the current path is clearly determined. The active switches drastically reduce the voltage across them due to low on-resistance, and power loss is greatly reduced. For example, the diode pair, either Schottky or body, is used for 16% of the rectification time to deal with automatic switchings of current paths, and the actively controlled FET pair is used for the remaining 84%. It can be especially beneficial when the primary side —electromechanical equipment— carries very high current. Moreover, the rectifier with active gate control has an additional benefit. It not only reduces power loss due to diode voltage drop, but helps the core maintain an unsaturated state a while longer due to lower voltage stress across the core, leading to a lengthened harvesting time window.

In this paper, the top diode pair is replaced with cross-coupled PFETs, and gate controlled NFETs are placed in the bottom, in parallel with Schottky diodes. The logic behind the decision on the cross-coupled PFETs instead of the cross-coupled NFETs is that the microcontroller in this paper is operating at a lower voltage than the voltage of the supercapacitor, and all the circuits share the same ground. In this case, logic-1 signals from the microcontroller may not be sufficiently high to guarantee cut-off regions for PFETs. For example, in the experiments, the regulated voltage of the supercapacitor (V_{DD1})

TABLE I. DESIGN VALUES AND CONSTRAINTS

B_{SAT}	$1.19\,\mathrm{T}$
A_{CORE}	$3.6 \times 10^{-5}\mathrm{m}^3$
N	200
ω	$2\pi \cdot 60\,\mathrm{Hz}$
C_{S}	$0.5\,\mathrm{F}$ with ESR of $140\,\mathrm{m}\Omega$
I_{P}	$0\,\mathrm{A}$ - $28.28\,\mathrm{A}$ [$0\,\mathrm{A_{RMS}}$ - $20\,\mathrm{A_{RMS}}$]
Target V_{DD1}	$4.5\,\mathrm{V}$
Target V_{DD2}	$1.8\,\mathrm{V}$
I_{LOAD}	$0\,\mathrm{mA}$ - $27\,\mathrm{mA}$ [DC]

is $4.5\,\mathrm{V}$, the supply voltage of the microcontroller (V_{DD2}) is $1.8\,\mathrm{V}$, and the threshold voltage of PFETs is $1.2\,\mathrm{V}$. In this case, the P-side control is not feasible without level shifters. On the contrary, the N-side control is guaranteed without level shifters, assuming the same $1.2\,\mathrm{V}$ threshold voltages for NFETs, because the voltage level of a logic-1 signal from the microcontroller ($1.8\,\mathrm{V}$) is greater than the threshold voltage of the NFETs ($1.2\,\mathrm{V}$). With the intention of including power conversion circuits for various loads with different operating voltages, the N-side control is chosen for simplicity. Detailed explanations on how to generate an initialization control and two gate controls are discussed in the later section.

C. Regulator

The current in the primary side is assumed sinusoidal. Since the magnetic core acts as a current-driven transformer, the core and the rectifier can be substituted by a positive periodic current source. However, there is a complication in the analysis that the core can periodically go into magnetic saturation during the harvesting operation, in which case no current can come out of the magnetic core [1]. In order to incorporate this observation, the description of this behavioral current source —the core and the rectifier— must be updated: it generates a positive periodic current, which is $|I_{\mathrm{P}} \sin(\omega\, t)/N|$, until the core saturation, and then zero current after the saturation. Assuming a sustainable operation of the sensor node with the harvester, the supercapacitor is forced to take-in a net positive current from this current source, which continuously increases the voltage across the supercapacitor. In order to protect the supercapacitor from being indefinitely charged up and maintain an optimized state for the energy harvesting, the voltage of the supercapacitor must be regulated.

The circuit operation of the core, the rectifier, and the supercapacitor altogether is identical to that of a boost converter with zero duty cycle. Therefore, a quick analogy from a boost converter can be used to achieve the voltage regulation: a switch. This switch is to connect and disconnect the supercapacitor to and from the current source, controlling the inward current that the supercapacitor receives. However, a second switch that shorts out the current source when necessary is required to ensure a safe operation because the current source needs a current path at all times. Otherwise, without the second switch, the magnetic core inside the behavioral current source becomes suddenly electrically floating, and generates very high voltage spikes across its two terminals. Ofttimes, diodes and FETs inside the rectifier cannot withstand such large voltage stress. The regulation strategies are simple: first, connect the supercapacitor to the current source if the voltage of the supercapacitor is lower than a certain lower threshold; second, disconnect the supercapacitor from the current source if the voltage is higher than a certain upper threshold. The core is shorted out during this phase using the second switch. The lower threshold and the upper threshold form the regulation band.

The regulation analysis on the first strategy begins with estimating a voltage fluctuation in the supercapacitor per one half cycle when the current source continuously transfers net plus charges into it:

$$\begin{aligned}\Delta V = \frac{\Delta Q}{C_{\mathrm{S}}} &= \frac{1}{C_{\mathrm{S}}}\left[\int_0^{t_{\mathrm{SAT}}} \frac{I_{\mathrm{P}}}{N}\sin(\omega\, t)\ \mathrm{d}t - \frac{T}{2}\cdot I_{\mathrm{LOAD}}\right] \\ &= \frac{I_{\mathrm{P}}}{\omega\, N\, C_{\mathrm{S}}}\left[1-\cos(\omega\, t_{\mathrm{SAT}})\right] - \frac{T\, I_{\mathrm{LOAD}}}{2\, C_{\mathrm{S}}}\end{aligned} \tag{1}$$

In the equation above, I_{P}, ω, T, N, I_{LOAD}, and C_{S} denote maximum amplitude of the primary side current, angular frequency of the primary sinusoid, a period of the primary sinusoid, a number of windings on the harvester side, a load dissipation current, and capacitance of the supercapacitor, respectively. Lastly, t_{SAT} denotes the time point where magnetic saturation occurs with respect to the most recent zero crossing of the primary side current. By setting up and solving the flux equality, t_{SAT} can be also estimated in terms of magnetic properties of the core and the circuit parameters.

$$t_{\mathrm{SAT}} = \min\left[\frac{B_{\mathrm{SAT}}\, A_{\mathrm{CORE}}\, N}{V_{\mathrm{DD1\text{-}target}}},\ \frac{T}{2}\right] \tag{2}$$

Here, B_{SAT} and A_{CORE} denote the saturation flux density and the flux area, respectively. The $\min$ function is used to bound t_{SAT} in case of nonsaturation throughout the entire half cycle. (The term "cycle" appearing throughout this paper indicates the period of the primary sinusoid. Since the fundamental frequency of the rectified current is twice the primary side frequency, half cycles are used in the analyses and equations of this paper.)

Since t_{SAT} is independent of I_{P} and I_{LOAD}, the worst fluctuation —the worst "increase" in this case— happens when there is no load current, and the supercapacitor takes in the maximum current from the current source. With the design values and constraints given in Table I, the worst case voltage increase is $0.185\,\mathrm{mV}$ per one half cycle. Targeting $45\,\mathrm{mV}$ for the regulation band, which is 1% of the nominal voltage, the worst case increase corresponds to generation of a "disconnect" control signal after 121 cycles with respect to the most recent time point where the voltage of the supercapacitor was at the lowest value of the regulation band. Since the cycle frequency is $60\,\mathrm{Hz}$, this translates to approximately $2\,\mathrm{s}$.

The regulation analysis on the second strategy for the other worst fluctuation —the worst decrease— also starts with (1). However, in this case, the worst decrease happens when the supercapacitor is disconnected from the current source ($I_{\mathrm{P}} = 0$), and I_{LOAD} is at maximum. In this extreme, the worst case voltage decrease is $-0.45\,\mathrm{mV}$ per one half cycle. It corresponds to generation of a "connect" control signal after 50 cycles, which translates to $833\,\mathrm{ms}$, with respect to the most recent time point when the voltage of the supercapacitor was at the highest value of the regulation band.

However, an effective series resistance (ESR) of the supercapacitor must be accounted as well, because whenever there

TABLE II. REGULATOR DESIGN TARGET

	1st Amplifier	2nd Amplifier
V_{REF}	2.4 V	2.4 V
R_1	1.5 MΩ	470 kΩ
R_2	2 MΩ	536 kΩ
R_3	12 MΩ	50 MΩ
V_{ON}	4.5 V	4.527 V
V_{OFF}	4.0 V	4.485 V
Target ΔV	0.5 V	42 mV
Max. Operating Current	7.38 µA	10.36 µA

is a current the ESR develops an additional voltage fluctuation across it. It adds a positive amount to the voltage fluctuation when the supercapacitor is connected to the current source, and negate amount when the supercapacitor is disconnected from the current source. Therefore, if the same signal intermittencies, 2 s and 833 ms, are desired, the target voltage regulation band cannot be met. However, since this control signal is extremely slow in electrical circuit's standpoint, the signal intermittencies can be adjusted to contain the voltage spikes due to the ESR within the target regulation band. Denoting the minimum signal intermittency as $t_{\text{MIN-}\phi_{ov}}$, the target regulation band, including the effects of charge transfer and the ESR, can be expressed as:

$$\text{Regulation Band} = \left(\frac{I_{\text{P-MAX}}}{N} + I_{\text{LOAD-MAX}}\right) \cdot R_{\text{ESR}} + \frac{I_{\text{LOAD-MAX}}}{C_{\text{S}}} \cdot t_{\text{MIN-}\phi_{ov}} \tag{3}$$

Here, $I_{\text{P-MAX}}$ is the maximum primary side current, $I_{\text{LOAD-MAX}}$ is the maximum load current, and R_{ESR} is the effective series resistance of the supercapacitor. The first term in the equation represents two voltage spikes caused by the ESR, one in the positive side, and the other one in the negative side. The second term represents the voltage fluctuation due to charge transfer. The regulation band estimated from this equation is actually an overestimation to be a conservative design guideline, because in reality the core may saturate, and the current from the current source does not reach $I_{\text{P-MAX}}/N$ in that case — a more optimistic expression for the positive ESR spike is $I_{\text{P-MAX}} \sin(\omega\, t_{\text{SAT}})/N \cdot R_{\text{ESR}}$.

Using the values from Table I, and R_{ESR} of 140 mΩ, the regulation band of 45 mV can be achieved with the signal intermittency $t_{\text{MIN-}\phi_{ov}}$ of 396.7 ms. Though it is smaller than the original intermittencies, it is still extremely slow in a circuit operation standpoint. Generation of this control signal is trivial with virtually any circuit, including, for example, a widely available MHz microcontroller with an analog ADC, or even a voltage detector with hysteresis amplifiers and handful of digital gates (or a microcontroller without ADCs). In any method, the fine regulation of 45 mV can be achived without any additional inductor, hence the regulator does not exhibit any output ripple by its nature, which contrasts usual inductor-based power converters, where the additional filter stage must be inserted to mitigate an output ripple.

The design of this paper employs a voltage detector, two hysteresis amplifiers, and an existing microcontroller in the monitoring package of the sensor node, without an analog ADC function. After the voltage of the supercapacitor V_{DD1} reaches a minimum voltage VDET, referring to Fig. 2, the first hysteresis amplifier is turned on, eventually turning on the microcontroller for the first time. The reason to employ the voltage detector is to avoid uncertain states of the comparator while V_{DD1} is below the minimum operating voltage during the V_{DD1} ramp-up. The voltage detector used in the design is Microchip's TC54VC2702 with 2.7 V threshold. The subsequent hysteresis amplifiers then set two different voltage regulation bands, which in general can be expressed as:

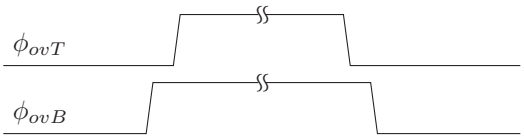


Fig. 3. Desired pulse waveforms of ϕ_{ovT} and ϕ_{ovB}

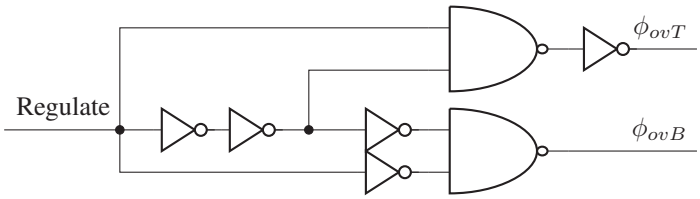


Fig. 4. Generation of ϕ_{ovT} and ϕ_{ovB} without a microcontroller

$$V_{\text{ON}} = V_{\text{REF}} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \cdot R_1$$
$$V_{\text{OFF}} = V_{\text{REF}} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \cdot (R_1 /\!/ R_3) \tag{4}$$

The first hysteresis amplifier sets a slightly wider operating voltage range than the finer regulation band to survive the initial turn-on transient where the initial surge current of the digital load combined with the ESR and parasitic inductances generates a huge voltage spike. Power of the first hysteresis amplifier is supplied by the output of the voltage detector, and power of the second hysteresis amplifier is supplied by the output of the first hysteresis amplifier. Therefore, once the first amplifier asserts "μ-on", the second hysteresis amplifier is powered up, and generates a fine voltage regulation signal, "Regulate", which can be processed with logic gates, or fed to the microcontroller for more signal processing. Table II presents the component values and resulting regulation ranges for the two amplifiers. The fine regulation band is slightly adjusted to 42 mV, because of available resistance values in components. The comparators used in the design are Microchip's MCP65R41T with internal voltage references of 2.4 V. A 56 nF capacitor is placed in parallel with an R_2 resistor in each stage to prevent sudden voltage coupling from changing the hysteresis state.

An extra dissipation current from the voltage detector and two hysteresis amplifiers is extremely low, in the order of µA, as calculated in Table II. ("Max. Operating Current" in the table includes a half of current drawn from the voltage detector, current drawn from resistors, and current drawn from a comparator in each stage.) The increased amount of current in the microcontroller is almost negligible, since an analog ADC function is not required, as will be explained

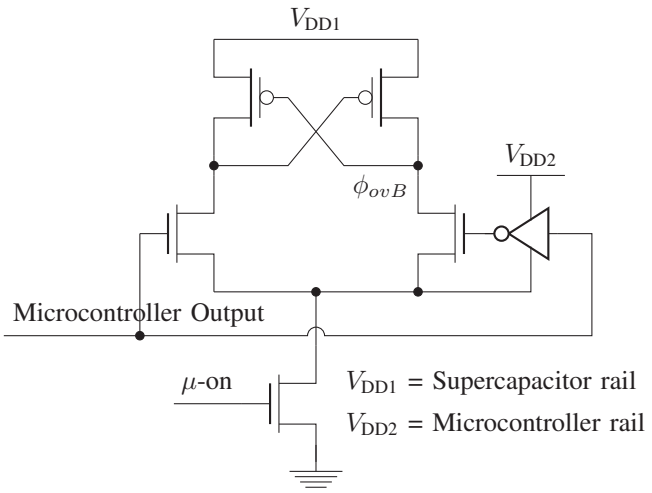


Fig. 5. Generation of ϕ_{ovB} through a level shifter with a microcontroller

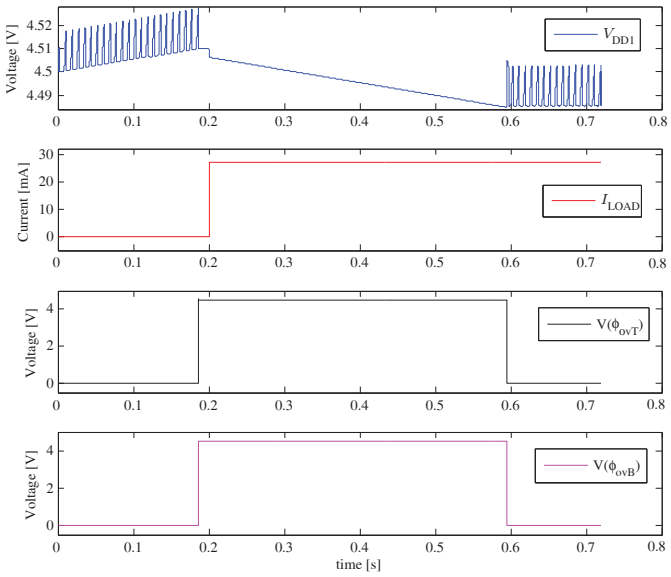


Fig. 6. Simulation of fine regulation

in the subsequent section, and the extra operations due to the regulation are fairly low frequency jobs, compared to the sensor package jobs. Therefore, the entire regulation stage is very power efficient.

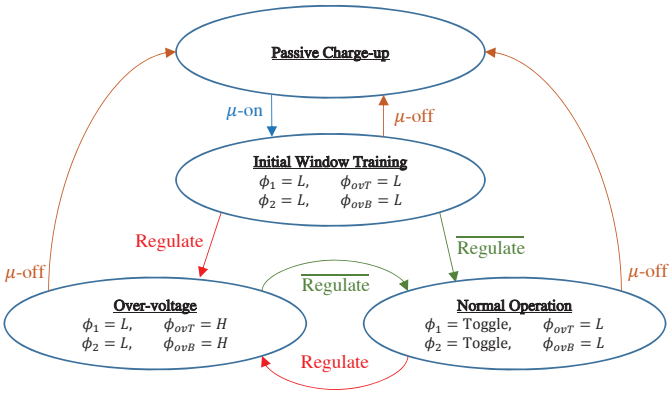
To control the two regulation switches, M_{RN} and M_{RP} in Fig. 2, two control signals are required: ϕ_{ovT} and ϕ_{ovB}. A diode can be used instead of M_{RP} for easier control implementation, in which case "Regulate" can be directly connected to M_{RN} as ϕ_{ovT}. However, identical to the case discussed in the previous subsection, it introduces power loss due to diode voltage drop. Therefore, for a more efficient design, two separate controls are required for the switches. Since any overlap of $\phi_{ovT} = H$ and $\phi_{ovB} = L$ makes a short-circuit path between V_{DD1} and ground, two signals must be generated as suggested in Fig. 3 to avoid undermining the stored energy. This is why "Regulate" cannot be used as a single source for both ϕ_{ovT} and ϕ_{ovB} without further signal processing on it. Even a brief moment during edge transition of the two switches significantly undermines the stored energy in the supercapacitor. In order to have a finite non-overlapping duration between the two control signals, a simple gate level implementation is suggested in Fig. 4. All the logic gates must be operating at V_{DD1} to correctly provide switch controls. On the other hand, if a more sophisticated logic signal is required, for example, digital filtering or combining with other logic functions, the existing microcontroller can be used as in the design of this paper. However, a need for a level shifter for the control of M_{RP} arises in this case, because V_{DD2} is lower than V_{DD1} by more than a threshold voltage of the PFET. In this paper, the microcontroller method is used for the design, and Fig. 5 illustrates the level shifter used in the design. As shown in the figure, the input inverter of the level shifter must be connected to the same low voltage supply that the microcontroller is connected to.

The simulation result of the fine regulation is shown in Fig. 6. In this simulation, Table I and Table II with $I_{P\text{-}MAX} = 20\,A_{RMS}$, $I_{LOAD\text{-}MAX} = 27\,mA$, and $R_{ESR} = 140\,m\Omega$ are used. For the worst case simulation, the load current step from $0\,mA$ to $27\,mA$ is applied at $t = 200\,ms$. The positive peak voltage happens just before the step where the load current is zero with the maximum primary current, and the lowest voltage happens just after disconnecting the supercapacitor from the current source, where the load current is at maximum with zero primary current. The worst case regulation band is still at $42\,mV$ including the effects of the ESR. Very close to the previous calculation, the signal intermittency is measured around $400\,ms$. The rising edge delay from ϕ_{ovB} to ϕ_{ovT} and the falling edge delay from ϕ_{ovT} to ϕ_{ovB} are set to $10\,\mu s$ to avoid the short-circuit path.

III. Control Algorithm

Starting from the zero energy state, the current generated from the magnetic core must be routed by passive components to charge up the supercapacitor until the microcontroller is available. The rectifier has diodes and cross-coupled FETs to initially handle the passive rectification. The regulation stage always receives the rectified current, therefore the diode and its parallel PFET can be always on to carry the initial charging current. Therefore, the only concern for this phase is to make sure all the active switching devices are properly initialized until the microcontroller is operational. This is done by "μ-off" signal from the first hysteresis amplifier stage. The value of μ-off is kept at logic-1 until the capacitor voltage reaches a certain threshold, for example, $4.5\,V$. This signal pulls down ϕ_1, ϕ_2, ϕ_{ovT}, and ϕ_{ovB} to ground, and forces the main NFETs, M_1 and M_2, to be turned off, and the regulation PFET, M_{RP}, to be turned on. Initially, M_{RP} does not conduct, and its parallel diode carries the full charging current. After V_{DD1} is higher than the threshold voltage of a PFET, M_{RP} takes over the charging current from the diode. This initial charging state continues until μ-off goes low, which indicates that the microcontroller is now operational. The initialization FETs are then all disconnected from the gate inputs of M_1, M_2, M_{RN}, and M_{RP}, and the microcontroller takes over the gate controls.

One important aspect of the magnetic energy harvester is that the core is a current transformer. Because the current in the secondary harvester side is forced by the primary side



* ϕ_{ovT} and ϕ_{ovB} must be generated as suggested in Fig. 3.

Fig. 7. State Diagram

current, the rectifier no longer has dead time unlike voltage-based rectifiers. Due to this property, as long as the current in the secondary side exists, one of "NL" and "NR" is connected to V_{DD1} and the other is connected to ground. Therefore, the voltages of the two nodes can be considered as digital when the current in the secondary side exists. If the core never saturates, both NL and NR exhibit full-rail square waves with the 50% duty ratio. Meanwhile, when the core goes into magnetic saturation, zero current is forced by the core. In this case, all the diodes and the cross-coupled FETs inside the rectifier are turned off to enforce zero current, and NL and NR become the same voltage potential, isolated from the outside. The voltage is $0 < v(\text{NL}) = v(\text{NR}) < V_{\text{DD1}}$ to disallow any current during the core saturation.

From the observations above, the status of the core regarding magnetic saturation can be inferred by sampling the digital values of NL and NR. If their values are different, the core current exists, and implies the unsaturated core. If their values are the same, the core supplies zero current, and implies magnetic saturation. This determination is power efficient and can be very fast, because of monitoring voltages using digital input ports (1-bit ADCs) of the microcontroller, instead of monitoring the current using multi-bit ADCs and a hall-effect sensor, which is usually very slow compared to MHz microcontrollers.

Constructing control signals for the rectifier can be easily illustrated with an example. The case where NL $= H$ and NR $= L$ will be assumed in this section for the analysis. This corresponds to $\phi_1 = L$ and $\phi_2 = H$ to support the correct current direction. The microcontroller can easily read in the digital values of NL and NR, and output the digital values within less than a few μs. Even logical inverters can generate such outcomes. There are three complications to this simple problem. The first complications is that, as previously mentioned, switchings of current directions are dealt with diodes in the rectifier to easily eliminate the backward conduction. For this diode operation, a certain amount of time must pass before asserting ϕ_2. Similarly, ϕ_2 must be deasserted a certain amount of time before the actual diode operation happens. Since a prediction is involved in generation of ϕ_2, the microcontroller is used to create a state machine. To create a pulse with the correct width, the percentages of a diode

```
While(μ-on && Regulate) {
 if(rising edge found at t_EDGE) {
  if(the very first rising edge) {
   t_RISE-PREV = t_EDGE;
   t_RISE-CURR = t_EDGE;
  }
  else {
   t_RISE-CURR = t_EDGE;
   t_HALFCYCLE = t_RISE-CURR - t_RISE-PREV;
   t_RISE-NEXT = t_RISE-CURR + t_HALFCYCLE;
   t_φ-RISE = t_RISE-CURR + 0.08×min(t_SAT, t_HALFCYCLE);
   t_φ-FALL = t_RISE-CURR + 0.92×min(t_SAT, t_HALFCYCLE);

   if(NL > NR) { generate φ2; }
   else { generate φ1; }
   // Generate using timer interrupts
   // Pulse timings at t_φ-RISE & t_φ-FALL

   t_RISE-PREV = t_RISE-CURR;
  }
 }
 if(falling edge found at t_EDGE) {
  t_FALL-CURR = t_EDGE;
  t_SAT = t_FALL-CURR - t_RISE-CURR;
 }
}
```

Fig. 8. Pseudo code of the control flow for the normal operation

operation and a FET operation is required. Additionally, this pulse must be placed at appropriate time points, and actual timing information of the load current is required for this job. Locating the two most-recent zero crossings of the load current can provide such timing information, and zero crossings of the load current can be found by detecting a rising edge of NL or NR. Since the microcontroller is running several orders of magnitude faster than the line frequency, detection of a rising edge of NL or NR by sampling the digital values can be considered as an accurate zero crossing. Once two most-recent zero crossings are obtained, the next zero crossing can be immediately predicted due to its periodicity, and the pulse can be placed at appropriate locations. The second complication is the core saturation. When the core saturates during the operation, the load current only exists during a portion of a half cycle. In this case, it is crucial to drive ϕ_2 low before the actual saturation happens. Otherwise, since the saturated core shorts out NL and NR, where NR is connected to ground through M_2 by $\phi_2 = H$, both cross-coupled PFETs conduct, providing short-circuit paths from V_{DD1} to ground if the M_{RP} is on. It significantly undermines the energy stored in the supercapacitor. In order to avoid this issue, another prediction is required, based on the pulse width, i.e., unsaturated window, learned from the previous half cycle. The remaining task is to deal with the initial prediction where there is no previous half cycle. When the microcontroller is initialized for the first time, the rectifier runs without any active gate controls, only relying on the diodes, in the first few cycles. Since the diodes in the rectifier automatically block the backward power flow from V_{DD1} to the rectifier, the width of the unsaturated window can be safely measured. Once the initial window length is measured, subsequent cycles can generate ϕ_2 with proper

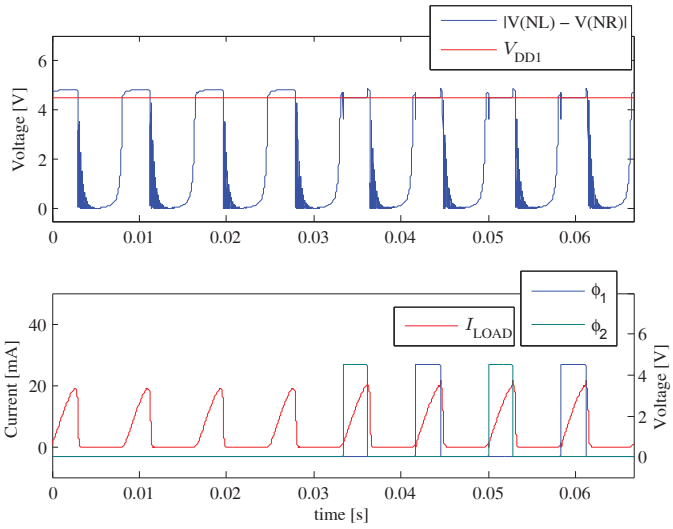


Fig. 9. Active rectification simulation ($I_P = 3.6\,A_{RMS}$, $N = 200$)

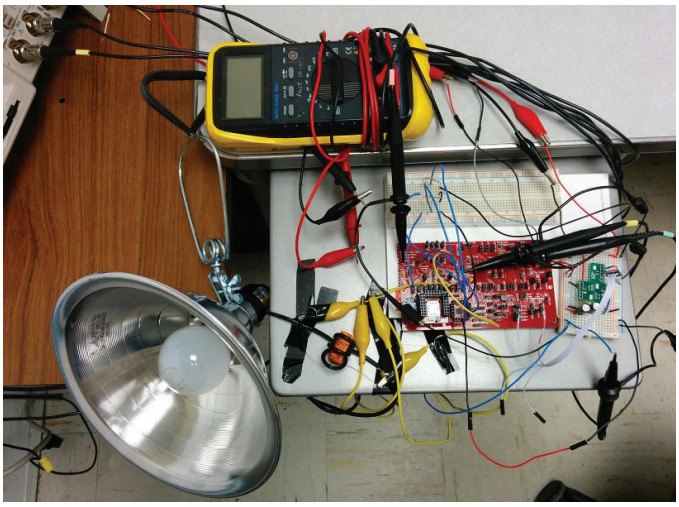


Fig. 10. Test Environments

TABLE III. EXPERIMENTAL RESULTS OF A REGULATOR

Primary Current Range	$0.9\,A_{RMS}$ — $20\,A_{RMS}$
Digital Load Current Range	0 mA — 27 mA
1st Hysteresis Amplifier Band	4.02 V — 4.54 V
2nd Hystersis Amplifier Band	4.503 V — 4.551 V
Regulated Voltage (V_{DD1})	4.524 V
Regulation Fluctuation (ΔV_{MAX})	48 mV
Regulator Circuitry Current Consumption	16.5 µA

margins.

As shown in (2), the window length is approximately constant in the first order, if the voltage of the supercapacitor is fixed and well regulated. If a single voltage target is used for the supercapacitor, a measurement of the initial window length does not have to be continuously tracked and adjusted. However, this does not necessarily mean the window length cannot be measured again. In fact, even after ϕ_2 is driven low, the diode takes over the remaining time duration until the core saturation, and develops NL and NR in the same way. Hence, the window length can be measured every cycle, the control signals can be adjusted accordingly. If the target voltage of the supercapacitor changes throughout the operation, a training must be performed occasionally to track the window length, and in each training, the rectifier must run only with diodes to block backward power flow. Even so, however, an on-the-fly change in V_{DD1}, especially increasing V_{DD1}, is not recommended because the future window length becomes smaller than the current window length, and may discharge the supercapacitor.

The third complication is the over-voltage indication, "Regulate", from the second hysteresis amplifier. When "Regulate" is asserted, the core is shorted out by M_{RN}, and the supercapacitor is disconnected from the core by M_{RP}. In this phase, the simplest implementation is to turn off controls for the rectification. The active rectification can be ignored in this case, because power is not transferred to the supercapacitor. However, since all the nodes in the rectifier is practically grounded during this phase, both NL and NR will read the same digital value. Therefore, this event must be separated from magnetic saturation in the state machine.

Summarizing all the considerations and complications discussed so far, the high-level state transition diagram is depicted in Fig. 7. Among the four states in Fig. 7, detailed pseudo code for the normal operation state is given as an example in Fig. 8. In this example, the window length is tracked every cycle, and the initial training state is also implied in the normal operation.

Figure 9 illustrates the simulated voltage waveforms, where the first four half cycles use a full-bridge diode rectifier, and the remaining four cycles use active rectification. In order to avoid short-circuiting the supercapacitor, the rising edges of ϕ_1 and ϕ_2 are generated slightly after the zero crossings of the load current, and the falling edges of them are generated slightly before the actual saturation happens, as discussed in this section. In the simulation, the same circuit parameters is used except for $I_P = 3.6\,A_{RMS}$. A margin of 8% of the window length is allocated to both the left and the right edges. When the active rectification is applied, the voltage across the core, $|V(\mathrm{NL}) - V(\mathrm{NR})|$, suddenly jumps down and tracks V_{DD1} much more precisely than when it is not. The difference between the core voltage and V_{DD1} in the first four half cycle —during passive rectification— is due to diode voltage drop. The average current generated from the harvester core during passive rectification is 4.1602 mA, whereas the average current during active rectification is 4.6349 mA.

IV. EXPERIMENT

Figure 10 shows test environments with a core of the magnetic energy harvester, test circuit boards, and an electrical load for the experiments. A desk lamp is used as an electrical load in the primary side to generate magnetic field. The primary side is $120\,V_{RMS}$ at 60 Hz. Light bulbs of 108 W and 300 W are used, each carrying $0.9\,A_{RMS}$ and $2.50\,A_{RMS}$, respectively. A number of turns on the primary side is varied from 1 to 8, in order to quickly change effective primary side current without installing another electrical load. In real sensor nodes, only single winding in the primary side is used to minimize invasiveness [1].

In the harvester, a nanocrystalline core, T60006-L2025-

TABLE IV. EXPERIMENTAL RESULTS OF ACTIVE RECTIFICATION

N	200
Primary Current	$3.6\,A_{RMS}$
Regulated Voltage (V_{DD1})	$4.524\,V$
Load Current under Passive Rectification	$4.17\,mA$
Load Current under Active Rectification	$4.65\,mA$

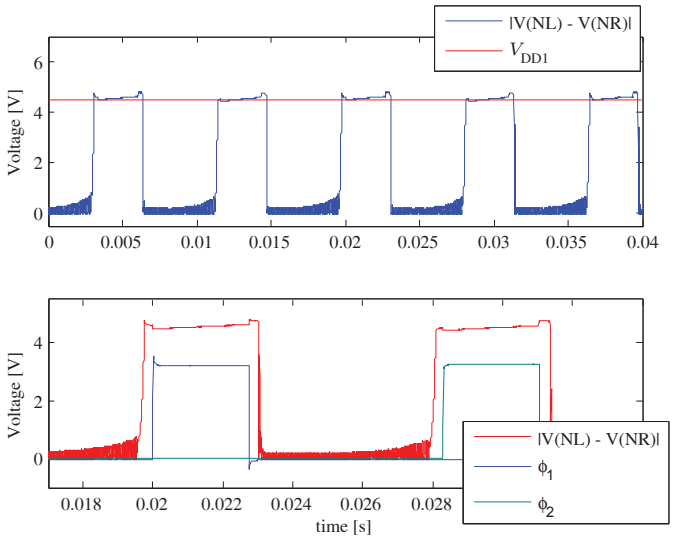


Fig. 11. Experiment result of active rectification

W380 by VAC, is used as a magnetic core, and two identical supercapacitors, PAS0815LS2R5105 by Taiyo Yuden, with $2.5\,V$ voltage rating are connected in series to provide the nominal voltage of $4.5\,V$. Each capacitor has capacitance of $1\,F$ with the ESR of $70\,m\Omega$. The experimental results are summarized in Table III. Fine regulation of $48\,mV$ is achieved in the experiment with I_P up to $20\,A_{RMS}$ and I_{LOAD} up to $27\,mA$. The current dissipation in the voltage detector, two hysteresis amplifiers, and associated resistors is measured in μA range, as expected.

Also, the experimental results for active rectification is described in Table IV. Under the experiment condition listed in the table, the average current with active rectification is increased by more than 10%, compared to the average current with the full-bridge diode rectifier. Also, both current measurements in the experimental results are very close to the simulation results. The experiment waveforms during active rectification are presented in Fig. 11. As discussed in the control section, ϕ_1 and ϕ_2 are generated with margins in both edges. Since active gate control suppresses diode voltage drop, the voltage across the magnetic core in the experiment also jumps down to V_{DD1} during the active control, generating distinct voltage steps around pulse edges of ϕ_1 and ϕ_2, similar to the simulation result.

V. CONCLUSION

This paper discusses power processing circuits and control methods for magnetic energy harvesters. A rectifier with active gate control and its manipulation using a microcontroller are introduced, and a power efficient voltage regulator with fine regulation of tens of mV is proposed and analyzed. Detailed power flow control methods, incorporating the rectifier and the regulator, from passive energy harvesting to the controlled harvesting, are discussed from an implementaional viewpoint with a state diagram and pseudo code. Simulation results and experimental results are presented to validate the design analysis. Higher power harvest with the active rectifier is verified, and fine regulation of $48\,mV$ is achieved at the nominal operating voltage of $4.5\,V$ with increase in the power consumption in μW order.

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