Quad-Switch Push-Pull (QSPP) RF Amplifier with Direct, Simultaneous Modulation of Phase and Pulse Position for Spread-Spectrum Power Applications

Al-Thaddeus Avestruz, Arthur H. Chang, and Steven B. Leeb
Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA 02139
Email: avestruz-at-mit.edu

Abstract—We present a new RF power amplifier for spread spectrum applications, including wireless power transfer with low electromagnetic interference (EMI). The amplifier delivers half sine wave voltage pulses of either polarity through direct push-pull modulation of phase and pulse position. EMI is a concern not only from a regulatory perspective, but also in medical and other critical environments. The voltage pulses can be optimized by a variety of methods for specific spectral characteristics to create a current, and hence a high frequency magnetic field with a spread spectrum. The topology takes advantage of the inherent characteristics of GaN FET devices.

Index Terms—Inverse-class D, current-mode class D, wireless power transfer, spread spectrum, minimum shift keying, direct modulation, EMI.

I. INTRODUCTION

There is a great concern for the reduction of electromagnetic interference (EMI) from high frequency inverters in power electronics applications, especially in wireless power transfer (WPT) [1]–[4], RFID [5]–[10], and electronic ballasts [11]–[15]. The importance is particularly heightened in medical environments with critical or life-sustaining devices [8], [16]–[18]. Not only are these concerns pertinent in medical devices, but also in portable and wearable applications [19], [20]. In wireless power transfer applications, the typical operating frequency is within the ISM bands such as 6.78 MHz or 13.56 MHz [1]–[3], where device optimization along with RF exposure of humans are a concern, it is advantageous to use other frequencies [2], [21]–[23].

There are a wide range of modulation methods to mitigate EMI in these systems by spreading the spectrum. These include frequency modulation [13], [24]–[26], random modulation [27]–[32], and pulse position modulation [33], among others. In [34], the optimization of a spread-spectrum method for wireless power transfer is discussed; this paper presents and discusses the design of an RF amplifier that is particularly suited for this, along with other spread spectrum methods. The amplifier directly modulates both phase and pulse-position simultaneously that is resonant yet produces spread-spectrum power.

We demonstrate a 23 W amplifier spreads over 90% of the power from 1 MHz to 20 MHz with up to 80% efficiency.
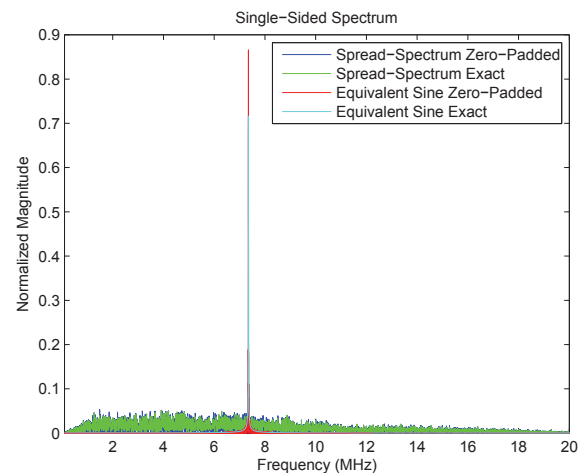

Fig. 1. Exact FFT of spread-spectrum sequence (RBW = 9 kHz). Note that the sine wave frequency 7.35 MHz is not a multiple of 9 kHz. Magnitude is normalized to unit spread spectrum pulse amplitude. Spread spectrum pulse-duty of 0.75 is included in the calculation of the equivalent single-frequency sine wave.

An advantage of spread-spectrum modulation with a resonant topology is that switching can be varied to match changes in resonance due to load or voltage-dependent components such as switch capacitance, which we show improves efficiency.

There are several improvements in this paper to the sequence optimization described in [34]. First, the pulse duty-cycle is held constant for a given optimization; the pulse duty-cycle is defined as the ratio of the time the pulses occupy in a given sequence to the total duration of the sequence (duration at zero, or zero duration, plus duration of pulses). The number of pulses in the sequence was increased from 1024 to 2048, but decreased the time resolution of the zero durations from 1/30 of a single pulse duration to 1/18, due to FPGA timing constraints at the new operating frequency, which is almost 150% higher. Fig. 1 shows that the ratio of the highest peak of the spread spectrum is over 16 times lower than that of a single-frequency sine wave with the same average power. The FFT spectrum was calculated with a 9 kHz RBW (resolution
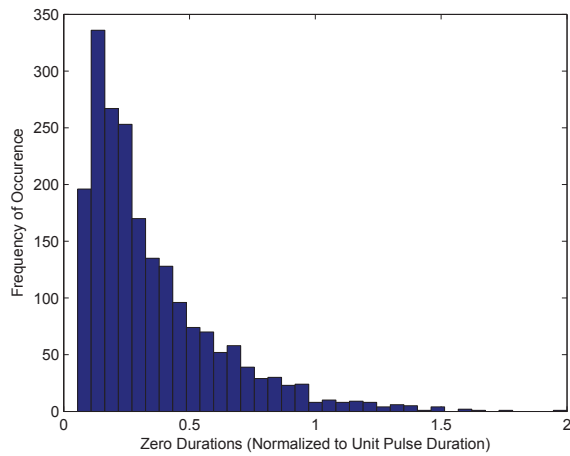
Fig. 2. Histogram of the zero durations for unit pulse duration. The sequence optimization was constrained to a pulse duty-cycle of 0.75.

(a) Dual-Switch Push-Pull

(b) Proposed Quad-Switch Push-Pull Topology

Fig. 3. Inverse Class D Derived Amplifiers with Wireless Power Transfer Loads.

bandwidth), which is specified for CISPR22 between 150 kHz and 30 MHz.

The pulse-duty of 0.75, among other optimized spread sequences, was a tradeoff between a higher spreading figure of merit (average power ratio to spectral peak) and lower conduction losses from current-carrying, zero-voltage durations. A histogram is shown in Fig. 2 of the distribution of zero durations when the total zero duration is constrained in the optimization. The results are different from that in [34] because of the zero duration constraints and the details of performing such an optimization will be described in a future paper.

II. COMPARISON OF D^{-1}-DERIVED TOPOLOGIES TO OTHER AMPLIFIERS

Class E amplifiers are conventionally used in high frequency amplifiers including those for wireless power transfer because both zero voltage switching and zero voltage derivative switching can be guaranteed over a range of operating conditions [35], ensuring that the body diode of FET switches do not turn on with the resulting reverse recovery loss. In [32], a spread spectrum system using pseudorandom modulation based on a class D (voltage mode) amplifier is described. The disadvantage of this conventional class D amplifier implementation is that the switches do not operate with zero voltage switching and hence incur higher switching losses, which limits its applicability in applications that require high frequency and higher voltage.

With the advent of gallium nitride (GaN) FETs, there is no reverse recovery loss because the inherent parallel diode is majority carrier. Even though the voltage drop is higher (2V vs. 0.8V for an equivalent Si MOSFET) the current conducts in the diode for only a short period of time, corresponding to a switch delay margin to ensure that the switch turns on at essentially zero voltage. This tolerance to switch timing means that the topology is relatively insensitive to mismatches in gate drive delay, device parasitics and parameters, and layout,
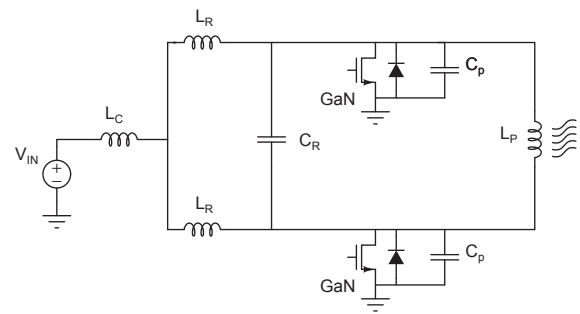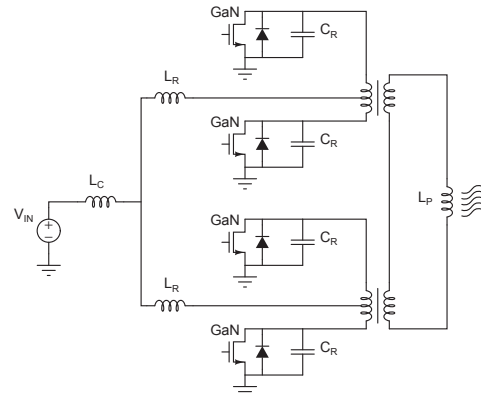
among others. Several advantages of topologies derived from the D^{-1} amplifier include:
1) Guaranteed zero voltage switching for high frequency/high voltage operation,
2) Guaranteed zero voltage switching from full load to no load,
3) Tolerance to unloading/device removal; ZVS guaranteed with voltages and currents bounded. All that is needed are drain clamps that absorbs a fixed amount of energy,
4) In the ideal case (i.e. current source input and no parasitics), when the switches are all closed, the states are essentially frozen (inductor currents unchanged and capacitor voltages zero). This allows pulse position modulation that is not limited by a resonance, e.g. output resonance of a class E.
5) Piecewise 2^{nd}order, unlike a Class E or other higher order amplifiers (F, EF, etc.), which means that much of the time domain behavior can be reliably predicted from linear analysis.

III. PRINCIPLES OF OPERATION

Quad-switch push-pull operation allows the independent and simultaneous modulation of the phase (polarity) and position of half-sine wave pulses. The amplifier is fed by a dc voltage source (V_{IN}) to ideally create a current source through a choke for what is essentially a switched parallel-resonant circuit. A push-pull configuration is advantageous because
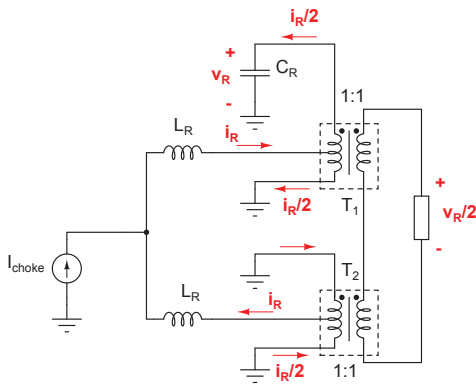
Fig. 4. Resonant Operation of QSPP Amplifier

Fig. 5. Proposed Quad-Switch Amplifier with Cross-Coupling Capacitors to Reduce Switch RMS Current.

ground-referenced gate drives can be used, hence obviating the difficulties in level shifting and floating gate drives at higher frequencies. Resonance is achieved through the center-taps of two transformers; although the use of transformers as combiners in RF power amplifiers is well-known [36], [37], consideration and analysis in their design for a particular topology is required.

In the proceeding design equations, approximations are used so that intuition towards design tradeoffs are less encumbered.

The basic operation is illustrated in Fig. 4. In this simplified model, the current through the choke is dc and i_R and v_R are the resonant current and voltages, respectively. This results in a half-sine voltage pulse to the output that is half the amplitude of the capacitor resonant voltage with a resonant frequency given by,

$$\omega_0 = \frac{1}{\sqrt{L_R C_R}}. \tag{1}$$

Referring to Fig. 3, during the zero duration interval t_{zd}, all the switches are ON and the resonant current i_R in Fig. 4 is constant and the voltages (including v_R) are zero. During a pulse, only a single switch is OFF, v_R resonates, and all the other switch behave as synchronous rectifiers so there is no diode voltage drop. After a resonant pulse, v_R is zero and the switch is turned ON at zero voltage switching. The timing margin for turning the switch ON is relatively relaxed because the reversing resonant current $i_R/2$ can turn the GaN FET body diode ON with only a small voltage drop ($\sim$2 V) for a short period of time corresponding to the timing error; as previously mentioned, no reverse recovery loss is incurred.

The switching pattern must alternate between the switches on T_1:(S_1, S_2) and T_2:(S_3, S_4) in Fig. 4 because the resonant current i_R alternates, i.e. only one of the switches necessarily on T_1 can be OFF to block positive i_R and charge the resonant capacitance, and vice-versa for negative i_R. Another constraint is that the time average of volt-seconds (or flux) in the transformers must be zero. One interesting consequence is that a symmetrical sine wave cannot be constructed. This can also result in a resonant current distortion from the magnetizing current that is dependent on the accumulated volt-seconds from the switching pattern. The construction of the
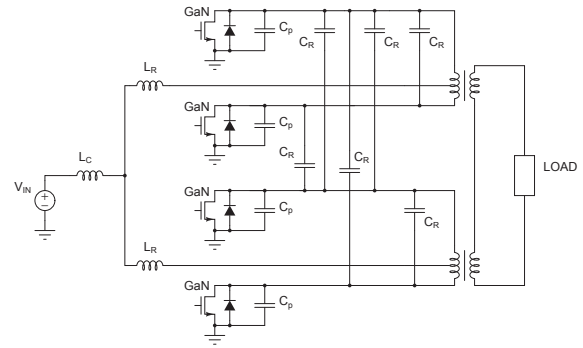
switching pattern is described in [34]: the switching pattern is constructed from a dictionary of subsequences each with zero average volt-seconds.

By using a cross-coupling capacitor, as in Fig. 3a, part of the resonant current is diverted from the switch ON resistance $R_{ds,on}$; to first-order, i.e. $R_{ds,on} \ll \sqrt{L_R/C_R}$,

$$i_{sw,on} = \frac{C_p}{C_p + C_R} i_R. \tag{2}$$

The idea of a cross-coupling capacitor can be generalized from the two-switch amplifier, to the quad-switch amplifier in Fig. 5. By placing the cross-coupled capacitors on the switch side of the transformer, the leakage inductance can be absorbed into the resonant inductors L_R. The switch current for this topology is

$$i_{sw,on} = \frac{C_p}{C_p + 3C_R} \frac{i_R}{2} \tag{3}$$

and the pulse resonant frequency is given by

$$\omega_0 = \frac{1}{\sqrt{L_R(C_p + 3C_R)}}. \tag{4}$$

The Q of the pulse parallel-resonance can be calculated from the output load,

$$Q = \frac{N^2 R_{LOAD}}{\sqrt{L_{R,eff}/C_{R,eff}}}, \tag{5}$$

where $N^2 R_{LOAD}$ is the load resistance reflected to the resonant terminal (C_{node} in Fig. 7); $L_{R,eff}$ and $C_{R,eff}$ are the effective resonant inductance and capacitance, respectively. For the QSPP topology with a trifilar-wound transformer ($N = 2$) and a 50 Ω load in Fig. 9, $Q \approx 3.5$.

The input choke L_C in Fig. 3b is typically designed with an inductance L_{choke} so that the current ripple is small, and hence must be designed for the largest zero duration $T_{z,max}$ for the sequence (see Fig. 2). The maximum current ripple is

$$\max \Delta I = \frac{V_{dc}}{L_{choke}} T_{zd,max}. \tag{6}$$

Also, by observing that the average voltage across the inductor L_C must be zero, V_{dc} is equal to the time-average of
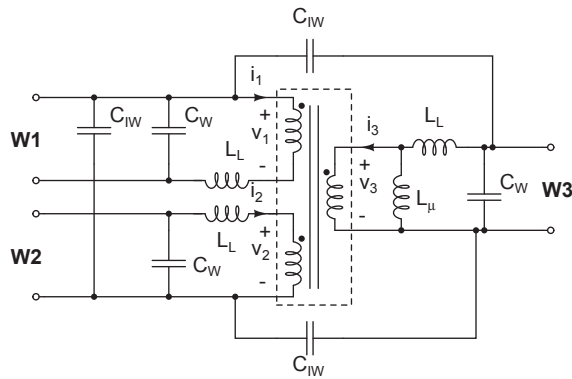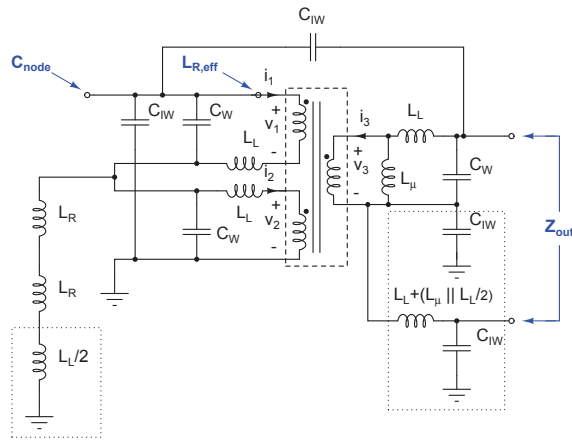
Fig. 6. Broadband Transformer Model.

Fig. 7. Stacked Transformer Model.

TABLE I
COMPARISON OF ANALYTICAL CALCULATION AND SIMULATION

Parameter	Analytical	Simulated	Experiment
$L_{R,eff}$	1.24 μH	1.25 μH	
$C_{R,eff}$	393 pF	400 pF	
f_P	7.2 MHz	7.53 MHz	7.35 MHz
L_{out}	450 nH	455 nH	
C_{out}	27.5 pF	26 pF	
Z_{out}	128 Ω		
f_T	45.2 MHz	43.21 MHz	

the sum of the drain voltages. For sinusoidal drain voltages with zero durations by overlapping switch ON-states,

$$V_{ds,pk} = \frac{2\pi V_{dc}}{D_p}, \tag{7}$$

where $D_p = T_p/T_{zd} + T_p$ is the pulse duty-cycle. This results in a voltage boost from the duty-cycle, similar to a boost converter, which can be advantageous in some applications.

IV. TRANSFORMER DESIGN AND PROTOTYPE

A simple, broadband model with no resistances, which can be derived from [38], [39] for a trifilar-wound transformer because of inherent symmetries, is illustrated in Fig. 6. This model exposes how most of the transformer inductances and capacitances can be absorbed into a second-order resonator.

If we replace the ideal transformers in Fig. 4 with the model in Fig. 6, we can arrive at the simplified model in Fig. 7. We're interested in the three denoted terminals: $L_{R,eff}$—the effective resonant inductance from explicit inductors, transformer inductances, and transformer behavior, C_{node}—the added capacitance from the transformer parasitics, and Z_{out}—the imaginary portion of the output impedance.

If the terminal loading at Z_{out} is open, $L_\mu \gg L_L$, and we ignore the capacitances,

$$L_{R,eff} = 8L_R + 4L_L, \tag{8}$$

where the boxed $L_L/2$ is the terminal inductance from T_2. The assumption that the output is open is a good approximation for the design of an amplifier with low output spectrum distortion; this means $Q > \approx 3$ and in the case of an output inductor for wireless power transfer, $L_{out} \gg L_L$.

$C_{node} \approx C_{IW}$ because typically $C_W \ll C_{IW}$ and we focus on the germane resonance and ignore the higher order LC effect, which is justified below when examining a more complete model using SPICE ac analysis. The effective resonant capacitance is

$$C_{R,eff} = C_P + 3C_R + C_{IW}, \tag{9}$$

where the device capacitance C_P includes both the GaNFET and clamp diode capacitances.

The useful bandwidth of the transformer is largely determined by terminal resonance ω_T at Z_{out} and load matching, the Z_{out} characteristic impedance. Typically, the transformer resonance ω_T is designed to be much higher than the pulse resonance ω_P. In this case effective capacitance $C_{R,eff}$, which includes the terminal capacitance at C_{node}, is in essence a short at ω_P. In this case, the output appears as a parallel resonance with

$$L_{out} = 3L_L, \qquad L_\mu \gg L_L, \tag{10}$$

$$C_{out} = \frac{C_{IW}}{2}, \qquad C_W \ll C_{IW}. \tag{11}$$

To verify the modeling as well as some of the approximations, an ac analysis was performed in LTspice for the switch configuration corresponding to *S1:OFF*. As illustrated in Fig. 8, this model uses nominal values for inductances, capacitances, and resistances that were measured from the transformer, gathered from datasheets for the devices, and estimated for trace parasitics. To examine the pulse resonance, the short across C19 in Fig. 8 is removed and I1 is placed across it instead. The impedance seen at this S1-node is plotted in Fig. 9 for both light load (10 kΩ) and full load (50 Ω). The peak in the lightly loaded condition nearly corresponds to the model natural frequency in (9) and the shift in the peak
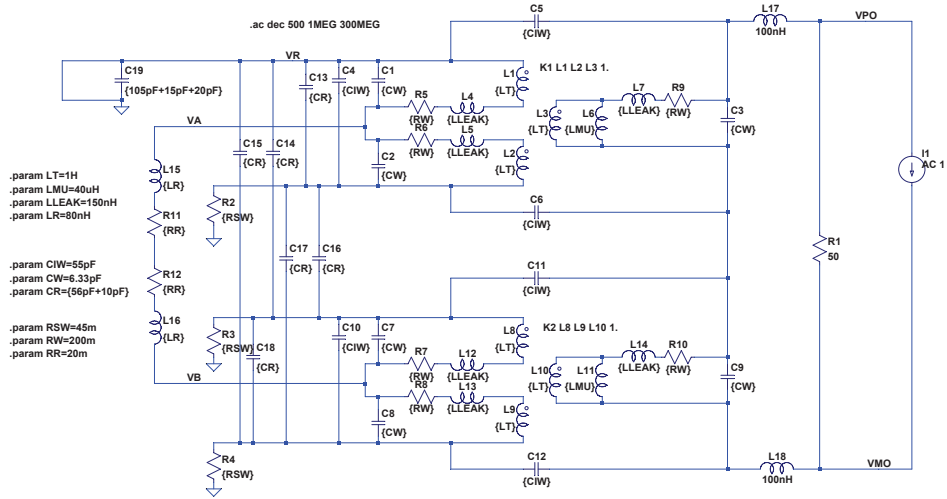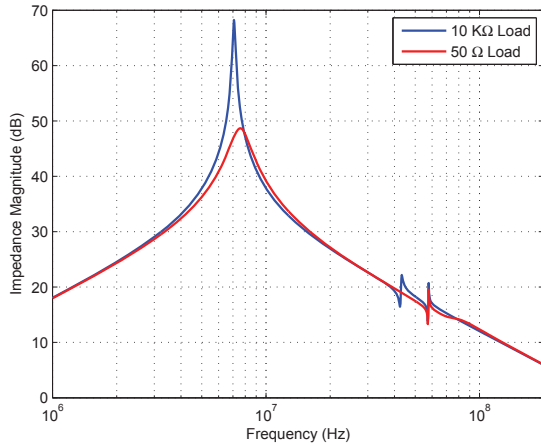
Fig. 8. LTspice AC Analysis Model.

Fig. 9. Simulated Impedance at Resonant Capacitor Node for Lightly Loaded (10 kΩ) and Fully-Loaded (50 Ω) Output.
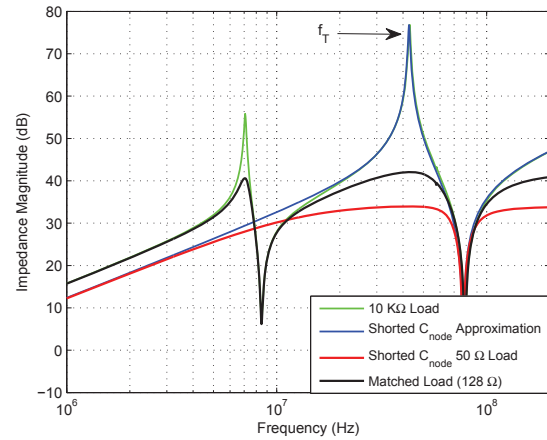

Fig. 10. Simulated Output Impedance.

corresponds to higher loading. L17 and L18 correspond to layout and lead inductance to the load; these inductance are neglected in some of the analysis for simplification because the perturbation (9.2 Ω at 7.35 MHz) does not impact the calculation significantly.

The correspondence of the shorted-node approximation used in 10 to the more accurate model in Fig. 8 is illustrated in the lightly-loaded (10 kΩ) higher frequency peak in Fig. 10. It is also apparent from this figure that 50 Ω loading is overdamped and a matched load (128 Ω) is shown for comparison. A comparison of approximate analytical calculation and values derived from the LTspice simulations, illustrated in Table I, shows good agreement; f_P corresponds to the pulse natural frequency and f_T to the output's natural resonant frequency.

Several transformers were designed and built using toroids (1015-1) of the M-material ($\mu = 125$), which is a NiZn ferrite from National Magnetics Group, Inc. Three promising designs are illustrated in Table II. The cores were configured in a binocular-style and stacked. PTFE-insulated, stranded wire

TABLE II
MEASUREMENT OF THREE TRANSFORMER DESIGNS

Parameter	2x24ga-Trifilar	20ga-Trifilar	24ga-Trifilar
Core[1]	5x2	4x2	3x2
Turns	6	7	8
L_μ	40 μH	39 μH	43.7 μH
L_{LEAK}	150 nH	195 nH	276 nH
C_{IW}	55 pF	20 pF	30 pF
C_W	6.6 pF	0 pF[†]	0 pF[†]
R_W[1]	0.25 Ω	0.45 Ω	0.5 Ω
R_W[2]	0.06 Ω	0.1 Ω	0.15 Ω

[1] m stacked toroidal cores X 2 (binocular-style).
[2] Approximate resistance at 10 MHz.
[3] Approximate resistance at 1 MHz.
[†] Not measured.

was used for low permittivity and loss, hence lower per unit capacitance and resistance: 24 ga. (19/36 strand) Alpha 5854 and 20 ga. (19/32 strand) Alpha 5856. The final prototype used

3371

the "2x24ga-Trifilar" design, which consisted of 2 pairs of 24 ga. trifilar windings paired in parallel with windings matched for the smallest interwinding capacitance C_{IW}. The parallel windings resulted in a lower winding resistance, but traded off a higher interwinding capacitance.

V. 23 W AMPLIFIER PROTOTYPE

A 23 W prototype illustrated in Fig. 11 was constructed with a resonant frequency nominally at 7.4 MHz, spreading power over 1–20 MHz. The prototype includes a 4-layer pcb module with the quad GaNFETs, their associated gate drives, and cross-coupling capacitors in a tight layout to minimize drain inductance. The magnetics, drain protection, and probe points are contained in the main 2-layer pc board.

The amplifier switches are controlled by an external board with a Xilinx Spartan 6 XC8SLX16 FPGA that stores the ternary sequences and zero durations timings using programmed timers and state machines to determine switching state. The FPGA clock frequency of 280 MHz, along with digital timing constraints limits the basic time resolution. Alternatively, a simple integrated circuit could be developed with a triggered ROM or EEPROM to store the modulation encoding, high speed counters, and digital delays enabling much higher operating frequencies.

A. Hardware Design

1) Input Choke: The input choke consists series connection of 16-turns of 20 gauge wire wrapped on a stack of 3, M-material toroids (1015-1) from National Magnetics and 2 paralleled 56 μH inductors from the EPCOS B82111E Series.

2) Resonant Components: 56 pF, 500 V, high Q resonant capacitors (E-series from Johanson Technology). No explicit L_R inductors were used; instead, transformer leakages and board parasitics provided the required resonant inductance.

3) Semiconductor Switches: EPC2019 GaN (gallium nitride) FETs from EPC.

4) Gate Drives: Each FET is driven by three SN74LVC2GU04DCKR dual logic inverters.

5) Drain Clamps: DFLS1200 Schottky diode rated for 200 V, 1 A, nominal capacitance of 23 pF, in series with a 1SMB5953BT3 150 V, 3 W zener.

B. Quad GaNFET Module

The critical components including the GaNFETs, gate drives, and cross-coupling capacitors are assembled on a small pc board. This eases prototyping by allowing a high density of components to be assembled on a board which is easy to manipulated. In addition, because the module is not directly bonded to the main board, it is tolerant of board flex from the heavier components and connections. The module was designed to minimize drain inductance and therefore trades this off for greater layout capacitances, which are not detrimental because it is absorbed into the D^{-1}topology's 2^{nd}order resonance. The layout capacitance to ground from the coupling capacitors is 10 pF and the added drain capacitance is 20 pF.
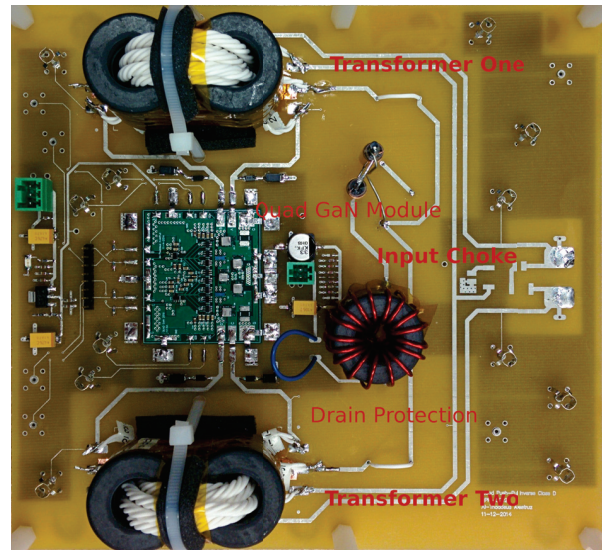

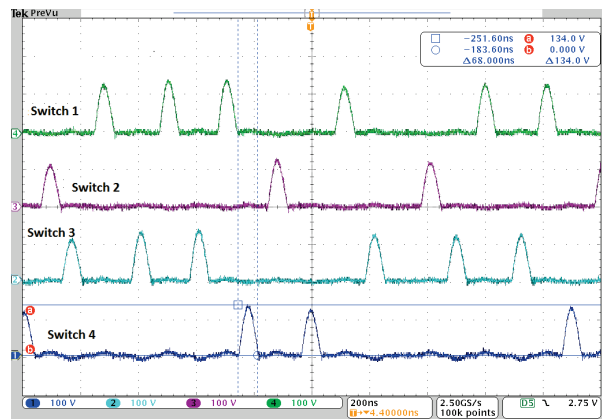Fig. 11. Prototype of the QSPP Spread Spectrum Amplifier.

Fig. 12. Drain Voltages for the amplifier prototype operating at 23 W into a 50 Ω Load.

C. Experimental Results

The amplifier drain voltages are shown in Fig. 12. The waveforms were measured with Tektronix TPP1000 probes and a 1 GHz MSO4104B oscilloscope. The waveforms show no spurious oscillations and good zero voltage switching.

The output voltage waveform is shown in Fig. 13 using a 200 MHz THDP0200 Tektronix Differential Probe. Peak-to-peak voltage is approximately 120 V and an output power of about 20 W into a 50 Ω load. From previous discussion, the output loading at 50 Ω is such that the output resonance is overdamped, which causes some distortion in the zero crossings at phase reversals. However, this distortion does not appear to significantly impact the spectrum shown in Fig. 14, which derived from the experimental waveform in Fig. 13. The spectrum is plotted from 150 kHz to 30 MHz, which is the relevant CISPR 22 frequency range and requires a 9 kHz resolution bandwidth. When plotted similarly and compared, the experimental output spectrum in Fig. 14 is in
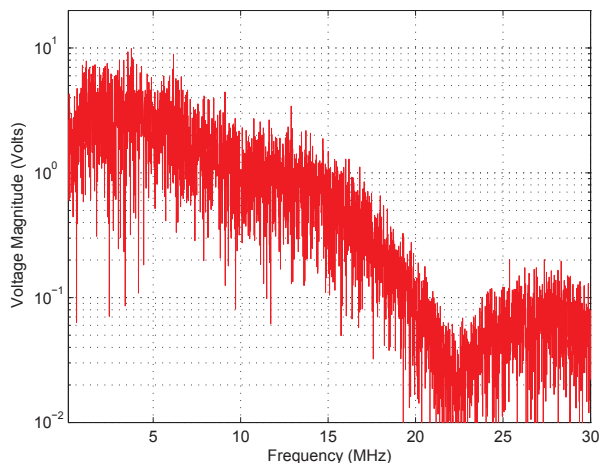
Fig. 13. Output Voltage.

Fig. 14. Output spectrum using an FFT of the experimental output voltage with a RBW = 9 kHz and a Gaussian window with 50 MHz bandwidth.

good agreement with the predicted output spectrum in Fig. 1.

The amplifier efficiency, $\eta = P_{out}/(P_{dc} + P_{gate})$ shown in Fig. 15 includes the loss from the gate drive, which is 156 mW at 23 W and corresponds to the highest average operating frequency and drain voltage; the efficiency error bars are estimated to span about 2%. Above a certain power level, the drain clamps conduct, hence reducing efficiency. The drain clamps use a 3 W, 150 V Zener with a high voltage Schottky in series, which is conservative for the 200 V GaN FETs.

Over the variation in power and for a fixed 50 Ω load, the output voltage and hence the peak drain voltage vary. Because the device capacitances are voltage dependent, from (9) the resonant frequency of the pulse changes, resulting in an error in the zero durations, excessive body diode turn-on time, and subsequent pulse duty-cycle error. This results in decreased efficiency if switch timing is not corrected for drain voltage as illustrated in Fig. 15. With this timing correction, which can be performed programmatically by the controller, an efficiency up to 80% can be achieved.

VI. CONCLUSION

We presented a new RF amplifier topology for spread spectrum power applications. This resonant topology improves
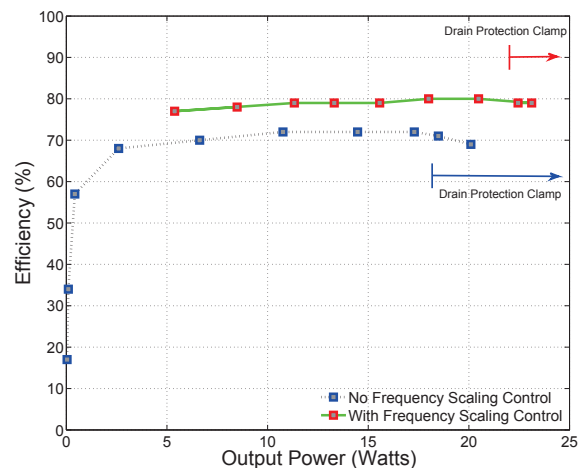

Fig. 15. Efficiency.

on prior designs to operate at high frequency: zero voltage switching, a reduction in switch rms current, and absorption of device capacitance. Most of the transformer parasitics such as leakage inductance and most of the capacitances are also absorbed, while those that cannot can be made negligible. A 23 W prototype was demonstrated that operates at up to 80% efficiency, and over 90% of the power from 1–20 MHz. The amplifier uses a spreading sequence to control the switches so that both phase and pulse-position are directly modulated.

Applications for this technology include wireless power transfer, RFID, and electronic ballasts where EMI is an important concern, not only in critical applications such as medical environments, but also in portable and wearable applications.

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